

*Greetings from
Georgia Tech*

3D Modeling and Process Design Kits for Flexible Hybrid Electronics (FHE) Challenges and Opportunities

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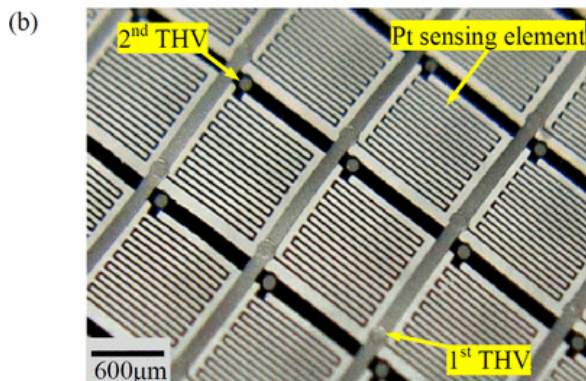
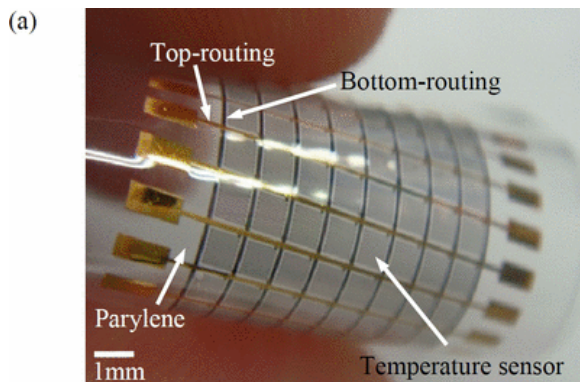
Overview

- Flexible Hybrid Electronics – Some Applications
- Digital and RF Design Methodologies/Flows
- Process Design Kits and 3D Multi-physics modeling
- Summary

FHE Applications

Sensors

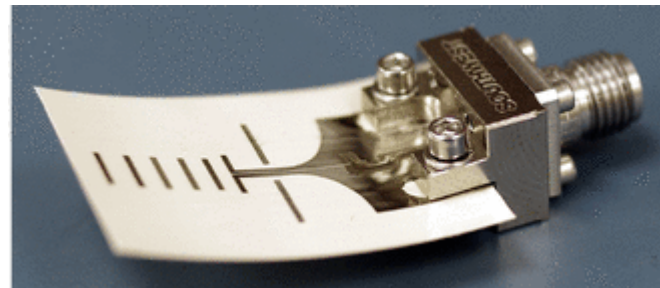
Example: Flexible temperature sensor array



Source: W. S. Su et al., "A polymer stacking process with 3D electrical routings for flexible temperature sensor array and its heterogeneous integration," 16th International Solid-State Sensors, Actuators and Microsystems Conference, Beijing, 2011.

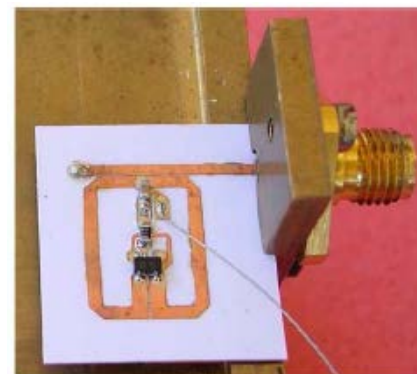
RF / mm wave

Example: Printed Yagi-Uda antenna



Source: B. K. Tehrani et al., "Inkjet Printing of Multilayer Millimeter-Wave Yagi-Uda Antennas on Flexible Substrates," in IEEE Antennas Wireless Propag. Lett., vol. 15, no. , pp. 143-146, 2016.

Example: Flexible voltage controlled oscillator

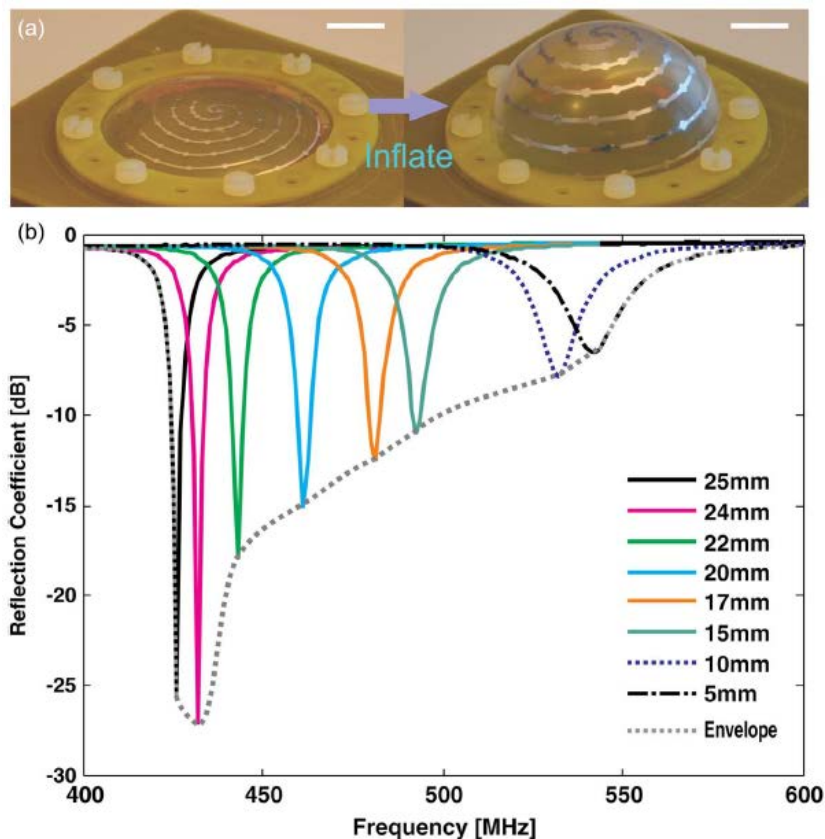


Source: F. Alimenti et al., "A 1.2 V, 0.9 mW UHF VCO Based on Hairpin Resonator in Paper Substrate and Cu Adhesive Tape," in IEEE Microw. Compon. Lett., vol. 23, no. 4, pp. 214-216, April 2013.

FHE Applications (cont.)

Microfluidics (+ antenna)

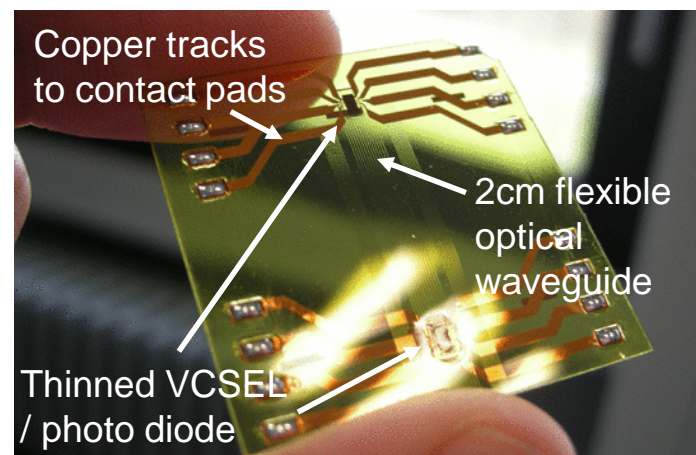
Example: microfluidic tunable 3DESA



Source: Z. Wu, K. Hjort and S. H. Jeong, "Microfluidic Stretchable Radio-Frequency Devices," in *Proceedings of the IEEE*, vol. 103, no. 7, pp. 1211-1225, July 2015.

Optics

Example: Fully embedded flexible active optical link



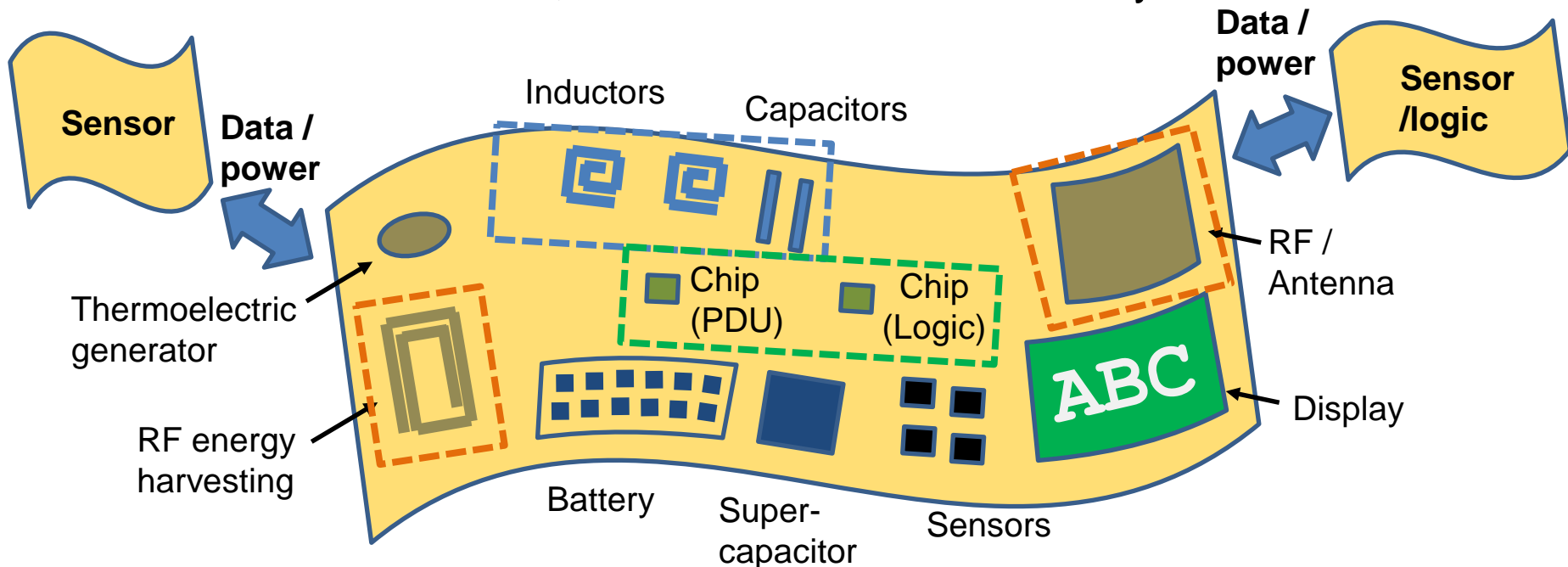
Source: E. Bosman et al., "Highly Reliable Flexible Active Optical Links," in *IEEE Photonics Technology Letters*, vol. 22, no. 5, pp. 287-289, March 1, 2010.

Flexible Hybrid Electronic (FHE) Systems

- Thinned chips
- R, L, C
- Sensors
- Antennas
- Battery
- ... many more!

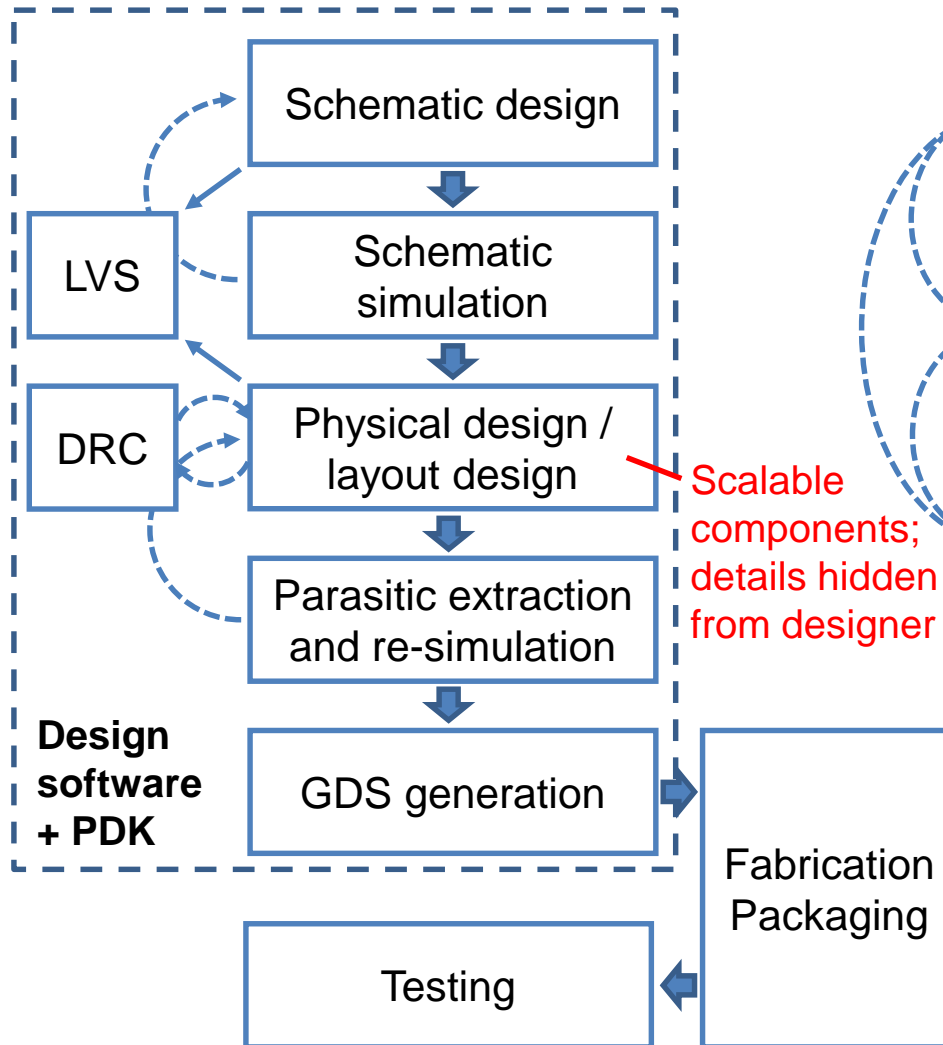
To a designer:

- Components connected together on a (*Flexible*) Substrate
- Each component performs a function
- Components connected together leads to a system response
- Verifies System functionality prior to tapeout
- So, what is different with FHE Systems?

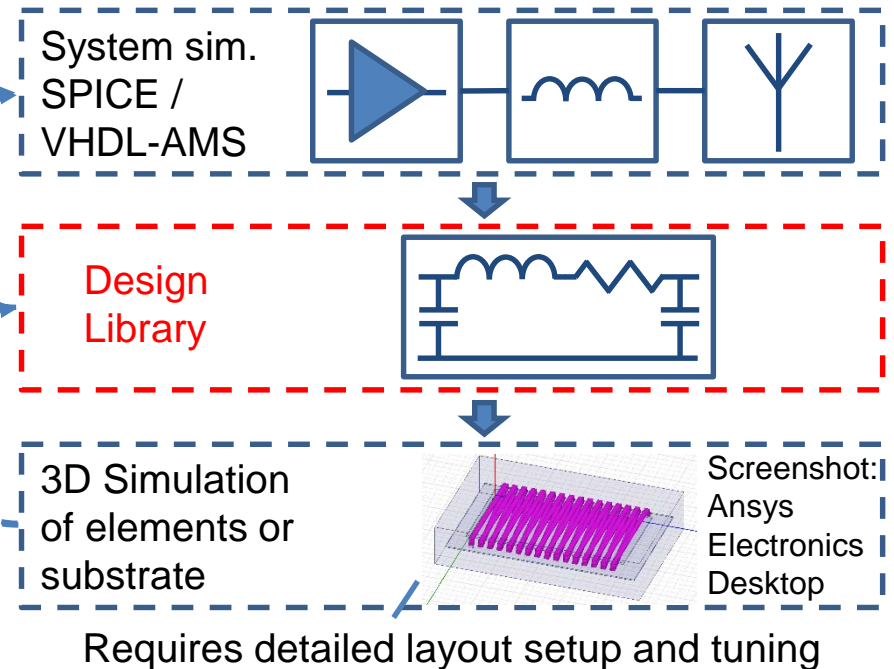


Let's look at Two Different Design Methodologies/Flows

CMOS Chip Design



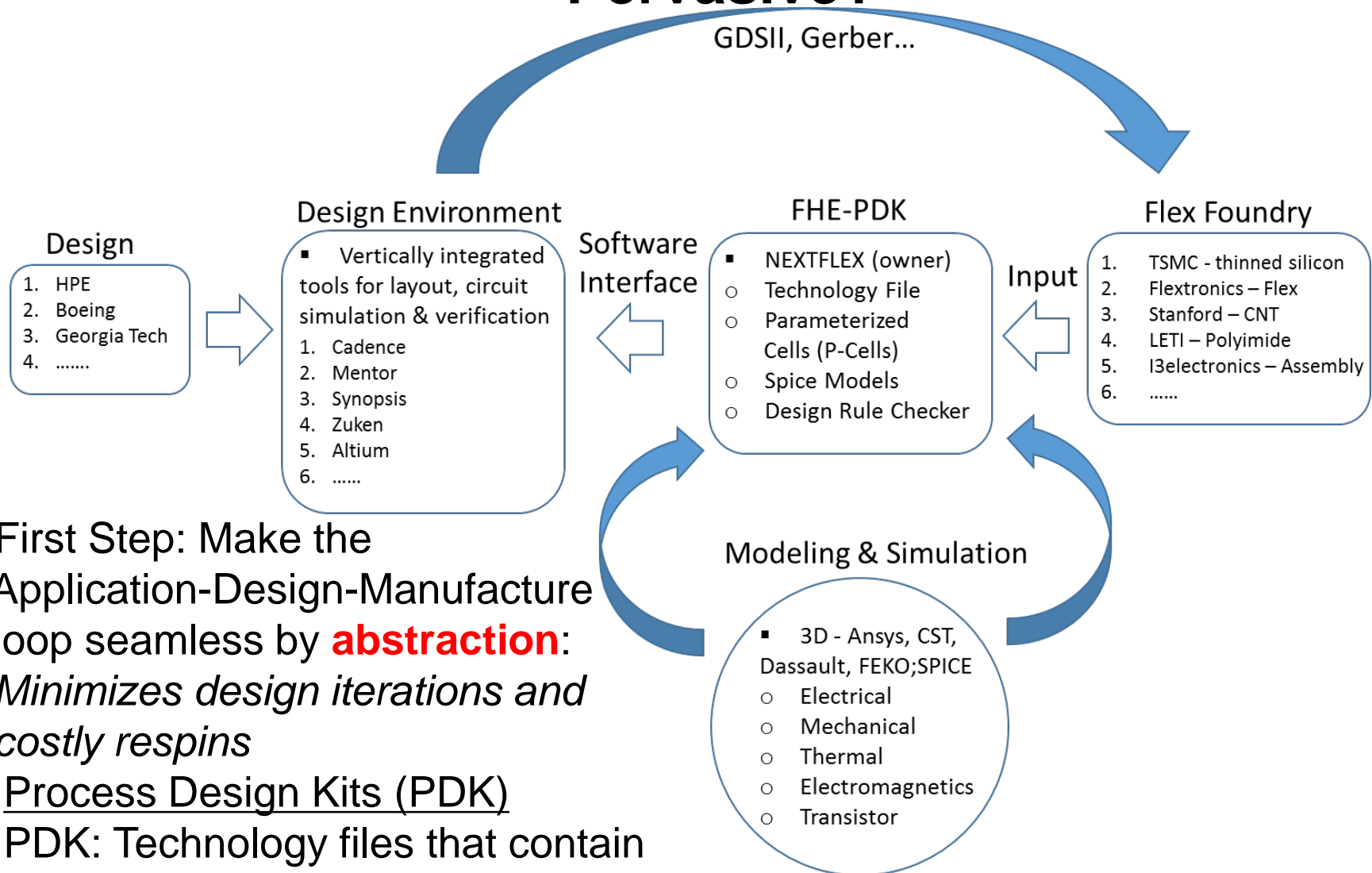
RF Design



Key Commonality

- CMOS: Scalable Components
- RF: Design Library
- These significantly reduce *design cycle time & minimize respins*

What is Required for FHE to become Pervasive?



- ❑ First Step: Make the Application-Design-Manufacture loop seamless by **abstraction**: *Minimizes design iterations and costly respins*
- ❑ Process Design Kits (PDK)
- ❑ PDK: Technology files that contain design rules, layout and model libraries

Abstraction and Flexible Electronics

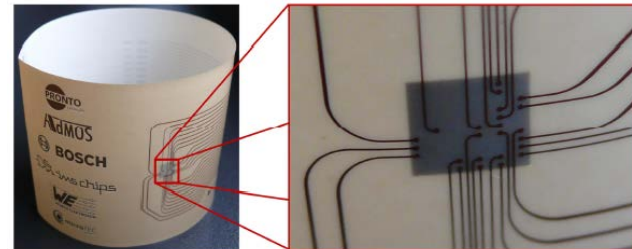
What do I mean?



Picture: PowerAct vibration sensor and dampener; Source: <http://ww1.prweb.com/prfiles/2008/08/12/416804/pa16nisopipe.jpg>



Picture: OpenGo Wirelessly connected sensor insole; Source: <http://www.moticon.de/products/science-research>



J. Wolf, J. Kostelnik, K. Berschauer, A. Kugler, E. Lorenz, T. Gneiting, C. Harendt, and Z. Yu, "Ultra-thin Silicon Chips in Flexible Microsystems," ECWC13, 2014.

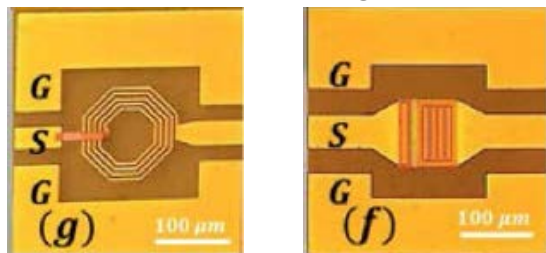
- Known and unknown bending condition
 - Electrical properties change
 - Bending/Stretching/Twisting
 - Material & electrical properties change due to fatigue
 - Ultra-thin chip connected to bendable traces
 - Signal characteristics change due to changing load conditions
- In all these cases the designer is only interested in the electrical response
 - However, the operating conditions affect the electrical response
 - Can these effects be abstracted into a high level model where the model can be parameterized based on geometrical and material parameters only? The designer doesn't see the underlying mechanical and thermal details

Example: Impact of Deformation on FHE

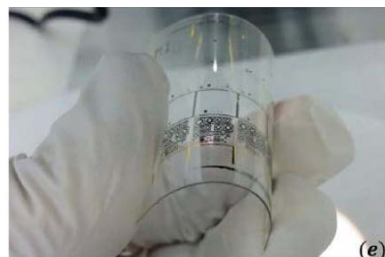
Impact of deformation on capacitor and inductor on flexible substrate

- Deformation and strain on electrical properties need to be modeled
- May often be approximated by simple relations → Use this to reduce number of 3D simulations and simplify behavioral models
- Simple approximations may not hold under extreme bending – approaches need enough “intelligence” to take that into account
- **Parameterized Model: $L(W, T, S, \epsilon_r, \text{bending radius})$**

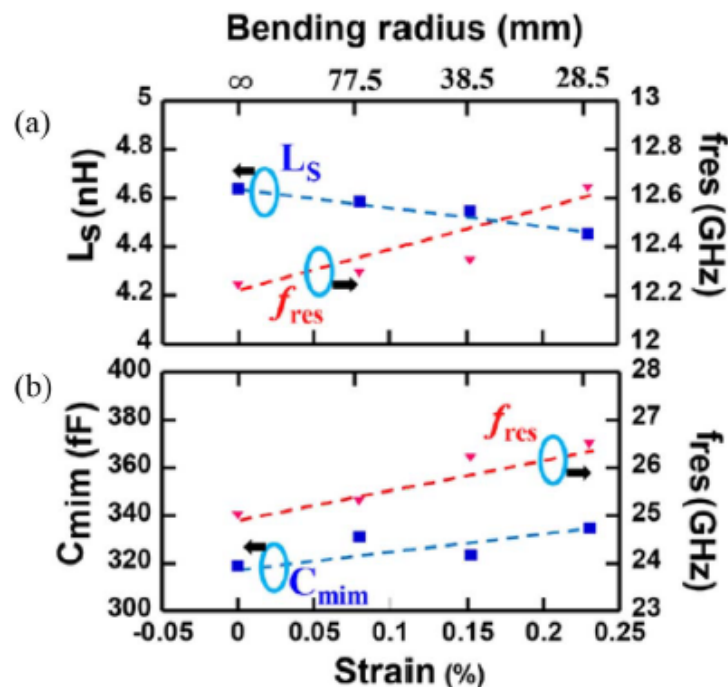
Flexible inductor (left) and capacitor (right)



Bending of flexible substrate



Impact of bending / strain on electrical properties (inductance / capacitance)



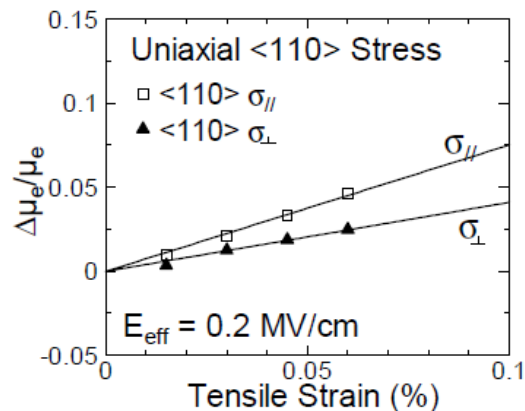
Source: S. J. Cho et al., "X-Band Compatible Flexible Microwave Inductors and Capacitors on Plastic Substrate," in *IEEE Journal of the Electron Devices Society*, vol. 3, no. 5, pp. 435-439, Sept. 2015.

Example: Thinned Chips

Impact on electrical characteristics due to bending of thinned chips

- Stress due to bending impacts electron mobility and therefore electrical properties
- Impact is represented as a parameterized behavioral model
- Opportunity: some relations show comparatively simple behavior – suitable ways to make use of this fact can be investigated

1. Electron mobility vs. strain



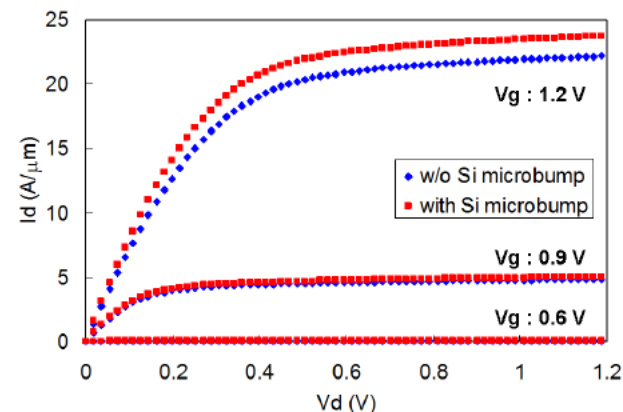
Source: K. Uchida et al., "Physical mechanisms of electron mobility enhancement in uniaxial stressed MOSFETs and impact of uniaxial stress engineering in ballistic regime," IEEE International Electron Devices Meeting, Washington, DC, 2005, pp. 129-132.

2. MOSFET drain current vs. carrier mobility

$$\frac{\delta I_D}{I_D} = \frac{\delta \mu}{\mu} (1 - B)$$

Source: M. S. Lundstrom, "On the mobility versus drain current relation for a nanoscale MOSFET," in IEEE Electron Device Letters, vol. 22, no. 6, pp. 293-295, June 2001.

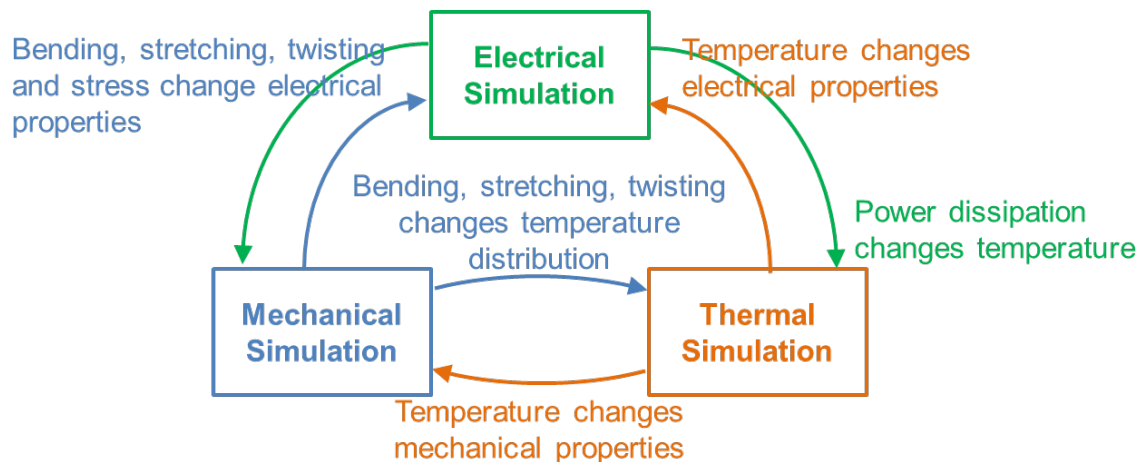
3. Impact of stress due to Si microbump in thinned chip



Source: H. Kino et al., "Impacts of static and dynamic local bending of thinned Si chip on MOSFET performance in 3-D stacked LSI," 2013 IEEE 63rd Electronic Components and Technology Conference, Las Vegas, NV, 2013, pp. 360-365

But how do you populate the PDK?

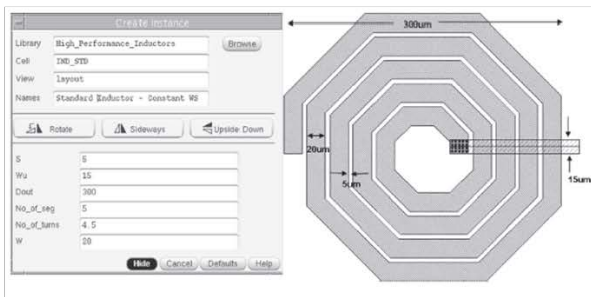
2D/2.5D/3D Multi-physics Simulation



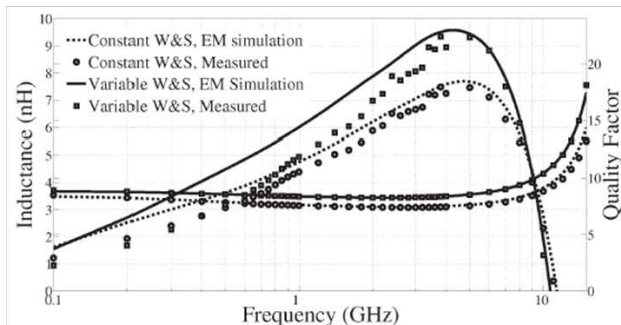
- Model the operating conditions
- Determine the parametric space
- Ensure that the mechanical, thermal and electrical behaviors are adequate in this space
- Done by the foundry providing the component

Parametrized Models

Model for on-chip spiral inductor



Simulation based on P-cell vs. measurement



- Map the parametric space to the electrical response
- Develop scalable models: linear and non-linear
- Scalable models provided using standardized format
- Used as P-cells in PDK

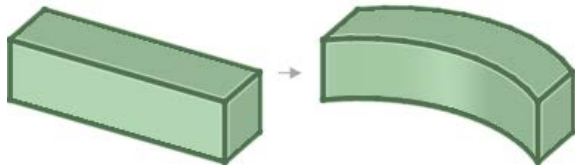
Source: R. R. Manikandan, V. N. R. Vanukuru, A. Chakravorty and B. Amrutur, "A parameterized cell design for high-Q, variable width and spacing spiral inductors," 2014 IEEE International Microwave and RF Conference (IMaRC), Bangalore, 2014, pp. 312-315.

Some Challenges and Opportunities in Multi-physics Modeling

Deformation (bending / stretching / twisting) of structures has to be taken into account

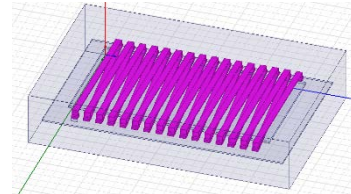
- Programs / CAD tools exist that can deform structures (e. g. Ansys SpaceClaim)
- However, integration with electromagnetic 3D modeling tools needs to be developed

Bending of a beam in Ansys SpaceClaim



Source:
<http://help.spaceclaim.com/2015.0.0/en/Content/Beams.htm>

Simulation tools sweep geometry parameters, but do not provide options for deformation



Screenshot from an electromagnetic simulation tool (Ansys Electronics Desktop)

Desired scenario:

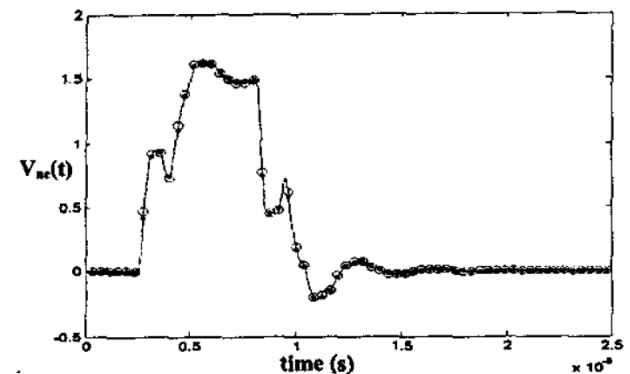
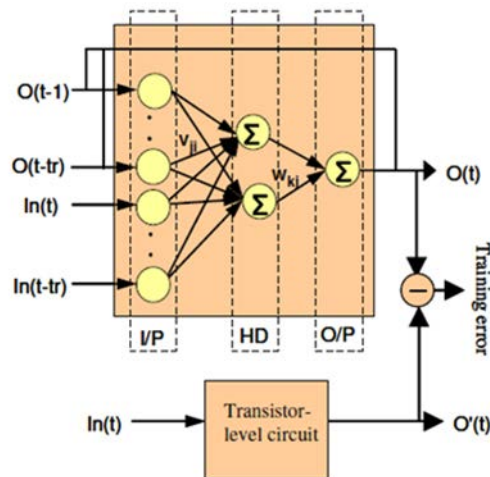
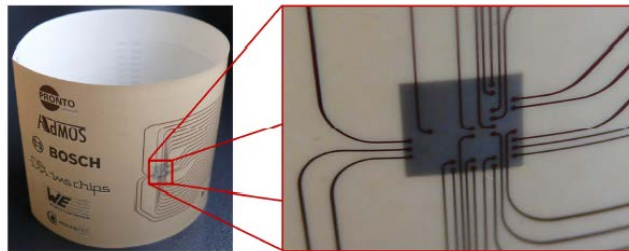
User defines range of deformation scenarios (such as minimum and maximum bending angle)



Simulation tool automatically selects points to be simulated and provides interpolated results for the defined range

Some Challenges and Opportunities for Parameterized Behavioral Modeling

- ❑ Most of the work limited to LTI systems (inductors, capacitors ...)
- ❑ With FHE non-linear and time variant characteristics become important
 - Time dependent viscoelastic and viscoplastic behavior
 - Stress creates fatigue over time that affects resistance
 - Loading on thin chips changes with time thereby changing output signal
 - Thermal gradients change with time that change electrical characteristics
- ❑ Capturing such effects in a parametrized behavioral model can be difficult
- ❑ Opportunity to use Machine Learning based methods
 - Huge body of work available through Computer Science
 - Tool boxes available (Neural Networks



[1] B. Mutnury, M. Swaminathan and J. Libous, "Macro-modeling of non-linear I/O drivers using spline functions and finite time difference approximation," Electrical Performance of Electronic Packaging, 2003, Princeton, NJ, USA, 2003, pp. 273-276



Summary

- ❑ Process Design Kits (PDK) have become the norm for chip design
- ❑ Design libraries are used for RF design flows
- ❑ Such approaches are known to reduce design iterations and minimize respins
- ❑ For FHE to become pervasive PDKs are necessary

- ❑ Creating PDKs for FHE have their unique challenges
 - ❑ Need multi-physics modeling tools to predict behavior based on operating conditions: bending, twisting, stretching, temperature gradient ...
 - Some capabilities exist but others are required
 - ❑ Need parameterized behavioral modeling that capture non-linear and time variant characteristics
 - Use of Machine Learning a possibility

- ❑ Opportunity for the supply chain (eco-system) to come together to help create:
 - The design environment
 - Standardize data exchange formats
 - Create and support PDKs
 - Enhance multi-physics modeling specifically for FHE
 -

Thank You

