Georgia Tech Consortium on Integrated Approach to Power Delivery for Electronic Systems

I. Vision

Moore's law has been the driver for the semiconductor industry for more than four decades which has led to phenomenal transistor density within the chip, as shown in Figure 1. Since the mid-1990s, with the emergence of mobile phones and other consumer devices, package level integration has increased significantly as well. Sometimes referred to as "More than Moore" integration, these advances have led to the miniaturization of packages, integration of components into the package, miniaturization of components and introduction of new materials, leading to an increase in the system component density outside the chip, as shown in Figure 1. A combination of "Moore" (IC) and "More than Moore" (package) scaling has led to the shrinking of the size of electronic systems over the last two decades, and this trend is expected to continue in the future. Georgia Tech has been in the fore front for both Moore and More than Moore scaling technologies.

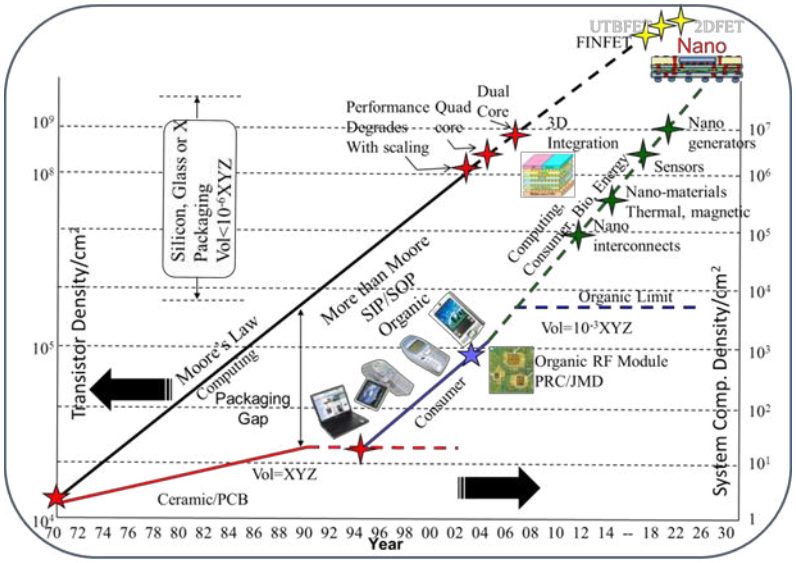

Figure 1: Transistor density and System component density trends. Source: M. Swaminathan and K. J. Han, "Design and Modeling for 3D ICs and Interposers", WSPC, 2013

All electronic systems, no matter how large or small, need to be powered. However, the amount of power required by the system can vary from several hundred watts for a server to a few micro or nano watts for sensor nodes. This requirement determines the source of power (battery or energy harvesting), methods used to deliver power (converters, regulators and network) and management of the load (control). Hence, applications classified as high/medium power, low power, ultra-low power and ultra-ultra-low power as shown in Figure 2 will each have its own set of unique requirements for generating, distributing and managing the power delivered. With energy minimization being a key driver for industry, advanced techniques such as near threshold voltage signaling, dynamic voltage frequency scaling (DVFS), and others are being developed to manage and minimize power consumption, leading to power

delivery networks that are becoming increasingly complex. Given the vast expertise and experience at Georgia Tech in the area of power delivery for microsystems, it is our vision to create a comprehensive consortium on this topic working closely with industry, where application specific technologies in the area of power delivery can be developed and transferred to industry. With the participation of both undergraduate and graduate students in such a consortium, we believe that Georgia Tech is uniquely positioned to educate and create a workforce that would be proficient in power delivery methods and technologies for emerging electronic systems.

II. Challenges

Power delivery for any electronic system consists of a source, network and load as shown in Figure 3. AC outlets, batteries, transducers and RF signals are various methods for generating the energy at the source. This energy needs to be rectified to generate DC voltage, which in turn needs to be up or down converted, depending on the source of energy, regulated, and distributed, before it can be used by electronics. These elements when connected together along with storage components such as capacitors and inductors form the power distribution network, which collectively transfers energy to the load.

Figure 2: Classification of applications based on power requirements

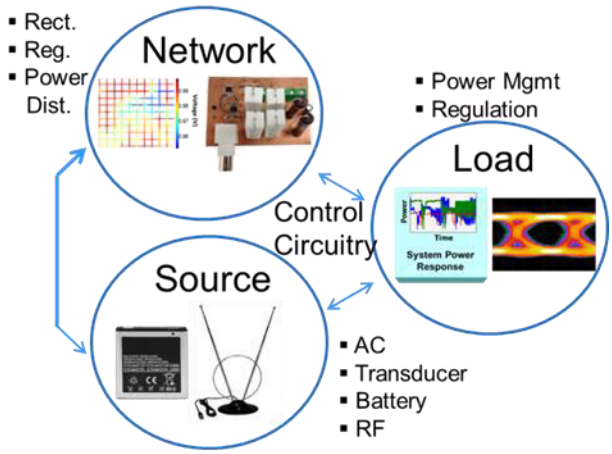

Figure 3: Constituents of a power delivery system

The interaction between the switching currents at the load and the parasitics in the network cause power supply transients that need to be regulated, which often times require decoupling capacitors. In addition, power management at the load is required to conserve and minimize the usage of energy. With miniaturization of systems over the last two decades, power delivery has become a very complex problem and this complexity

is being amplified manifold with emerging applications that require high levels of regulation at ultra-low power in a very small form factor.

With miniaturization comes strong interaction between the constituents of the power delivery system as depicted in Figure 3, where co-design of the elements becomes necessary. Some of the challenges for providing clean power to the switching circuits can be listed as follows: i) development of high speed and high efficiency integrated voltage regulators with good regulation capability, ii) integration of high density storage elements such as capacitors and inductors in the chip and package, iii) wireless power transfer in a small form factor with buck/boost converters and integrated battery, iv) development of robust power distribution networks with minimum decoupling capacitors, v) maximizing isolation between mixed signal electronics integrated together in a tiny package, vi) rectifier less energy conversion, vii) energy harvesting from far field with high efficiency, viii) micro-architectural power management methods and ix) co-design of the elements which are distributed in the chip, package and printed circuit board.

III. Thrust Areas

Georgia Tech proposes four broad thrust areas to address the power delivery challenges described earlier. The thrusts are integrated together using the test bed shown in Figure 4 which will be used for the integrated analysis of power converters, regulation, distribution and load. Hence, the impact of each developed technology within a thrust on system performance and its effect on other parts of the power delivery system can be evaluated using the test bed in Figure 4. Each thrust is described in this section

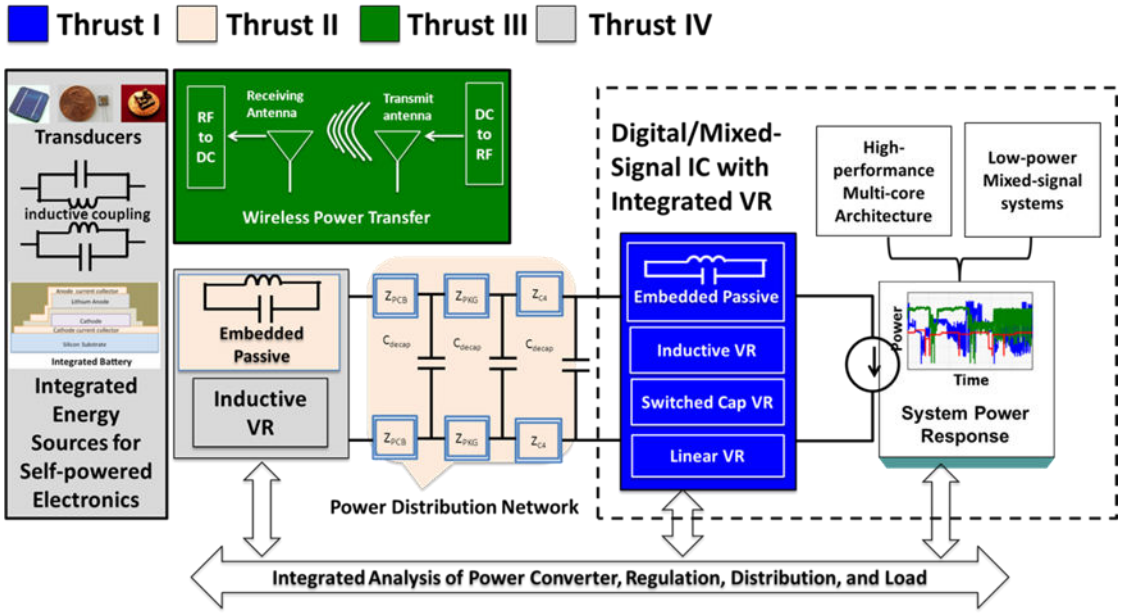

Figure 4: Integrated system test bed

Thrust 1: Integrated Voltage Regulators (IVRs)

Project scope: As the need for low-power circuits and systems continue to grow, the importance of design with low operating voltages and wide dynamic ranges has become indisputable. Increased variations, increased numbers of power states and the necessity for maximizing energy efficiency have led to fine-grained voltage domains and voltage assignments in many multi-core microprocessors and Systems-On-Chip (SoCs). This thrust will address the growing challenges associated with the design and application of IVRs for efficient power management. On-chip power delivery networks for today's systems-on-chip (SoC) characterized by dynamic supply voltage, many embedded IVRs, lower de-cap, high current ranges, multiple power modes and fast transient loads are designed to minimize AC load transients and supply noise. We will provide design solutions for inductive buck IVRs (on-package/on-die), switched capacitor (SC) IVRs (on-die) and linear IVRs (on-die) to address power "hotspots" across multiple-voltage domains and wide dynamic operation. The optimal power delivery network with intelligent placement of the different types of VRs in the hierarchy will be developed. Further, the design advantages enabled by integration of passives (e.g., high quality inductors) on package and on the die will be demonstrated. Application of such IVRs in micro-architectural design to enable more power states, faster transitions between power states and wide dynamic operation will be investigated. In this thrust we will work closely with researchers from Thrust-2 to demonstrate efficiency improvement as well as faster transient responses, which are enabled by advanced process technologies featuring embedded inductors and capacitors.

Technical Approach: The five tasks of research in this thrust are discussed below:

i) Integrated Inductive Buck VRs: Inductive buck regulators provide high-efficiency DC-DC conversion and voltage regulation, as illustrated in Figure 5. This task will develop inductive buck IVRs with integrated switching MOSFETs and on-chip/on-package passives to be integrated on the same die or on the same-package (on interposer or as a 3D die-stack) with a SoC. The core goal is to demonstrate very high frequency (>100MHz) operation of buck regulators to enable fast reference tracking and load transients (< 100ns) as well as enhance low-load efficiency of the regulators. Along with traditional pulse-width-modulation (PWM), alternative pulse-frequency-modulation (PFM) topologies will be explored to achieve the goal. To enable a scalable number of on-chip power domains with fewer inductors, single-inductor-multiple-output (SIMO) regulators augmented with linear VRs for transient management will be explored. The SIMO topologies to minimize coupling noise across voltage grids and improve power efficiency across wide operating ranges will be developed. The goal of the task will be to develop control topologies to facilitate integration with digital/mixed-signal SoCs.

ii) Switched Capacitor IVRs: Switched Capacitor VRs (SCVRs) provide faster transient response and complete integration for finer-grained DC-DC conversion, as shown in Figure 5. At target conversion ratios they can exhibit more than 90% power efficiency which has already been demonstrated through optimized designs in technologies that enable integration of high density and low ESR capacitors. We will provide design

solutions tailored to the demand of the load and process specifications required for high efficiency. Our designs will demonstrate fully programmable SCVRs with multi-conversion ratios for wide operating ranges and large load changes.

iii) Linear point-of-load (PoL) IVRs: At the very end of the IVR hierarchy we have PoL linear regulators that exhibit very fast transient response, as illustrated in Figure 5. Traditional designs, mostly analog, are typically designed for a narrow range of load conditions. Our goal in this project is to demonstrate all digital solutions which enable both process and voltage scalability. By providing novel control strategies for loop adaptation, we will provide high power efficiency across ultra-wide load current ranges. In our on-going work we have already demonstrated more than 95% current efficiency along with 100X load current ranges in fully digital linear IVRs.

iv) Embedded Passives for Efficient IVR designs: Buck converters and SCVRs whose operating principle is pivoted on switching high quality passives (inductors or capacitors) will benefit from embedding passives in the package, interposer and on the die. In this thrust we will work closely with researchers from Thrust-2 to enable the integration of high-value passives in the design of IVRs. Our goal is to develop low-cost processes for integrating capacitors with a density greater than 10μF/cm² (based on superficial surface area) that would be ideal for integrating multiple SCVRs on die.

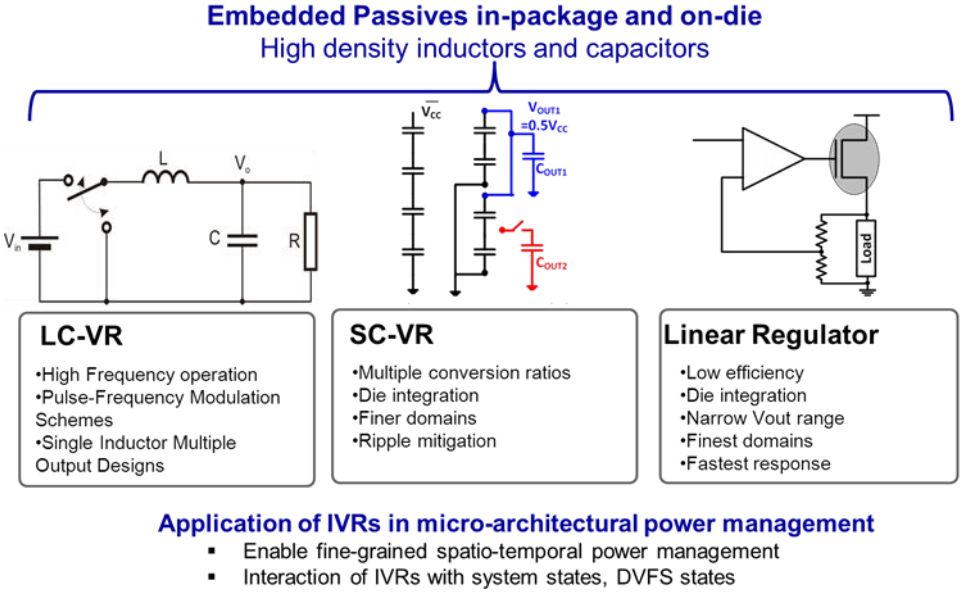

Figure 5: Hierarchical Design of IVRs illustrating dc-dc conversion and regulation with different system specifications and applications

v) Application of IVRs in micro-architecture level power management: Scaling energy-efficiency (ops/joule) will be a key enabler for performance scaling in future processors. The energy-efficiency of the processor as a whole depends on both the design of high-performance and high-efficiency IVRs and their effective application in micro-architectural level power management. This can be realized by providing design abstractions of IVRs at higher levels of the design hierarchy. Our goals are to provide a full system modeling and simulation environment wherein application binaries can

execute on cycle level model of a multicore architecture with integrated models of the power delivery system. Such explorations can be utilized by IVR designers in gaining insight into the effects of their design decisions and to optimize the integrated IVR-micro-architecture design.

Thrust 2: Power Distribution

Project scope: The focus of any power distribution network is to provide the necessary charge from the source to the load in real time. With the load constantly varying, regulating the power supply within a required tolerance level can be very challenging. With a wide range of applications all requiring unique power delivery techniques, the power distribution network is becoming very complex. This complexity is being amplified through the introduction of new technologies such as embedded inductors and capacitors, integrated voltage regulators, embedded sensors and integration of mixed signal electronics, as shown in Figure 6. The scope of this thrust is to develop new techniques and technologies in conjunction with microarchitecture level power management methods that provide for a robust power distribution network. With resonances being a major problem (Figure 6), managing and mitigating these resonances will be a focus of this thrust.

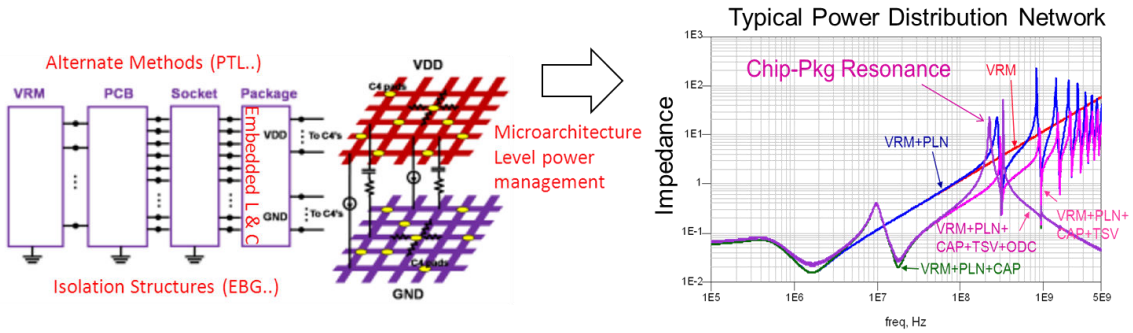

Figure 6: Emerging Power Distribution Network (left) and resonances (right)

Technical Approach: There are five tasks that have been identified in this thrust with details provided below:

i) Embedded inductors: Integrated Voltage Regulators (IVR) such as buck converters requires inductors that need to be integrated in the package. Shrinking inductor size requires new magnetic materials. Use of magnetic materials as the core can exhibit hysteresis effects. Our goal is to work closely with Thrust-1 and develop low-cost processes for the integration of inductors in the package for IVRs. A key feature of the task is to explore ferromagnetic materials with high permeability that can be used as the magnetic core and ultra-low loss insulators to increase the quality and magnitude of the inductance. The optimum permeability for the core will be decided based on the application. Our focus will be on fabricating embedded coiled inductors with minimum size using simplified processes that can be integrated with buck converters and suitably characterized.

ii) Embedded capacitors: Decoupling capacitors serve as reservoirs of charge and are often times used for noise isolation as well. In the frequency range 100MHz – 10GHz, capacitors integrated into the layers of the package provide for a good decoupling solution. Our goal is to develop low-cost processes for integrating capacitors with a density in the order of 10 $\mu F/cm^2$ (based on superficial area). A key feature of the work is to explore the formation of photodefined high aspect ratio vias within a polymeric well and use super filled copper electroplating along with high-k dielectric materials to form metal-insulator-metal capacitors.

iii) Alternate methods: Depending on the application, power can be distributed in many ways by creating a network that is optimum for that particular application. An example is the Power Transmission Line (PTL) method developed at Georgia Tech which when combined with alternate signaling techniques can be used to distribute power for applications such as DDR3, smart phones, low power ICs etc. PTL has been shown to reduce layer count, significantly reduces power supply noise and minimizes capacitor usage as well. A more standard approach is to use power and ground planes in the package and printed circuit board where the resonances can be mitigated using decoupling capacitors. Our goal is to apply the PTL method and its derivatives with suitable modifications and develop other alternate methods to deliver power that is customized to specific applications.

iv) Isolation: Mixed signal design that often times integrates digital, analog and RF circuits together require high levels of isolation between the functional blocks. For example switching noise from the digital blocks can propagate through the power/ground network causing problems. Similarly, power amplifiers can generate significant transient spurs, which may travel through the power distribution network and perturb noise-sensitive blocks, such as voltage-controlled oscillators. Our goal is to develop techniques that provide high levels of isolation between circuits that are integrated together. These solutions can be applied at the chip, package and printed circuit board level. The team has a wealth of experience in developing these strategies where EBG (electromagnetic bandgap) and PTL based solutions are some of the methods that have been developed in the past to effectively decouple, without the need for decoupling capacitors.

v) Microarchitecture level power management: Energy-efficiency of a system depends on both the losses in the power delivery and the effectiveness of power management, e.g., dynamic voltage frequency scaling (DVFS). In particular, interactions between the power management techniques and the power delivery schemes are important. Traditionally, the design of power distribution and power management has been pursued independently. Further, time-varying application workloads place unique demands on the power distribution which are impacted by the microarchitecture level power management techniques. In effect, co-exploration and co-design of power delivery and power management techniques is necessary. Our focus will be to understand tradeoffs between these two anytime a power distribution scheme is proposed and implemented. The co-design process will also include the consideration of thermal interactions which affect power delivery.

Thrust 3: Wireless Power Transfer

Project scope: Transferring power via far-field electromagnetic (EM) radiation enables a plethora of applications where wireless power transfer is necessary but the distance is beyond the reach of near-field inductive coupling. These applications include locating and charging personal electronic devices by local "wireless power hub", tracking and powering moving robots or miniaturized UAVs (Unmanned Aerial Vehicles), operating free-of-maintenance wireless sensor networks, and the fast-growing Internet-of-Thing (IoT) devices. However, conventional far-field power transfer experiences compromised efficiency compared to other power transfer approaches. The focus of this thrust is to develop new technologies to substantially enhance the power transfer efficiency via far-field radiation by 10× to 100×, as shown in Figure 7. In addition, techniques to improve the power transfer robustness (e.g., against radiation environment variations or multi-path fading) will also be explored.

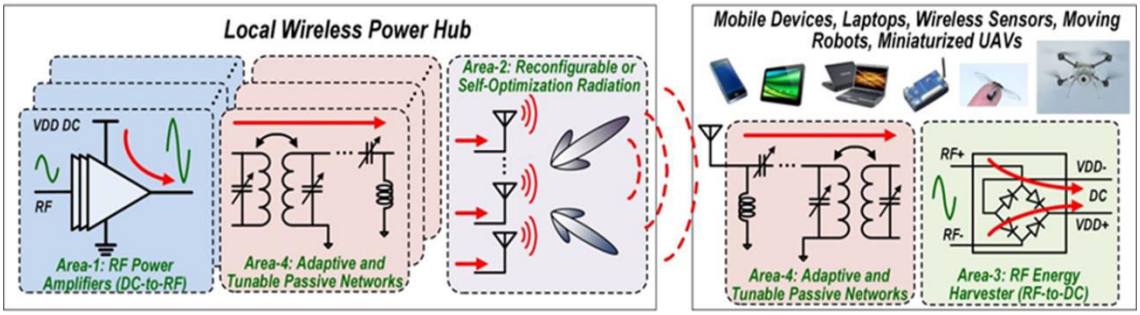

Figure 7: High-Efficiency Wireless Power Transfer

Technical Approach: There are four tasks that have been identified in this thrust with details provided below:

i) High-Efficiency, Power-Scalable, and Frequency-Agile RF Power Amplifiers (PA) for DC-to-RF Conversion: In far-field wireless power transfer, the DC power needs to be first converted to RF power through power amplifiers (PA) for radiation propagation. The DC-to-RF efficiency, i.e., PA drain efficiency, is of paramount importance for the total wireless power transfer efficiency. Moreover, watt-level RF power generation and power scalability are equally essential in order to allow dynamic power adjustment according to the mobile devices' need for energy saving. The major challenge on the power scalability aspect is to maintain a high PA drain-efficiency at deep power back-off (PBO) levels, e.g., -6dB or -12dB. In addition, it is highly desirable to employ frequency-agile, e.g., multi-band or broadband, RF PAs to explore and leverage the optimum radiation environment. This is particularly relevant when multi-path effect comes into play for indoor scenarios. We have extensive experience in watt-level high-performance RF power amplifiers. We will investigate different switching PA, transistor stacking, and power combining topologies to achieve both high power and DC-to-RF conversion efficiency. We will also explore advanced RF PA architectures to significantly boost the PA efficiency at deep PBO levels, such as Doherty, Envelope-Tracking (ET), and Class-G operation. In addition, low-loss multi-resonance passive networks will be explored to

provide frequency agility for the PAs. We will work closely with Thrust-1 to exploit co-designs between RF power amplifier and voltage regulator and their synchronized operations as well as Thrust-2 to leverage the novel high-quality passives for PA efficiency enhancement and thermal management. We will also collaborate with Thrust-2 on the chip-/package-level isolation design strategies.

ii) Reconfigurable or Self-Optimization Radiation: Once the RF power is generated, it will be radiated for far-field delivery. Unfortunately, such propagation is often the major culprit causing low efficiency in far-field power transfer, since the radiated power intensity decreases as the square of the propagation distance. Although high-gain antennas can remedy this issue, they are often highly directional and unsuitable for powering moving devices. We propose to utilize smart antenna architectures at the "local wireless power hub", e.g., phased arrays, to achieve reconfigurable beam-forming for efficiency enhancement, electronic beam-steering for directional flexibility, and concurrent multi-beam for powering multiple devices. Moreover, we will explore the possibility of extending the phased-array architectures to the mobile devices for further efficiency boost. In this case, the array should operate and be steered at minimum power consumption or even in a completely passive manner. We have a long track-record in RF/mm-wave phased-array systems, which will be leveraged here. We will collaborate with Thrust-2 to explore efficient/low-profile on-package antennas/antenna array designs as high-quality radiation structures.

iii) Efficient RF-to-DC Power Conversion: The mobile devices will receive the RF power and rectify it to DC output power, as RF-to-DC energy harvesters. The efficiency in such conversion is equivalently critical as the DC-to-RF conversion. We will leverage different high-efficiency RF rectifier topologies to ensure optimized RF-to-DC efficiency, in particular at low received RF power levels (-20dBm or below). These include multi-stage Dickson's RF rectifiers, threshold compensation techniques, and low-loss passive matching/power combining networks for RF voltage swing boosting. Research efforts in this area will also be synchronized with the work in Thrust-1. Voltage regulators and power management circuits are essentially the loads for the RF-to-DC harvesters, and co-design and co-optimization will be explored. We will further work together with Thrust-4 to optimize RF-to-DC power conversion from both architecture and design perspectives.

iv) Adaptive Techniques for Power Transfer Efficiency Enhancement: In practice, the wireless power delivery system may be subject to different variations, which affect its total delivered power and efficiency. These include radiation environment changes, typical P.V.T. variations, device aging, etc. Therefore, adaptive circuit techniques to compensate for these changes will always be necessary to ensure the robustness of the power transfer. These techniques should consume little power overhead or cause negligible power loss. We will mainly focus on the RF aspects of the adaptivity, such as low-loss tunable matching networks and antenna load tuners. In particular, we will work closely with Thrust-2 to explore on-chip or package-level tunable passive networks, which provides compact chip area, low-loss, broadband, and wide impedance tunability. These adaptive passive structures also ensure the frequency agility of the wireless power

transfer. In addition, the development in this sub-area can contribute to Thrust-4 to realize optimized and reconfigurable resonance structures to enhance near-field inductive coupling efficiency.

Thrust 4: Power Delivery Solutions for Self-Powered Internet-of-Thing Devices

Project scope: The power delivery and management for ultra-low-power Internet-of-Things (IoT) devices like wearable electronics or wireless sensor nodes poses intriguing design challenges. The devices should be self-powered from various types of, potentially co-existing, energy sources including battery, energy harvesting, or wireless transfer of power. A critical challenge is to ensure such energy-sources are compact, low-cost, and can be easily integrated within the small form factor of the IoT devices. The DC-DC and/or AC-DC conversion and regulation (power conditioning) are necessary to obtain usable voltage from these energy sources. The voltage/power levels available from the energy sources, particularly, when working with energy harvesting or power transfer, can vary over a wide range and may even be unavailable. For example, a thermoelectric energy harvester may produce ~10-15mV for 1-2^{0}C temperature difference – running RF electronics at 3.3V requires > 300X conversion. A single device will have multiple power domains with different output levels, e.g. sub-0.5V digital electronics and 3.3V RF electronics. The power consumption of the IoT devices may be widely time varying and often include burst mode of operations (i.e. long sleep/standby modes with ~μWs of power with intermittent higher activity/power modes with mWs of power). Hence, power conditioning modules should support multiple power domains; provide good efficiency at high and low power modes; have high and widely varying conversion ratio; very low bias power; and in general, require less area/cost with minimum number of passives. This thrust will address the preceding challenges associated with the design of power management solutions for ultra-low-power devices. The thrust will develop technologies in three major areas: (a) integrated energy sources; (b) integrated voltage conversion/regulation; and (c) power delivery and conditioning system with on-line management.

Technical Approach: The four tasks of research in this thrust are discussed below and illustrated in Figure 8.

Integrated Energy Sources for Self-powered IoT Devices

The projects in this area will develop new technologies for integrated energy storage and near-field wireless power transfer; and leverage existing technologies for transducers.

i) Integrated Energy Storage: We will integrate high-capacity energy storage components closer to the chip (i.e. directly on-chip or on-board). The storage technologies of interest are thin-film lithium ion batteries (very high energy and power density, but slow response time), electrolytic super capacitors, and dielectric capacitors. Ideally, these components can be co-fabricated with the silicon chip (e.g. using the backside) or co-fabricated with the printed circuit board using many of the same fabrication methods and materials as the other materials present. Also, it is our intention to integrate multiple storage components into a single storage hierarchy. For example, it is known

that a super-capacitor component can be integrated with a battery to improve the response time. So too, an on-chip or on-board dielectric capacitor for power-ground decoupling can be integrated into the storage hierarchy.

ii) Energy Transfer through Near-Field Coupling: We will develop high-frequency (~1-3 GHz) near-field resonant inductive coupling to facilitate contactless energy transfer between an IoT device and an inductive probe. To minimize the size/cost we will enable energy transfer even with low-Q on-chip inductors in the IoT and ~mm distance between an inductive probe and the device. This will be accomplished by designing a digitally controlled low-power trans-receiver in the probe and in the device to generate optimally designed high-frequency current pulses. A major goal is to develop boost converter topologies that can operate at a very high frequency to harvest without using rectifiers. The rectifier-less approach is particularly suitable where eliminating the bulky/lossy diodes can improve system size/cost. The circuits for energy transfer can be further used for near-field contactless communication.

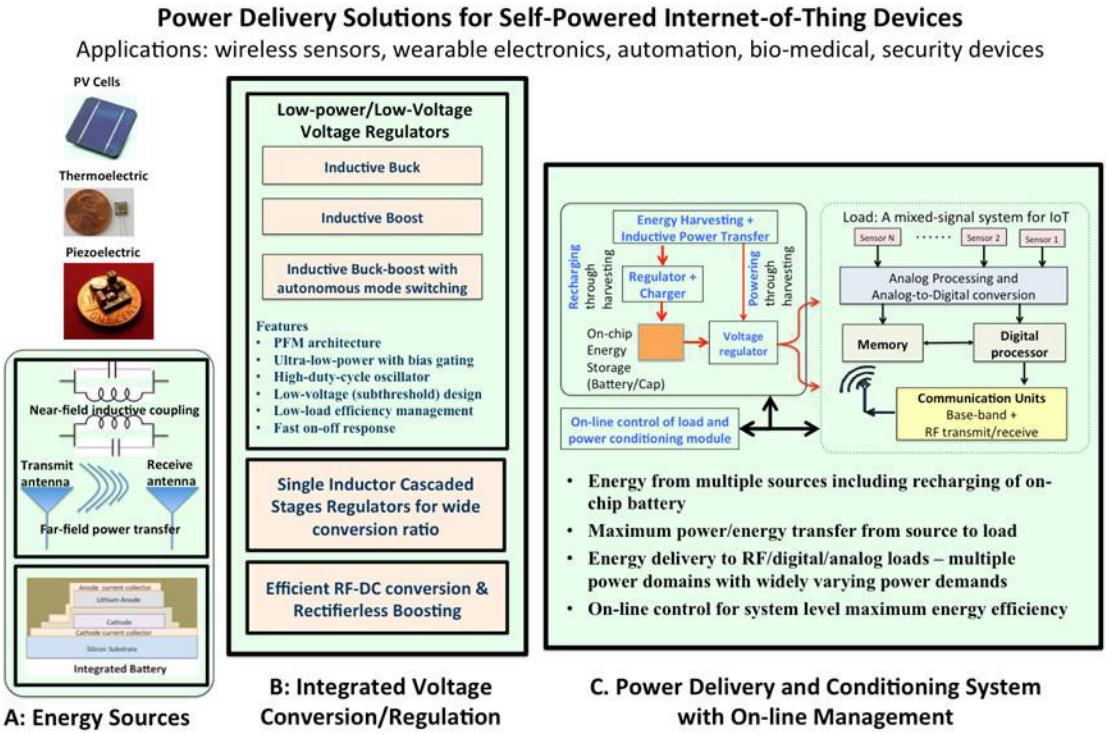

Figure 8: Power delivery solutions for Ultra-low power devices

Integrated Voltage Conversion/Regulation for IoT Devices

The projects in this area will develop innovative regulator topologies and new circuit/system techniques to address the design challenges for voltage converter/regulator for IoT devices.

iii) Low-power/Low-voltage Inductive Converters with High Conversion Ratio: Inductive boost, and buck regulators will be designed to work with extremely low bias currents, and capable of producing large (~100X) and widely varying conversion ratio. Buck-boost converters that can autonomously switch between the buck and the boost mode will be

designed to guarantee continuous functionality even with variable input. The single-inductor-multiple-output (SIMO) topologies will be explored to minimize system volume while supporting multiple power domains. We will develop mostly-digital pulse-frequency-modulation (PFM) based regulator topologies to achieve ~100s of nA bias currents. The bias gating techniques will be demonstrated for such converters. High-frequency operation of the regulators will be pursued to minimize the need for off-chip (or off-package) inductor/capacitors to reduce system volume. The control circuits will be designed to operate even at very low (sub-threshold) supply voltages to guarantee wide operating range and minimum bias power. We will design innovative high duty cycle oscillator and *single inductor scalable stage* topologies to design regulators with very large (300X or higher) conversion ratio. Autonomous efficiency management principles will optimally balance the conversion factors across stages to improve efficiency at higher conversion ratio. The converters will be designed for very fast transitions to maximize harvested energy and deal with varying power demands.

Power Delivery and Conditioning System with On-line Management

iv) This area will combine the innovations described earlier to develop the integrated power delivery and management solutions for IoT devices. We will leverage the technologies developed in Thrust-3 for IoTs powered by far-field wireless power transfer. We will develop methods to optimally integrate various energy source and storage technologies depending on the power characteristics of the IoT device. We will specifically explore a hybrid approach where the integrated battery acts as the primary source; while energy harvesting or power transfer is used to recharge the battery. The buck, boost, and buck-boost converters along with optimal power transfer techniques will be used to simultaneously harvest/obtain energy from multiple sources. The system will enable operation of multiple voltage/power domains to support mixed-signal IoT devices with wireless communication. The co-design and on-line control of the energy source, power delivery system, and the operating conditions of the RF/digital/analog load blocks will be used to most efficiently use the available energy while meeting system performance requirements. With the varying performance demands, environmental conditions, and energy availability, on-line control will optimize the conditioning as well as distribution of the energy.

Our past experience in Thrusts 1 and 2 has been in developing IVRs, power management systems and power delivery schemes for microprocessors, RF Front ends, graphics units, SoCs, FPGAs, memory controllers etc. We believe that the methodologies developed can be applied to a wide variety of applications that include smart phones, laptop computers and servers, to name a few. In Thrust-3, our technical expertise include high-efficiency watt-level RF power amplifiers, power/efficiency scalable RF/mm-wave power amplifiers, scalable and self-healing phased-array systems, active/passive beam forming networks, RF-to-DC rectifiers, tunable passive networks, and antenna load tuners. In the commercial space, these applications include locating and wirelessly charging personal electronics, e.g., mobile phones or laptops, and operating massive field-deployable sensor networks. Our technologies also align well with various defense applications, such as tracking and wirelessly powering moving

robots and miniaturized UAVs. The power management solution for ultra-low-power systems proposed in Thrust-4 is critical for the progress of mobile, wearable, and consumer electronics. The tremendous prospect of IoT devices cannot be realized without optimal design of the power management solutions that supports complex mixed-signal systems with dynamic power variations, functioning with harvested energy or integrated battery, and has stringent energy/size/cost constraints. We believe that the methodologies developed can be applied to a wide variety of wearable and IoT devices. In Thrust-4 we have demonstrated expertise in designing/integrating battery, developing inductor topologies for energy transfer, and demonstrated ultra-low-power regulator topologies suitable for mobile devices.

IV. Center for Advanced Electronics through Machine Learning (CAEML)

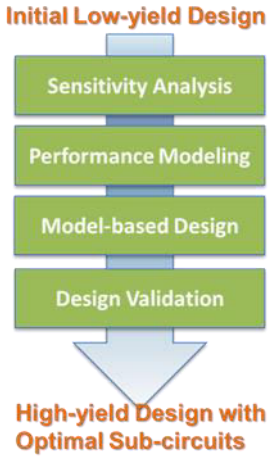

Figure 9: Application of compact models for design

Developing power delivery technologies requires modeling, which is a critical part of the design process. Often times companies may be interested in the modeling aspects where the deliverables could include modeling algorithms and methodologies that lead to the generation of compact models. The compact models can be used in a number of ways as shown in Figure 9. These companies may be interested in joining CAEML, which is an NSF Industry/University Collaborative Research Center (I/UCRC) being formed between University of Illinois, Urbana Champaign (UIUC), North Caroline State University (NCSU) and Georgia Tech. Research topics in CAEML cover the development of compact models for high speed links, chip-package co-design, system level ESD, non-linear power distribution networks, RF, mm-wave and mixed signal. For further information on CAEML please contact Madhavan Swaminathan (madhavan@ece.gatech.edu).

V. Consortium Model

The consortium will be administered by the Institute of Electronics and Nanotechnology (IEN), Georgia Tech with its research programs managed and executed by world renowned Georgia Tech faculty. Madhavan Swaminathan will be the consortium principal investigator and director. He will be supported by several other Georgia Tech faculty who will lead each technical thrust of the consortium. It is envisioned that the consortium will provide a pre-competitive research environment in which competing companies can work with faculty in a shared Intellectual Property (IP) model on basic building blocks. The duration of the consortium, and the program plans are initially anticipated to be for a six year period, organized into 2 year project blocks. A company will be asked to join the consortium for a minimum of 2 years. Renewal will occur every 2 years, thereafter. Membership fees will be due on an annual basis. In parallel, a company may be interested in a customized research project which can offer competitive and company specific research leveraging the consortium outcomes. These customized

projects costs are not included in the membership fees and will be administered via a separately negotiated research contract. It is envisioned that based on application, interest and company feedback, consortium projects will be developed that involve tasks from each thrust, as shown in Table 1.

As an example, Project 1 could involve the development of power delivery schemes for high performance computers and FPGAs which requires research in integrated inductive buck VRs, micro-architectural power management, embedded inductors and alternate methods for power distribution, as shown in Table 1. Similarly Project 2 could involve an RF application which requires energy harvesting from far field, tunable passives network, linear regulation, distribution of power and its isolation from digital logic ICs. In Table 1, Project 3 is an example of an IoT device that requires near field/far field coupling with rectifier less DC conversion which periodically charges an integrated battery with power management solutions. Definitions of such projects will be decided by the full member companies (working with faculty) who will also mentor the projects so that the project scope, deliverables and progress can be monitored to the satisfaction of all in the consortium. An Industry Advisory Board (IAB), which will meet formally twice per year, will be formed to advise the Director on project selection and progress. Progress between semi-annual meetings will be communicated via various methods including web meetings, teleconferences, e-mail, and other face-to-face meetings as deemed necessary.

Table 1: Project Definitions

Project	Thrust I					Thrust II					Thrust III				Thrust IV			
	Task 1	Task 2	Task 3	Task 4	Task 5	Task 1	Task 2	Task 3	Task 4	Task 5	Task 1	Task 2	Task 3	Task 4	Task 1	Task 2	Task 3	Task 4
1	x				x	x		x										
2			x					x	x				x	x				
3						x		x					x		x	x	x	x

❑ Project 1
- Application: High Perf/ FPGA
- Integrated inductive buck VR
- Power Management
- Embedded inductors
- Power distribution methods

❑ Project 2
- Application: RF
- Energy harvesting (far field)
- Passives Tuning
- Linear regulation
- Power Distribution
- Mixed Signal Isolation

❑ Project 3
- Application: IoT
- Near/Far field coupling
- Embedded inductors
- Rectifier less DC conversion
- Integrated battery
- Power management

VI. Membership details

As a consortium, a membership structure offering multiple levels of participation will be deployed. Each member will be asked to execute a 2 year Membership Agreement commensurate with their level of engagement; pay their dues at the beginning of each year; and asked to actively participate in the research program during their membership

cycle. Specific rights, privileges, and benefits will be defined via Bylaws and the appropriate Membership Agreement.

i. Research Program Full Membership:

As the primary membership category, companies joining as Full Research Members will enjoy non-exclusive intellectual property rights, with the potential for exclusive IP rights; the ability to actively engage in the steering and shaping of research program and projects; full access to the faculty, staff, and students involved; as well as full access to the research outcomes, including confidential patent disclosures and other publications.

ii. Research Program Supply Chain Membership:

Companies joining in this category are limited to those who have a more passive role with no IP rights; while also providing some of the needed materials, tools, or services needed to execute the projects. As such, payment can be made in both cash and in-kind materials, tools, or services. Generally, this category is for companies desiring to have their products or services included in future generation products.

Table 2: Georgia Tech Institute of Electronics and Nanotechnology

Membership Tiers, Benefits, and Costs

Key Reports, Information and Research and Participation Benefits	Research Program Full Member	Research Program Supply Chain Member
IEN Advisory Meeting Participation	Yes	Yes
Supply Process Service and Materials	Yes	Yes
Provide Equipment to be used in research	Yes	Yes
Access to GT Faculty for Consulting	Yes	Yes
Access to GT Students for Internship or Hiring	Yes	Yes
Participation/Hosting of Technical Seminars at GT	Yes	Yes
Research Program/Consortia Advisory Meeting	Yes	Yes
6 Month Updates in all Focused Projects	Yes	Yes
Monthly Program Update Webinar	Yes	Yes
Test Vehicle Information	Yes	Yes
Supply Chain Participation	Yes	Yes
Co-Invention Opportunity	Yes	Yes
Participation in Commercialization Path	Yes	Yes
Research Program Shaping and Project Steering	Yes	
Research Project/Student Mentoring	Yes	
Dispatch Engineer to Georgia Tech Campus	Yes	
Detailed Reports for Steering Programs	Yes	
Critical Feedback for Focused Research Programs	Yes	
Selected One-on-One Research Project oFocus	Yes	
Definition of Research Test Vehicle/Prototype	Yes	
Non Exclusive Royalty Free I/P Rights	Yes	
Potential for Exclusive I/P Rights	Yes	
Use of Project FIP for Exclusive Project BIP	Yes	

iii. IEN Access and Awareness Membership: (No Cost Added Benefit)

Companies who join the consortium will also receive a no-cost membership in the IEN. IEN membership will offer companies exposure to a broader set of IEN faculty and students, and their research efforts. Details of IEN can be found at: http://www.ien.gatech.edu/. Benefits for each category are outlined in Table 2.

VII. Core Faculty and Staff

The core faculty involved in the consortium is listed in Figure 10. Given the vast expertise of Georgia Tech in related fields, we will involve other faculty in specific projects based on need. Mr. Dean Sutter from IEN will be responsible for Membership Coordination and Administration while Dr. George White from Office of Industry Relations will be involved in membership recruitment and retention.

Figure 10: Core faculty and staff

VIII. Facilities

Georgia Tech has deep and long-standing experience in electronics design as well as micro and nanofabrication. Examples include silicon and compound semiconductor devices, design of silicon and non-silicon integrated circuits, micro-electromechanical systems, photovoltaic, and electronic systems packaging, as illustrated in Figure 11. Some recent developments that stem from this experience include epitaxial graphene and silicon-germanium for high-speed electronics, zinc oxide nanostructures for sensing and power generation, and nanofabricated devices for studying quantum computing and quantum interactions. In addition, there has been a growing emphasis on research

at the intersection of nanotechnology and the life sciences/biomedical (nano-bio) areas, such as bioMEMS and nanoparticle diagnostics. These research efforts are supported by strengths in such related areas as biomedicine, nanomaterials, and public policy.

Figure 11: Research areas in Electronics and Nanotechnology at Georgia Tech

This extensive activity is now further strengthened with the formation of the Institute for Electronics and Nanotechnology (IEN), a cluster of 9 research centers each topically focused on key enabling areas of electronics and nanotechnology. The 9 research centers under the IEN include Center for Compound Semiconductors (CCS), Center for MEMS and Microsystems Technologies (CMMT), Georgia Electronic Design Center (GEDC), Georgia Tech Quantum Institute (GTQI), Georgia Tech Research Institute on Microelectronics and Nanotechnology (GTRI), Interconnect Packaging Center (IPC), Epitaxial Graphene Science and Engineering Center (MRSEC), Packaging Research Center (PRC) and University Center of Excellence for Photovoltaics (UCEP). This consortium will be part of the Interconnect and Packaging Center. IEN provides not only a fabrication and facilities infrastructure that supports all of these topical centers, but also an intellectual infrastructure that supports faculty efforts in resource acquisition, discovery, innovation, and realization of relevant technologies. Finally, the IEN provides a common platform to enhance interdisciplinary interaction across all of electronics and nanotechnology, and a common intersection point for representing efforts in this area to both internal and external stakeholders.

Figure 12: Marcus Nanotechnology Building

Much of the research in electronics and nanotechnology is carried out in two key IEN facilities: the Marcus Nanotechnology Building (Figure 12) and the Joseph M. Pettit Microelectronics Research Building. The Marcus Nanotechnology Building is an innovative combination of traditional inorganic clean room space adjacent to an organic (bio) clean room. This approach not only allows important advances in both inorganic and organic applications of nanotechnology, but also exploits the physical proximity of these clean rooms to enable research at the interface between life sciences and nanotechnology, e.g., by allowing for device fabrication in one laboratory to be functionalized and characterized in the other. The Marcus and Pettit laboratories provide 30,000 square feet of cleanroom space (Figure 13) to enable IEN to serve a growing national community of users.

Figure 13: Clean room in the Marcus Building

Georgia Tech also has a start of the art design and measurement facilities that include 325GHz RF laboratories, 40Gbps digital laboratories, automatic and scan based testing for FPGAs, direct probing of ICs/packages and low

current/low power with sub nA and sub nW precision capability.

IX. Collaboration

Discussions are currently underway with Fraunhofer IZM, Berlin, Germany to make them a collaborative partner in the consortium. Details are currently being discussed.

X. Key Dates

An informational webinar on the consortium was held on Nov 19, 2014. This webinar has been recorded and is available on request. A one day workshop is planned for Mar. 2, 2015 at Georgia Tech where interested companies can participate. The workshop will be used to finalize projects including the scope, deliverables and time line. Another one day workshop is being planned for California (Bay Area) with the date still to be finalized. The consortium is expected to be launched on May 15, 2015. For further details or questions please contact us by sending email to madhavan@ece.gatech.edu, dean.sutter@ien.gatech.edu or Georgia.white@gatech.edu.