EFFICIENT POWER MANAGEMENT CIRCUITS FOR ENERGY HARVESTING APPLICATIONS

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To my parents and sisters

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APS	Active Pixel Sensor
CLC	Current Limit Comparator
CMOS	Complementary Metal-Oxide-Semiconductor
FC	Feedback Comparator
ILIM	Current Limit Threshold
IoT	Internet of Things
IREF	Reference Current
MPPT	Maximum Power Point Tracking
OSC	Oscillator
PFM	Pulse-Frequency Modulation
PWM	Pulse-Width Modulation
SIMO	Single Inductor Multiple Output
TEG	Thermoelectric Generator
TON	On time
TOFF	Off time
VBAT	Battery Voltage
VEH	Energy Harvesting Voltage
VIN	Input Voltage
VINT	Intermediate Voltage
VLX	Inductor Switching Node
VOUT	Output Voltage
VREF	Reference Voltage
ZCC	Zero Current Comparator

SUMMARY

Low power IoT devices are growing in numbers and by 2020 there will be more than 25 Billion of those in areas such as wearables, smart homes, remote surveillance, transportation and industrial systems, including many others. Many IoT electronics either will operate from stand-alone energy supply (e.g., battery) or be self-powered by harvesting from ambient energy sources or have both options. Harvesting sustainable energy from ambient environment plays significant role in extending the operation lifetime of these devices and hence, lower the maintenance cost of the system, which in turn help make them integral to simpler systems. Both for battery-powered and harvesting capable systems, efficient power delivery unit remains an essential component for maximizing energy efficiency.

The goal of this research is to investigate the challenges of energy delivery for low power electronics considering both energy harvesting as well as battery-powered conditions and to address those challenges. Different challenges of energy harvesting from low voltage energy sources based on the limitations of the sources, the type of the regulator used and the pattern of the load demands have been investigated. Different aspects of the each challenges are further investigated to seek optimized solutions for both load specific and generalized applications. A voltage boost mechanism is chosen as the primary mechanism to investigate and to addressing those challenges, befitting the need for low power applications which often rely on battery voltage or on low voltage energy harvesting sources. Additionally, a multiple output buck regulator is also discussed. The challenges analyzed include very low voltage start up issues for an inductive boost regulator, cascading of boost regulator stages, and reduction of the number of external component through reusing those. Design techniques for very high conversion ratio, bias current reduction with autonomous bias gating, battery-less cold start, component and power stage multiplexing for reconfigurable and multi-domain regulators are presented. Measurement results from several silicon prototypes are also presented.

CHAPTER 1

INTRODUCTION

With the proliferation of deeply integrated user experience through ubiquitous electronics, we now surround ourselves by countless electronic sensors, data and decisions. Our everyday lives are running smooth so long as the transition from one electronic to another remains frictionless. From smart home to advanced cars, from wearable electronic to remote monitoring, from smart communication devices to implantable chips - small scale electronics permeate our lives in almost every aspects - sometimes without our being fully aware of them. These small form factor electronics offer numerous new features including easy integrability, mobility and seamless connectivity. They also bring strong economic impact, improved health decisions and a new and better way of life.

With the benefits come the challenges of achieving those feature with as little possible housekeeping for the electronics themselves. Scientist and engineers are focusing on practical challenges including, but not limited to, how to improve the operation lifetime of these electronics, how to run them for longer time per charge cycle, how to communicate better within noisy channels and how to to uphold the privacy of the data.

In this thesis the primary focus is to explore the challenges designing efficient power delivery systems for small scale electronics. More specifically, for systems those are usually operated in stand alone condition, far from a commercial energy sources and hence rely either on battery powered operation or solely on harvested energy. Following is the organization of this dissertation.

Chapter 2 provides a detailed literature survey of the power management system innovations reported in the application areas such as, Body Area Network (BAN), Wireless Sensor Network (WSN), Internet of Things (IoT) and Remote Surveillance (RS). Upon identifying broad research objectives from the survey, several specific research goals are proposed which defines the scope of this research.

Chapter 3 provides a basic discussion on pulse-frequency modulation (PFM) based boost and buck regulator. This discussion helps to understand few basic terminologies of the regulator and offers a basic understanding of how a switching regulator works.

Chapter 4 presents a detail design of a highly skewed oscillator in the context of a PFM mode boost regulator. The conversion ratio of a boost regulator depends primarily upon the maximum possible duty cycle generation capability of the internal oscillator and hence is the determinant of how low the operating input can be. The specific design details of the oscillator is provided along with silicon results.

While the high duty cycle oscillator enables the regulator to reduce the operating input voltage; high conversion ratio comes at a price of efficiency degradation in these regulators. For low power applications, it is essential to minimize the regulator loss as much possible. One key loss component is regulator's self bias consumption, which can be critical for very low load range. To address the challenge, Chapter 5 introduces a concept of adaptive bias current shading in selective analog blocks. By identifying non-critical circuit blocks during idle mode of PFM operation, bias gating technique aims to reduce the overall self current consumption. The transistor level design details are discussed for bias gated analog circuit along with architecture level bias gating management.

To improve the efficiency further and to reduce the operating input of a boost system, cascaded architecture is explored in Chapter 6. By investigating the effect of intermediate node voltage on regulator efficiency, this chapter offers insight of system design for very high conversion ratio application or extremely low input voltage application.

Having discussed the cascaded system, emphasis is given on reducing overall system volume considering external components. While a cascaded system offers efficiency improvement for high conversion ratio applications, the increased number of external component might be an impediment for feasible application of such technique. To address this challenge, Chapter 7 discusses the design technique for inductor multiplexing. This chapter presents a complete design of a single inductor dual stage boost regulator addressing the

challenges of switch multiplexing and intermediate node management.

In Chapter 8, a single inductor multiple output power management system is presented which encompasses the learnings in the previous chapters. The combined power delivery and energy harvesting system embeds a boost regulator for low voltage energy harvesting and battery charging, a buck regulator with multiple output domains to supply different loads; all using a single inductor which is time multiplexed. An autonomous mode management system is discussed that dictates seamless mode hopping between harvesting and power delivery and ensures simultaneous and prioritized power delivery to multiple domains. The system also includes a reconfigurable CMOS image sensor that duals as an on-chip energy harvesting transducer. By combining the dual purpose sensor with the power management unit, this design offers a highly compact solution for low power integrated imaging system.

Eying towards self-powered sensors, Chapter 9 offers a brief discussion on how to reuse a single sensor for multiple purposes. Few preliminary results are presented demonstrating a CMOS active pixel sensor (APS) being used for dual purposes, capturing image and harvesting energy. Discussion on pixel design is also presented.

Chapter 10 offers few concluding remarks and a brief discussion on future research direction.

CHAPTER 2

PROBLEM STATEMENT AND GENERAL CHALLENGES

2.1 Problem Statement

The goal of this research is to investigate the challenges of designing efficient power management circuits for low voltage energy harvesting applications. Different challenges of energy harvesting from low input voltage energy sources and different aspects of efficient energy delivery for complex IoT devices are closely investigated for suitable solutions.

2.2 General Challenges of Energy Harvesting

Many of our everyday electronics remain mobile throughout the day. Mobile phones, smart watches, music players, laptop computers must run by the on-board battery. Many non-personal electronics applications e.g., remote surveillance, structure monitoring sensors, weather sensors - by dint of their application nature - too must run from independent power supplies, mostly batteries.

Batteries, or any other type of limited energy storage must be replenished as the stored energy is depleted. This fact imposes a significant constraint on the overall performance matrices of the electronics. For example, a small drone equipped with camera used for areal surveillance must return to the base before its on-board energy storage gets fully depleted. This limits the range of the drone. Similarly, weather and climate monitoring sensors placed in remote areas must be serviced for energy storage more often than any other types of maintenance even though for regulator operation the energy it uses is usually very small.

Energy autonomy, hence, is a critically sought feature for many systems. A platform that can generate or harvest its required energy from the ambient environment without manual interventions can be generally defined as an ‘energy autonomous’ system. An energy autonomous system brings new dynamics to the big picture by enabling larger operating

region, longer duration of operation and even, better performance.

Energy autonomy requires on-site energy harvesting from ambient sources. Often the ambient sources are low in energy fields and the relevant transducers can only generate a small electrical potential difference [1–8]. For example, one such transducer [8] only generates voltage in the order of 20mV to 50mV from a temperature difference of 5°C to 10°C. Although this transducer produces power in the order of 100μW which is enough for many applications, most of the electronics operate typically with 1V or higher voltage. Thus a voltage boosting system is essential to increase the voltage to a usable level. Another requirement comes from the fact the ambient sources vary in magnitude too often while the electronics requires a relatively fixed voltage to operate efficiently. Thus the requirement of a regulator which provides well regulated supply voltage remains in effect for such an energy harvesting system [9–31].

These requirements constrict the system design space in multiple dimensions. Several prior works focused on different types of challenges in energy harvesting systems. General challenges for the regulator system identified by most of the researchers are,

**** Low Voltage Operation Challenges***

**** System Start-up Challenges***

**** Power Consumption and System Efficiency Improvement Challenges***

**** Selection of Regulator Architecture Challenges***

In the following subsections we will focus on prior arts in these specific challenge areas.

2.2.1 Low Voltage Operation Challenges

Operating from low voltage remains a critical challenge area for almost all energy harvesting systems. For any regulator to operate from low voltage (i.e., high conversion ratio), the internal oscillator must be capable of generating a pulse with a high 'on-time' to 'off-time' ratio. This essentially translates to a very skewed oscillator design. Carlson et al. [28] address this challenge by designing a shift register based ring oscillator. The generated 50MHz and 50% duty cycle pulse is then passed through a frequency divider to allow a

wide range of frequency variation. The period of pulse is adjustable from 320ns to 4480ns using a 4-bit control signal. This 4-bit control produces quantization error and in worst case the oscillator take about 15 cycles to reach to steady state. This design involves a significant number of gates due to the use of ring oscillator and frequency divider. Additionally, although the maximum operating frequency is 3.1MHz, the continuous internal oscillator switching frequency of 50MHz might introduce both supply and ground noise.

2.2.2 System Start-up Challenges

Starting up is as critical as regular operation of the system. In general, start-up phenomenon can be categorized in to two types; assisted start up (with battery) and autonomous start up (battery free). In the following subsections we will summarize how the relevant issues are addressed in prior works.

Battery-less Start up: Battery free start up is a crucial system feature. It addresses both the first-ever start-up and start-up after deep discharge. In this mechanism the system starts up without any on-board energy storage, and hence provides ultimate solution for energy autonomy. The system is required to harvest initial energy from the environment to start-up, and henceforth for all operation. Several works addresses the challenges through different approaches.

Ramadass et al. [29] proposed a battery-less start up mechanism using a mechanical vibration sensor. Ambient mechanical vibration turns on a mechanical switch that shorts connects the inductor from the energy source to the ground. The vibration activated on and off states of the mechanical switch help build up current through the inductor and charge the output capacitor. Once the output builds up to 1V, the regular circuitry kick-in and the boost regulator operation normally. The authors are able to start from 35mV input voltage without battery. This system requires special mechanical switch and is only suitable for application areas where intermittent vibrational energy is available, e.g., body-worn electronics.

Jong-Pil et al. [30] demonstrated a boost system that can start-up without battery from

40mV. The system utilizes the transformer in conjunction with a negative-threshold voltage n-MOSFET to form a resonant circuit which oscillates from very low input voltage. Primary drawback of this mechanism is the use of a negative-threshold device which may not be available in a standard process technology.

Linear Technology [32] has reported a boost regulator that starts up from 20mV input voltage. A resonant oscillator is formed during low voltage start-up using internal n-MOSFET, and external capacitor and external transformer of 1:100 turn ratio. The major drawback of such a system is the use of bulky transformer that hinders the use of this solutions in tiny space and weight constrained systems.

Battery-Assisted Start up:

Both Carlson et al. [28] and Doms et al. [33] demonstrated systems those start up from 600mV. These system depends on the lowest operation of the standard circuits and is limited by the intrinsic threshold voltage (V_{TH}) of the active devices. Kadirvel et al. [34] reported a system that starts from 330mV input. By designing a three-stage ring oscillator the author were able to generate useful pulse from low voltage which in turn help build up current through the inductor. However, the oscillator produces only a 50% duty cycle pulse.

2.2.3 Power Consumption and System Efficiency Improvement Challenges

Energy harvesting systems are often deployed where energy is scarce. Hence efficient usage of energy is a vital requirement of such a system. Efforts to improve system efficiency might be targeted at different domains such as selecting the right architecture, reduction of the regulator's self usage loss, reduction of the parasitic losses associated with external/internal passive components, optimum value selection for inductor and capacitors. Many of these losses are reduced primarily through design innovation and optimization hence significant efforts have been put in these regards. Except the effect of architecture, works focusing on other design innovations are discussed here.

Gyselinckx et al. [12] reported that typical body area network (BAN) sensors consume

$\sim$100μW while operating and $\sim$6μW while in sleep/standby mode. On the other hand, for energy harvesting sources, Paradiso et al. [9] reported that it might be possible to harvest $\sim$60μW/cm^2 from thermoelectric, $\sim$4μW/cm^3 from vibrational, and $\sim$100μW/cm^2 from ambient office light. Because the load demands are comparable with the available energy, the power management systems must be capable of operating with power of $\sim$10μW or even below to achieve an operating efficiency of 90% or above. Several works have reported reasonable efficiency ranging from 40% to 92% using different design techniques [28–30, 34–37].

Lhermet et al. [35] presented a boost regulator with digital mode pulse width modulation (PWM) control scheme that consumes 70μA bias current and exhibited 50% efficiency. Almost half of the total bias current was consumed by the clock generator and the I/O pads. Richelli [36] demonstrated a hybrid boost regulator that has a charge pump stage following the inductive boost stage. The regulator starts up from 200mV and exhibits $\sim$35% efficiency.

Carlson et al. [28] has demonstrated a boost regulator designed with digital PWM mode control scheme and exhibits efficiency up to 79% and delivers peak load of 200μW. Ramadass et al. [29] proposed an energy harvesting system that boost from energy source to intermediate storage followed by a buck regulator that finally delivers the power to the load. The initial boost and the load side buck, both are designed with a comparator controlled sliding pulse width modulator scheme. Reported end to end efficiency is 58%.

Kadirvel et al. [34] presented a battery charging boost regulator system for energy harvesting application that exhibits 80% efficiency at 2x conversion ratio and 30% at 30x conversion ratio while deliver power at 3V output. The system is designed with digitally controlled pulse with modulator topology and embeds Maximum Power Point Tracking (MPPT) to maximize harvested energy and cold-start, to start without a battery. Jong-Pil et al. [30] demonstrated a boost regulator with MPPT that exhibits 61% effieincy at 6x conversion ratio while delivering output at 2V.

2.2.4 Selection of Regulator Architecture Challenges

Small scale electronics such as those used in WSN or BAN nodes usually runs on very light loads. Additionally many of these electronics also spend a significant time on standby [38–42]. Although inactive, these electronics must remain in standby mode as opposed to completely shut down, since many of the sensors/electronics might need to be unpredictable event activated. Hence, a large share of the energy is consumed in standby or idle mode and only a small portion of energy is spent on actual work getting done. For example, a remote motion/surveillance system might detect less than one event per hour, however it must be silently monitoring the environment for an event to occur. This non-typical load pattern demands a new kind of power management to optimize energy usage that provides a suitable balance between the power quality delivered to the electronics and the reduction of standby power.

In most cases, the architecture of a regulator defines the overall system efficiency for a given load current range. For a specific solution, it is hence better to perform the feasibility study based on the system's load activity pattern and range of load. Studies have shown that for a higher load range, fixed frequency operation remains largely efficient and for a lower load range, spurious frequency operation offers better overall efficiency [43–45]. Chang et al. [45] discuss that, at medium to low load range, the switching loss dominates over all other losses in switching regulators and hence, fixed frequency regulators (e.g., PWM mode) suffers from lower efficiency. Because of the variable frequency, PFM mode regulators usually operate in discontinuous conduction mode at low to medium load conditions; hence they exhibit superior efficiency at low to medium load range.

2.2.5 Summary of Literature Review and Prospects of Research

Holistic power management for efficient operation remains largely depended on the specific system architecture and the activity pattern of the load. From the existing literature survey it is found that significant efforts have been put to meet the challenges in various aspects of challenges faced in energy harvesting systems. Despite efforts, several issues are yet

to be solved. An extremely high duty cycle oscillator with easily controllable and process invariant duty cycle is yet to be proposed. Such an oscillator will help widen the operating input voltage range by allowing the regulator to operate from very low input voltage. Similarly, although PFM mode topology has emerged as a relatively optimized solution for low-power and burst-power loads, a circuit level self-consumption reduction methodology is yet to be demonstrated. Additionally, a system level solution that is capable of storing harvested power and simultaneously delivering power at multiple voltage domains with different values still remains challenging. Additionally, the challenges of reducing the number of passive components (specially, inductor and capacitor) through possible reusing, remain largely unmet.

CHAPTER 3

OPERATION PRINCIPLE OF SWITCHING REGULATOR

This chapter discusses the basic operation of inductive DC-DC switching regulators. This chapter provides a basic understanding of the boost and buck regulator. The design details are discussed in subsequent chapters.

3.1 DC-DC Regulator

DC- DC regulators are important power converters for various applications. The fundamental operating condition of these converters is that both input and output voltage levels are DC. There are various types of DC-DC converters such as inductive converter, capacitive converters and linear converter. Except linear converter, both inductive and capacitive converters can generate either higher or lower output level as compared with the input voltage. Depending on the specific demands of different applications, system designers might use a certain type of converter or the other. This research will focus on inductive regulators. Majority of the topics are related to inductive boost regulator, however buck design is also discussed in chapter 8 .

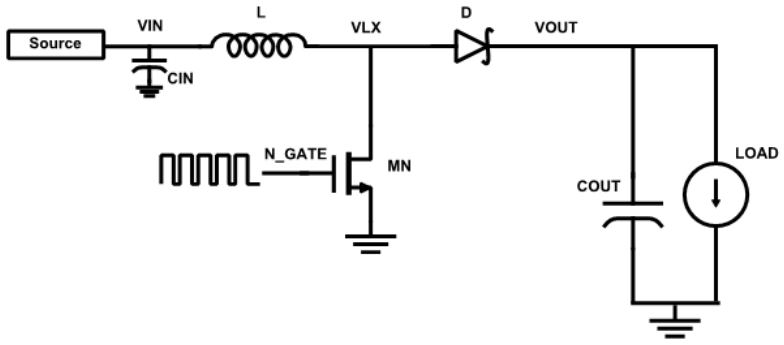


Figure 1: Basic architecture of an asynchronous boost regulator. The device MN can be replace by BJT as well. The free wheeling diode D can be replaced by another MOS device (usually P-Type) in which case the architecture will be a synchronous boost regulator.

3.2 Principle of Operation of Boost Regulator

A boost regulator generates an output voltage that is higher than the input voltage. The regulator performs the task by switching the inductor to store energy in one phase and transferring the stored energy to the output capacitor in the next phase. A feedback loop usually monitors the output voltage and keeps it regulated with varying load current and varying input voltage.

Fig. 1 shows a basic boost structure. The system consists of an inductor, a switching transistor, a freewheeling diode and an output capacitor. The gate of the device MN is controlled by the internal oscillator and controller which provides frequent pulsating signal to turn on and turn off the device. By controlling on and off time of the switch the regulator maintains a stable output voltage.

3.2.1 Boost Operation: Phase 1 - Inductor Current Charge Phase

Fig. 2 shows the first phase of boost operation. During this phase the gate of MN receives 'high' signal which turns the device on. This brings the V_{LX} close to ground potential. Hence the inductor experiences a voltage difference equal to V_{IN} across itself. This potential difference across the inductor results in an increasing current whose slope is defined by V_{IN} / L. Because the device remains on for T_{ON} duration, the final value of the current after the T_{ON} period is defined by $I_{PK} = S_p * T_{ON}$. During this time, since the V_{LX} node is connected to ground potential, while the cathode of the diode is connected to V_{OUT} (which is higher than V_{IN}), the diode is forced off. Hence there is no current path to the V_{OUT} node during this period and the output voltage discharges by the load current, which manifests as a linear drop at the V_{OUT}.

3.2.2 Boost Operation: Phase 2 - Inductor Current Discharge Phase / Boost Phase

Fig. 3 shows the second phase of boost operation. This phase starts when the device MN is turned off. Since the inductor current has already increased to a certain level during the first phase, turning off MN forces the inductor current to first charge the parasitic capacitance

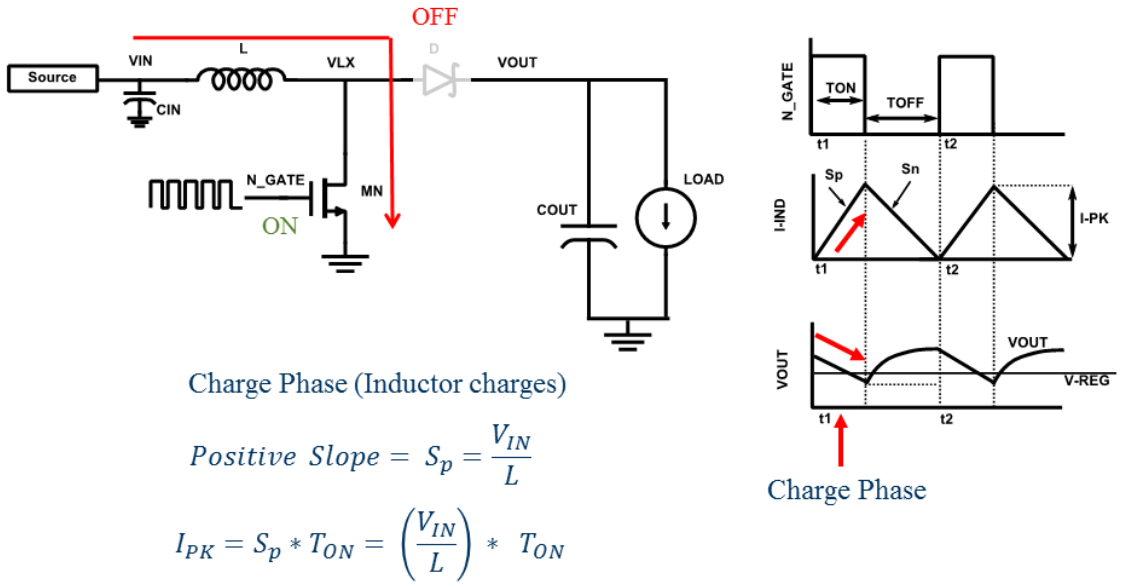


Figure 2: Boost regulator inductor current charging phase during switch ON-time (T_{ON}). The on-time is controlled by the internal oscillator and controller. At the end of on-time, the switch MN is turned off and the build up inductor current (I_{PK} is determined by both the positive slope of the indcutor current and the T_{ON}. The flow of current is shown by the arrow.

associated with the V_{LX} node, raising the voltage from ground. As soon the V_{LX} node goes higher than V_{OUT}, the diode D turns on, allowing the inductor current to charge the capacitor C_{OUT}. Since the output voltage is higher than the input voltage, the inductor experiences a negative voltage across itself and the current starts decreasing. The negative ramp of the inductor current during boost phase is proportional to the difference voltage between V_{OUT} and V_{IN} and is defined as S_n =V_{OUT}-V_{IN} / L. The time it takes for the inductor current to reach to zero is expressed as T_{OFF} and is defined by I_{PK} / S_n. The output voltage receives charge from the inductor during this phase and goes up, producing a ripple at the V_{OUT} node. Once the inductor current reaches zero, the switch turns on again to repeat the process and thereby regulates a steady output.

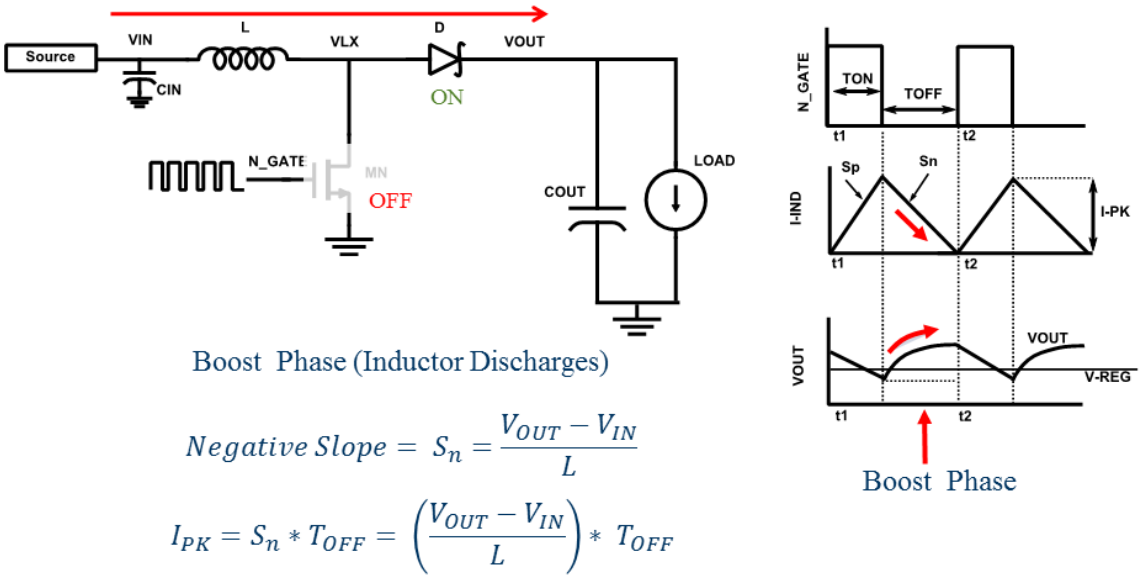


Figure 3: Boost regulator inductor current discharging phase during switch OFF-time (T_{OFF}); this phase is also known as 'boost phase', since during this phase the output voltage is boosted. The off-time is either controlled by the internal oscillator and controller or by the zero crossing detection of the inductor current. At the end of off-time, the switch MN may be turned on again to repeat the whole process. The inductor (I_{PK} discharge time is is determined by the negative slope of the inductor current. The flow of current is shown by the arrow.

3.3 Principle of Operation of Buck Regulator

Fig. 4 shows an asynchronous buck regulator. Switch MP is controlled by the internal oscillator and controller and connects the input to the inductor and disconnects the input in two phases. The diode D provides a freewheeling path for the current during discharge phase. This diode can be replaced by an N-channel MOS device in which case the regulator is called synchronous. The inductor and the capacitor forms the output filtering. The voltage regulation with dynamic load input is achieved by a feedback loop which monitors the the output voltage and controls the T_{ON}, T_{OFF} and the level of inductor DC current.

3.3.1 Buck Operation: Phase 1 - Inductor Current Charge Phase

At the beginning of the buck regulation, the switch MP is tunned on by providing ground potential at the gate of the device. The switch essentially connects teh node V_{LX} to the input which turns of the diode D. The inductor experiences a voltage difference across itself that

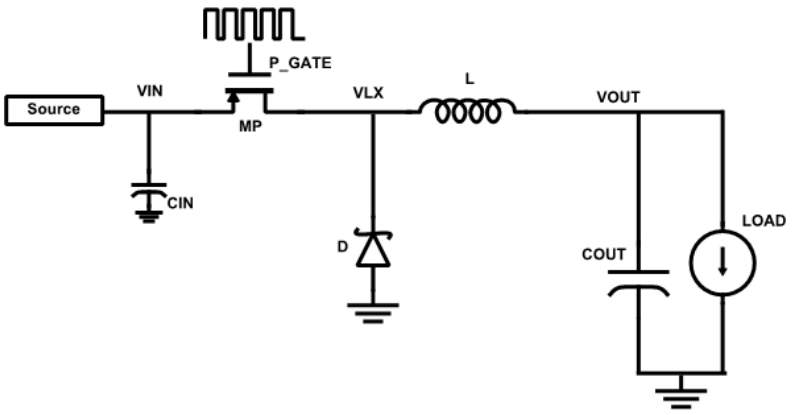
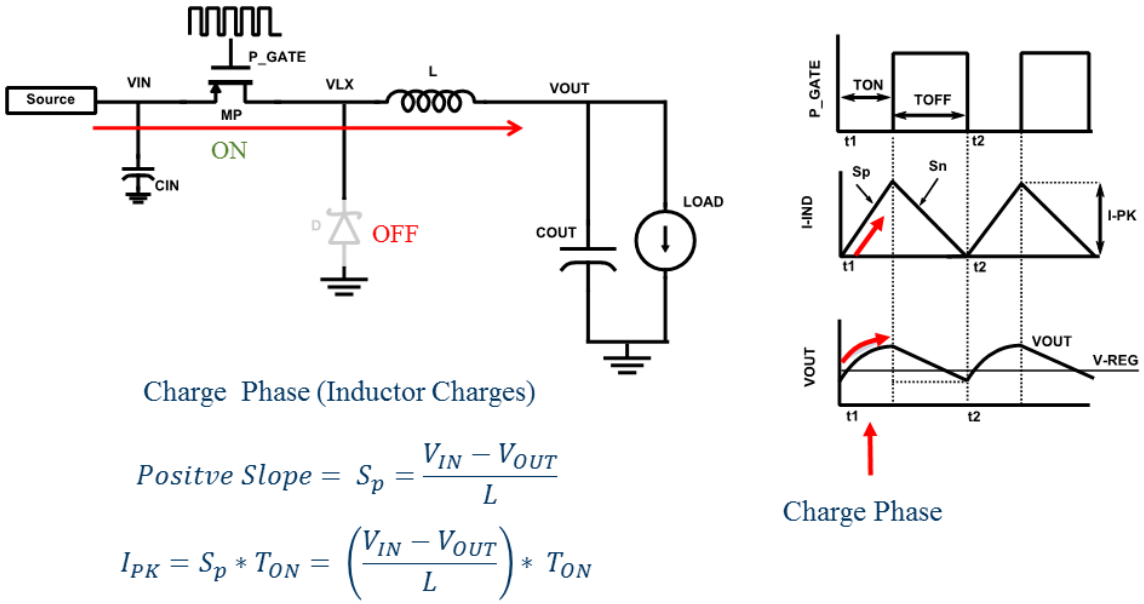


Figure 4: Basic components of an asynchronous buck regulator

equals to V_{IN}-V_{OUT}. Consequentially, the inductor current increases with the the positive slope S_p = (V_{IN}-V_{OUT})/L and the output capacitor charges. This is shown in Fig. 5. The inductor current reaches a value IPK that is defined by S_p * T_{ON}.

3.3.2 Buck Operation: Phase 2 - Inductor current discharge phase

The second phase starts when T_{ON} expires; immediately succeeding phase 1. As T_{ON} expires, MOSFET MP turns off and the V_{LX} node is pulled towards grounds due the current through the inductor. As the V_{LX} node drops below ground, diode D turns on and forms a current loop as shown in Fig. 6. During this time, the inductor current starts to decrease. The negative slope (Sn) fo the inductor current is defined by V_{OUT}/L. Because there is no active charging, the output capacitor discharges depending on the load current. The current I_{PK} reaches to zero after T_{OFF} which is defined by I_{PK}/S_n. As soon as the inductor current reaches zero, the system starts another T_{ON} phase and the process repeats itself.

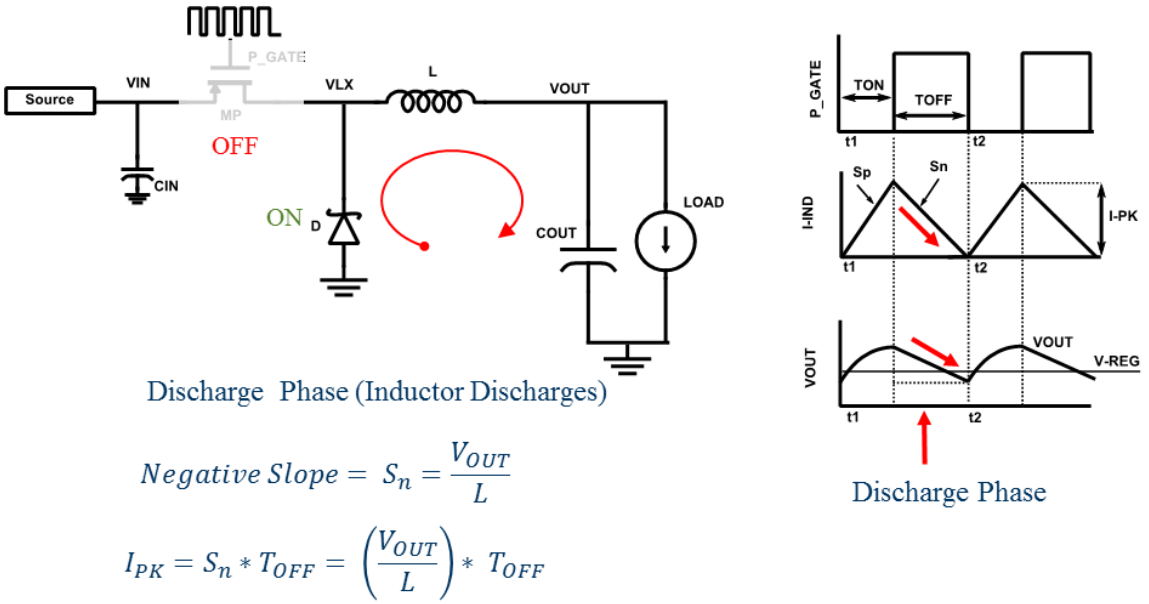


Charge Phase (Inductor Charges)

$$Positve\ Slope = S_p = \frac{V_{IN} - V_{OUT}}{L}$$

$$I_{PK} = S_p * T_{ON} = \left(\frac{V_{IN} - V_{OUT}}{L}\right) * T_{ON}$$

Figure 5: Buck operation phase 1 - inductor current charging phase. MP is on, D is off and the inductor current ramps up. The output capacitor charges as well.



Discharge Phase (Inductor Discharges)

$$Negative\ Slope = S_n = \frac{V_{OUT}}{L}$$

$$I_{PK} = S_n * T_{OFF} = \left(\frac{V_{OUT}}{L}\right) * T_{OFF}$$

Figure 6: Buck operation phase 2 - inductor current discharge phase. MP is off, the inductor current loops through D which is forced to turned on. The output capacitor discharges in this phase.

CHAPTER 4

BOOST REGULATOR WITH HIGH CONVERSION RATIO

This chapter discusses the analysis and design of the high duty cycle oscillator. The design is implemented in a a Pulse-Frequency Modulaton (PFM) mode boost regulator that demonstrates harvesting from less than 20mV input sources. Design details of the oscillator and the regulator are presented along with silicon results.

4.1 Introduction

Energy harvesting from ambient environmental signals have become critical with the advent of wireless sensor networks, body area network and other low power consuming, autonomous electronic applications. Many environmental transducers produce significant potential difference and power from ambient sources like body temperature or indoor light [2,3,8,21,46]. Some transducers, e.g., thermoelectric generator (eTEG) reported in [8] can produce ~100W output power at ~10-15mV output voltage from less than 2C temperature difference. This range of power (10μW-100μW) can enable appreciable analog/digital functionality to meet power demands of the sensor nodes. To exploit the full potential of these low voltage transducers, the power converters should be capable of generating a usable voltage levels from very low (sub-20mV) input voltage. The converters also need to be capable of wide input range because of the transducers output might vary widely. Moreover, since advanced digital circuits are designed with dynamic supply variation to minimize energy/power dissipation; the converters are required to support a wide range of output voltage as well. Finally, low standby current is essential for efficient power conversion, particularly at low load conditions. Different methods of energy conditioning from ambient sources have been explored in several prior works [28–30, 34–37, 47, 48]. For some autonomous converters the minimum input are higher in the range of 200mV to 300mV [34,36,47] or set by the lowest self-start voltage determined by the required special

devices like mechanical switch [29] or transformers and negative-VTH FETs [30]. Another reported converter achieves close to 100mV input range but consumes stand-by current in the order of 100A, making it unsuitable for extreme low voltage (sub-20mV) operation both for extremely low input range and the limitation of current and power delivery capability of the transducers. One recent work [28] demonstrates minimum input voltage of 20mV through the use of a complex digital oscillator that provides an effective maximum conversion ratio of 50:1 but it also limits the minimum conversion ratio to 4:1 preventing boost operation with higher input voltages. This chapter presents a boost regulator to address the challenge of wide input range operation and achieve sub-20mV minimum input voltage. The key contribution of the chapter is the design of a current based analog oscillator that achieves high duty cycle, enabling boost conversion ratio of up to 63:1. Instead of controlling the duty cycle by complex digital method, we propose a symmetric analog circuit pair in which matched capacitors are charged by constant current ensuring fixed duty cycle over wide bias voltage and temperature range. The oscillator design puts no lower limit on the conversion ratio. The high duty cycle oscillator is integrated with the reference generator and comparator circuits designed to operate down to subthreshold voltage to design this pulse frequency modulation (PFM) boost regulator. The PFM architecture is employed to ensure higher efficiency at lower load condition to make the converter suitable for low power energy harvesting [43–45].The low-threshold voltages transistors and subthreshold analog design methods including reducing transistor stacking are utilized to ensure all control blocksthe oscillator, the reference generator, and the comparators can start operating at very low (subthreshold) supply voltages. This allows the converters to start autonomously (i.e. without using any battery, special devices, or non-electronic components) at a very low output voltage. A test-chip is designed in 130nm CMOS to verify the operation of the regulator. The oscillator demonstrates a maximum duty-cycle of 98.4% (enabling conversion ratio of 63:1) and the analog control circuits demonstrate functionality down to 305mV. The chip regulates output from as low as 12mV input, starts up autonomously with

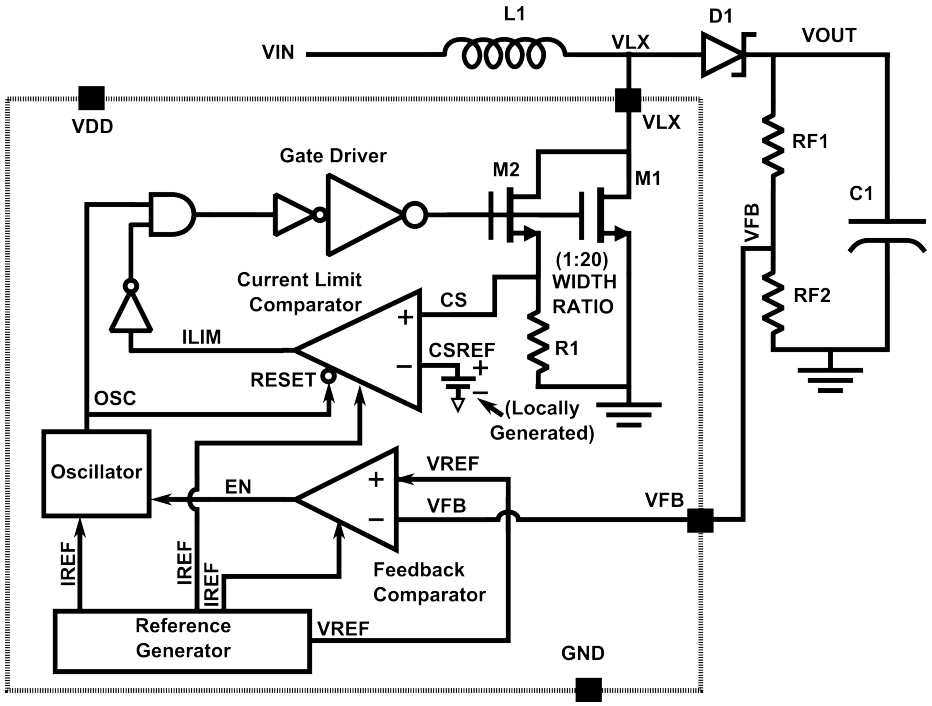


Figure 7: Functional block diagram of the proposed PFM boost regulator. Shaded boundary represents the proposed chip. External components, shown outside the shaded line, are required for the operation of the regulator.

305mV bias at the output, and demonstrate an output regulation range from 0.6V to 3.3V. The design achieves bias current consumption of 3.5μA and a peak efficiency of 82%.

4.2 Architecture and Circuit Description

Fig. 7 shows the functional block diagram of the PFM boost regulator, designed with hysteresis mode voltage feedback mechanism (also known as bang-bang control). The feedback signal monitors the output voltage and compares it with the internally generated reference voltage. The output of the feedback comparator remains low when the V_{FB} signal is higher than the V_{REF}; a condition that happens when output is above the regulation level. In this condition, the oscillator and the current limit comparator remain off and the output discharges under the given load condition. Once the decreasing output voltage crosses the regulation level, V_{FB} signal falls below the V_{REF} signal and the feedback comparators output becomes high. This turns on the oscillator which produces pulse train as long as the

EN remains high (i.e., V_{FB} remains lower than V_{REF}). The integrated n-MOS transistor is turned on by the positive edge of OSC and turned off either by the negative edge of the OSC or by the current limit signal (ILIM), whichever occurs earlier within OSCs single time period. The feedback comparator is designed with 15mV hysteresis on the upper side.

The conceptual waveforms of the converter with different input voltage and load current conditions are shown in Fig. 8. Fig. 8a shows a typical condition with load, IL1 and input voltage, VIN1, for which the converter is running at single pulse operation. At each switching event, given the input, the inductor current is increases to I_{PK} (= V_{IN1}/L_{IN} T_{ON}) and that produces an output voltage increase of V_{RIPPLE}. The V_{RIPPLE} being more than the V_{HYS}, the feedback comparator turns off the oscillator (EN goes low), before starting the next pulse and forces the converter into idle mode. The no-switching mode is defined by the section of idle mode when the inductor current has reached zero and output discharges under given load, I_{L1}. The average of the inductor current during T_{BOOST} period is equal to the load current I_{L1}. Fig. 8b represents operation with decreased input voltage, V_{IN2} (V_{IN2}<V_{IN1}), as compared to Fig. 8a. The peak current is lower and the V_{RIPPLE} decreases too. Consequently, the idle time is reduced and switching events happen more often, as shown in Fig. 8b. Fig. 8c shows the operation with increased load as compared to Fig. 8a. The inductor peak current remains same as Fig. 8a, but to compensate for higher load current the converter reduces the idle time. Note that both with conversion ratio increment (input voltage decrease) and load current increment, the converter exhibits more frequent switching. In both cases load and input variation is compensated by modulating only the idle time. The converter switches to multi pulse operation (Fig. 8d) at higher load as a single pulse cannot provide enough charge to recover the output. In multi pulse mode, for every active period, the oscillator is turned on for longer duration to allow multiple cycles. The inductor current builds up at every T_{ON} and decrease only a little during the T_{OFF} (because T_{ON} to T_{OFF} ratio is very high). At every successive pulse, output voltage continues to increase. Once the output voltage crosses the hysteresis value above the regulation level,

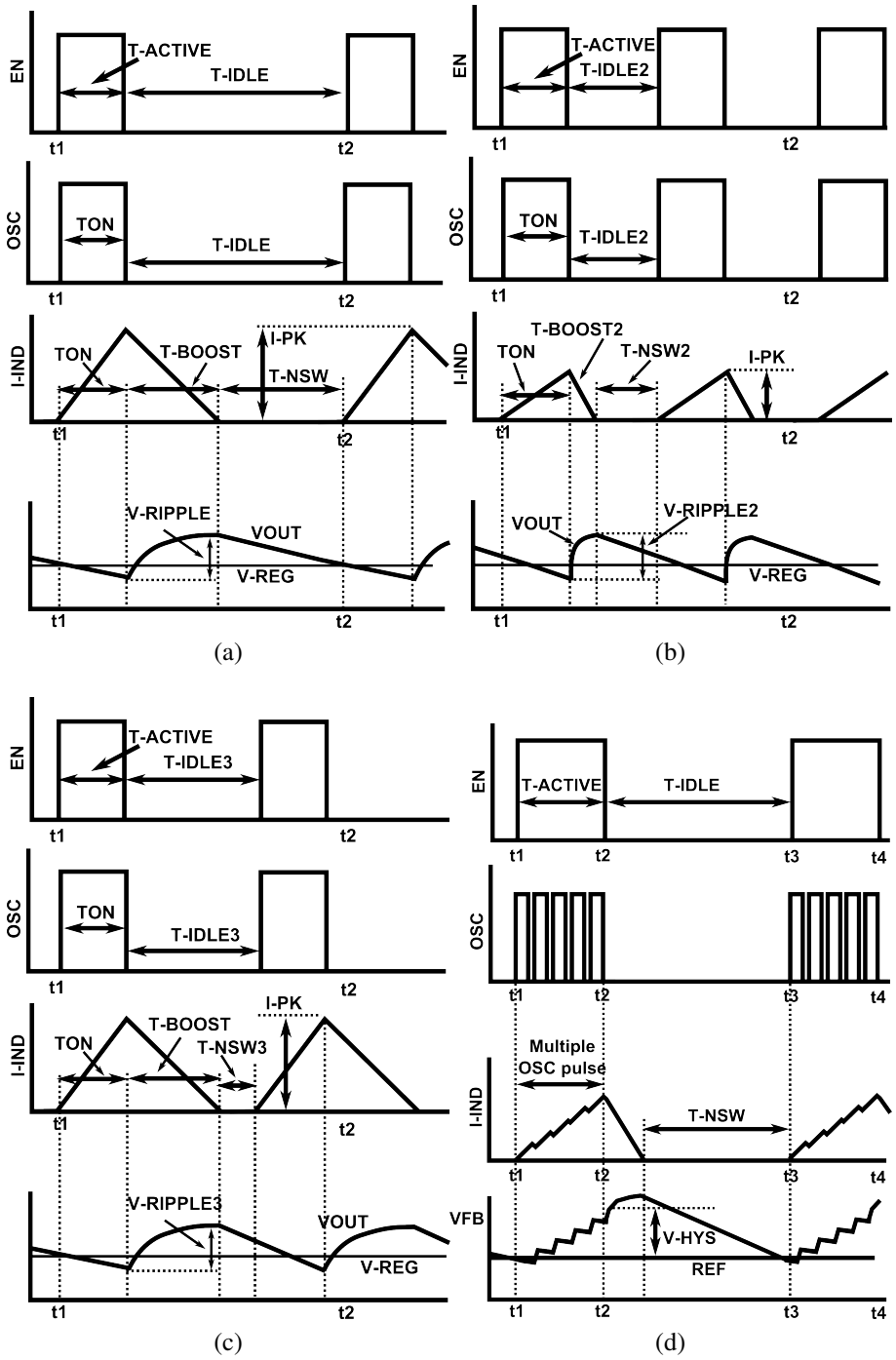


Figure 8: Conceptual waveform of the PFM mode converter. (a) Typical single pulse operation. (b) Single pulse operation with decreased input voltage as compared to situation shown in (a). (c) Single pulse operation with increased load as compared to the condition shown in (a). (d) Multi pulse operation, when the converters idle time is exhausted due to increased load or conversion ratio or for both, the converter switches for multiple pulses at every active period. T_{NSW} represents the time of no switching events. Total idle time is the sum of the T_{BOOST} and T_{NSW}.

the converter switches to idle mode. Note that unlike the single pulse operation, the ripple voltage in this condition is defined primarily by the hysteresis value, not by the inductor peak current. In practice, the ripple magnitude in this condition is little more than the hysteresis value, because after the converter switches to idle mode, the remaining inductor current charges the output voltage little more than the level where the decision was taken. On the contrary, the ripple magnitudes in the single pulse cases are defined by the value of the peak current, and can be much higher than the hysteresis value.

The converter regulates its output voltage by modulating the frequency of the switching events. By controlling both the active and idle time, the feedback comparator (EN pulse) modulates the architectural duty cycle [$T_{ACTIVE}/(T_{ACTIVE}+T_{IDLE})$] in response to changes in V_{IN} and I_{LOAD}. However, oscillator's self duty cycle [T_{ON}/T_{OSC}, where, T_{OSC} is the period of the oscillator] remains constant under all input and load conditions. It is critical to have as high duty cycle as possible to achieve higher conversion ratio. A lower input voltage demands a smaller idle time (Fig. 8b) and the minimum idle time is the off period ($T_{OFF}=T_{OSC}-T_{ON}$) of the oscillator. Therefore, maximizing T_{ON}/T_{OSC} helps reduce the minimum input voltage for operation. Further, note that variation in the duty cycle needs to be minimized (T_{OSC} and T_{ON} can vary but the ratio needs to be constant) to ensure constant maximum conversion ratio under voltage/temperature variation. In summary, oscillator with a high and well-controlled (voltage/temperature invariant) duty cycle is necessary for high conversion ratio PFM mode voltage regulator. This chapter presents an oscillator with $> 98\%$ duty cycle to enable boost operation from very low input voltage.

4.3 Analysis and Design of the Oscillator

For boost regulator, maximum ratio of the output voltage to the input voltage is determined by the internal oscillator's capability of producing maximum possible duty cycle. To produce a typically working voltage level of 1V from 20mV, a duty ratio of 50:1 or more is required, which translates to 98% duty cycle. In this work, a process invariant high duty

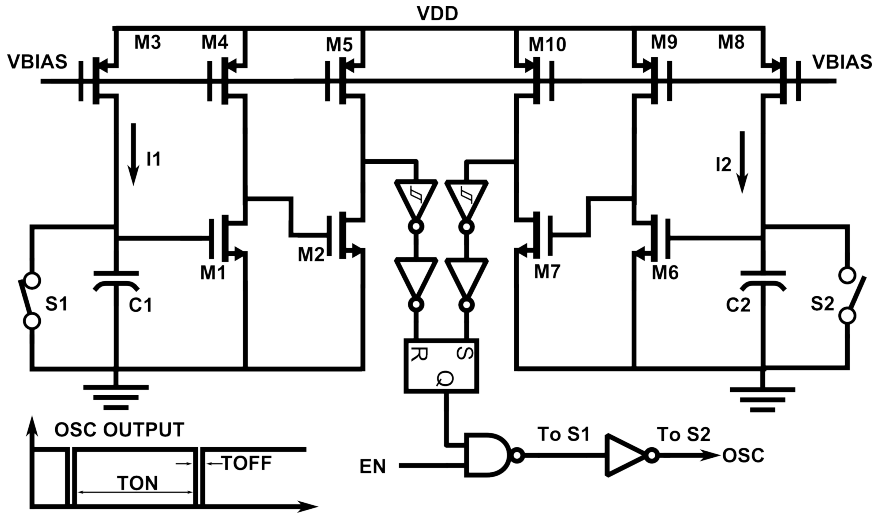


Figure 9: Schematic of the oscillator circuit.

cycle generation mechanism is presented. The high duty cycle is demonstrated using a boost regulator to harvest from very low input voltage.

The circuit schematic of the proposed oscillator is shown in Fig. 9. The oscillator utilizes on-chip capacitors and internally generated current to produce high duty cycle binary pulse. The ON-time and the OFF-time (T_{ON} and T_{OFF}) are produced by two symmetric, n-MOS threshold based comparators differing only in capacitor values (C_1 and C_2) and charging currents (I_1 and I_2 by means of widths of M_3 and M_8). Switches S_1 and S_2 are complementary current bypass paths to reset the capacitors at the end of the respective periods. At the beginning of T_{OFF} (signal OSC is low), S_2 opens allowing the current $I_2$to charge C_2, whose voltage rises linearly. Once the capacitor voltage crosses the threshold of M_6, it pulls down the drain node which in turn generates a positive edge at 'S' input of the latch. This changes the states of OSC from low to high and marking the end of T_{OFF} and the beginning of T_{ON} phase. At the same time, switch S_2closes, resetting the capacitor C_2 and switch S_1 opens initiating the charging of C_1. Similarly, when the increasing voltage of C_1crosses the M_1 threshold, a positive edge is generated at 'R' input and marking the end of T_{ON}, and also the beginning of the next T_{OFF} period. The ratio of I_1/C_1 to I_2/C_2 determines the ratio of high time to low time. In this design, the $I_1/I_2 = 10$(designed by

controlling widths of M3 and M8) and $C_1/C_2 = 7$, resulting a theoretical T_{ON}/T_{OFF} ratio of 70. However, in practice this ratio will change due to parasitic capacitances and threshold offsets. The discrepancies will be discussed further in the result section. The output of the oscillator is masked by the output of the feedback comparator (EN); OSC remains low when EN is low, and when EN is high, the output switches between high and low (regular operation).

The proposed design helps achieve the wide input voltage range in the following ways. First, with a battery assisted start-up, the key concern for low input voltage is the maximum possible conversion ratio and hence, the duty cycle. The oscillator circuit is designed with mirrored current and matched capacitor helps achieve extremely skewed, yet stable duty cycle of 98.4%, which enables the converter to achieve very high output to input conversion ratio. The ratio-metric design eliminates process, temperature and other systematic variation from affecting the duty cycle. Although the frequency changes across temperature or bias voltage, the duty cycle which is defined by the ratio of $T_{ON}/(T_{OFF}+T_{ON})$ remains constant which in turn ensures maximum achievable conversion ratio at all conditions.
The invariance of the duty cycle against variation can be derived as follows. The off-time and on-time are defined by the following equation,

$$T_{OFF} = \frac{C_1}{I_1} V_{TH1} \tag{1}$$

$$T_{ON} = \frac{C_2}{I_2} V_{TH6} \tag{2}$$

Where, V_{TH1} and V_{TH6} are the threshold voltages for devices M_1 and M_6.C_1, C_2 I_1, I_2, are the capacitors and charging current as shown in the Fig. 4. The oscillation period is then,

$$T_P = T_{OFF} + T_{ON} = \frac{C_1}{I_1} V_{TH1} + \frac{C_2}{I_2} V_{TH6} \tag{3}$$

Since device M_1 and $M_6$are identical, we can define$V_{TH1} = V_{TH6} = V_{TH}$, resulting

$$T_P = \left(\frac{C_1}{I_1} + \frac{C_2}{I_2}\right) V_{TH} \tag{4}$$

Now duty ratio (duty cycle) is the ratio of the on-time to the period, which is expressed by the following equation,

$$D = \frac{T_{ON}}{T_P} = \frac{\left(\frac{C_2}{I_2}\right) V_{TH}}{\left(\frac{C_1}{I_1} + \frac{C_2}{I_2}\right) V_{TH}} = \frac{1}{\left(1 + \frac{I_2}{I_1}\frac{C_1}{C_2}\right)} \tag{5}$$

From equation (5) it is evident that the duty ratio is solely defined by the ratio of the capacitors and the charging current. Because the capacitors remains discharged before the beginning of the charging phase, the current setting devices (M3, M8) always start with full supply rain (V_{SD_MAX}=V_{DD}− V_{SS}) as their source to drain voltage (V_{SD}). As the voltage across the capacitor increases, the V_{SD} across the transistors decrease. At the trip point, where V_{SD} is minimum, it is expressed by as V_{SD_MIN} = |V_{DD}-V_{THN} |. The biasing voltage (V_{BIAS}) is designed such that the transistors operate in the saturation even with this value (V_{SD_MIN}). Hence for the entire charging phase, both the transistor M3 and M8 remain in saturation. The saturation currents I_1 and I_2 through the transistors M3 and M8, are defined as:

$$I_1 = \left(\frac{1}{2}\right) C_{ox} \left(\frac{W_{M3}}{L}\right) (V_{DD} - V_{bias} - V_{THM3})^2 \tag{6}$$

$$I_2 = \left(\frac{1}{2}\right) C_{ox} \left(\frac{W_{M8}}{L}\right) (V_{DD} - V_{bias} - V_{THM8})^2 \tag{7}$$

Therefore, the current ratio is obtained by:

$$\frac{I_1}{I_2} = \left(\frac{W_{M3}}{W_{M8}}\right) \frac{(V_{DD} - V_{bias} - V_{THM3})^2}{(V_{DD} - V_{bias} - V_{THM8})^2} = \left(\frac{W_{M3}}{W_{M8}}\right) assuming V_{THM3} = V_{THM8} \tag{8}$$

where, V_{THM3} and V_{THM8} are the threshold voltages of the transistors M_3 and M_8, respectively; and W_{M3} and W_{M8} are widths of the transistors M_3 and M_8, respectively. The above analysis shows that the I_1/I_2 is independent of V_{DD} and V_{BIAS}. The variation in temperature and V_{DD} will result in variation in the V_{BIAS} as determined by the reference generator circuit (Section 4.4.1), however, we observe that the I_1/I_2 remains constant even with variation in V_{BIAS}. This ensures that the duty cycle remains fixed even under variation in V_{DD} and temperature. It is important to consider the scenario when the V_{DD} is reduced below the threshold. With reduced V_{DD}, the current setting transistors might be pushed

to sub-threshold region (i.e. $V_{DD} - V_{BIAS} < V_{TH}$). In sub-threshold region, I_1 and I_2 are defined as (assuming $V_{DS} > 100$ mV):

$$I_1 = I_0 \left(\frac{W_{M3}}{L}\right) e^{\left(\frac{V_{DD}-V_{bias}-V_{THM3}}{nkT/q}\right)} \tag{9}$$

$$I_2 = I_0 \left(\frac{W_{M8}}{L}\right) e^{\left(\frac{V_{DD}-V_{bias}-V_{THM8}}{nkT/q}\right)} \tag{10}$$

Where n and I_0 are process dependent device parameters. Hence, the current ratio simplifies to:

$$\frac{I_1}{I_2} = \left(\frac{W_{M3}}{W_{M8}}\right) \tag{11}$$

for subthreshold condition and the above conclusion holds true even for subthreshold operating region as well.

In summary, the maximum duty cycle of the oscillator is designed by deciding I_1/I_2 and C_1/C_2. The following equation defines the oscillator frequency,

$$f_{osc} = \frac{1}{\left(\frac{C_1}{I_1} + \frac{C_2}{I_2}\right) V_{TH}} \tag{12}$$

During operation of the booster, the maximum oscillation frequency, defined in equation (12) varies with V_{DD} and temperature as I_1, I_2, and V_{TH}, are functions of V_{DD} and temperature. The change is frequency may result in marginal degradation of efficiency with increasing temperature, however, does not impact the functionality and conversion ratio. *The duty cycle of the oscillator is well controlled and is invariant to the changes in V_{DD} and temperature*. It is important to note that the oscillator's duty cycle determines the maximum conversion ratio of the booster. In maximum conversion ratio condition, the converter runs in 100% active mode, i.e., EN remains high for the whole duration. The less than maximum conversion ratios of the booster are not determined by the oscillator's maximum duty cycle. In these cases, the converter either operates in single pulse mode or in multi pulse mode depending on the load current and the desired conversion ratio as discussed earlier.

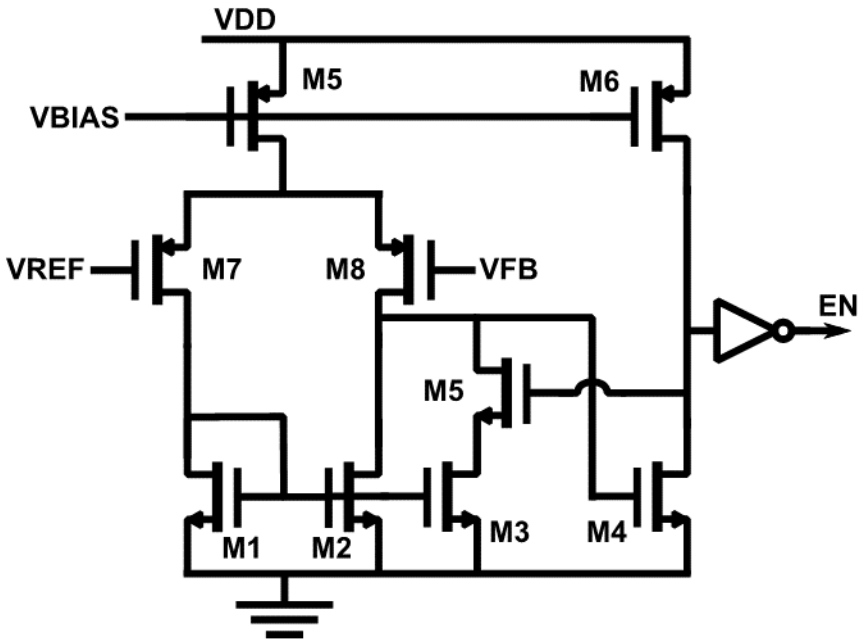


Figure 10: Feedback comparator circuit. M3 and M5 produce hysteresis.

Second, for low-voltage autonomous start-up the oscillator needs to start oscillating at a very small V_{DD}. In the proposed design, the oscillation is enabled by the bias currents (unlike a digital oscillator where oscillation is enabled by V_{DD}). As soon as the bias voltage (V_{BIAS}) and hence, the bias current is ready the oscillator starts oscillating. Although the frequency of oscillation is very low at lower V_{DD} (in bootstrap configuration, V_{DD} is connected to V_{OUT} and is essentially ˜50mV less than the input voltage, due to schottky diode drop) voltages, it still turns the power FET on and off and ensures the output voltage build up even from moderately low input voltage level. Three essential blocks necessary at startup condition, i.e., reference generator feedback comparator and oscillator, are designed without any cascoding devices. This low stacking design allows these circuits to operate from deep subthreshold bias levels and ultimately enables the chip to start autonomously at moderately low input voltage.

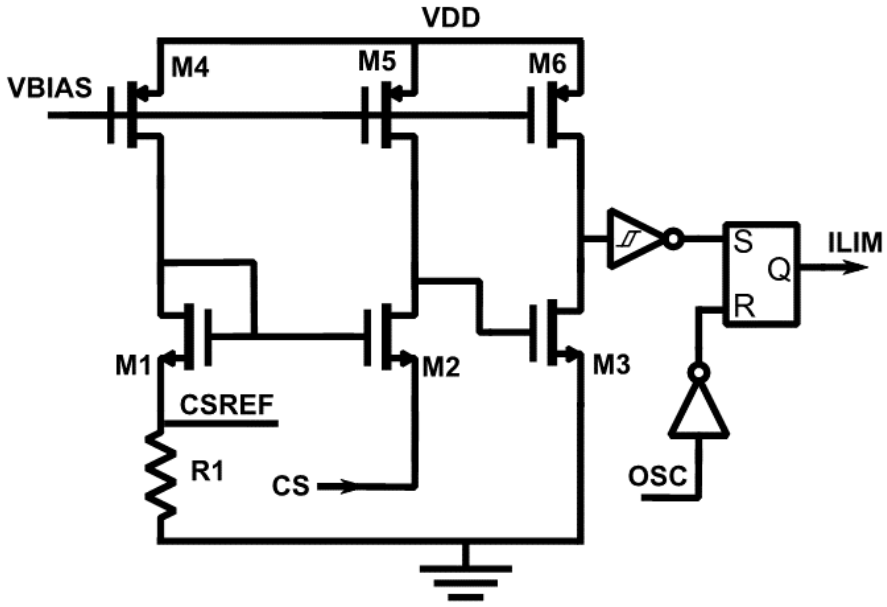


Figure 11: Current limit comparator circuit. The current sense signal (CS) is from the source degenerated finger of power nMOS and the current sense reference (CSREF) is internally generated. The output ILIM is reset at the end of every TON of OSC signal. During regular operation, the ILIM goes high whenever the CS signal goes above CSREF, indicating peak detection of induction current and hence truncating the power FET gate pulse to limit the current.

4.4 Design of the Other Circuit Blocks

4.4.1 Reference and bias generator

The reference block is a supply independent current generator and V_{BE}-based reference voltage generator as described in [49]. The generated bias current is mirrored in all other blocks. For simplicity the block level schematics (Oscillator, feedback comparator and current limiter circuit) are drawn with V_{BIAS} only, although in reality, all block level V_{BIAS} are locally generated through the standard current mirroring technique.

The use of this reference design eliminates complex temperature correction and close loop bandgap reference generation techniques to reduce area and power overhead. The design choice is a tradeoff between temperature insensitivity with continuous biasing overhead and is justified by the fact that in many applications (e.g., Body area network) the actual operating range of temperature is quite narrow. The circuit is designed without

cascoding element helping it to start generating current at subthreshold bias levels. Additionally fewer branches and elimination of the close loop control ensures only small bias current consumption.

4.4.2 Feedback Comparator

Feedback comparator works as the core decision making circuitry for this hysteresis mode converter. Feedback voltage is sensed via the external resistive network and is compared with the internally generated reference, as shown in Fig. 10 . The output of the comparator (EN) defines active (V_{FB}<V_{REF}) or idle (V_{FB}>V_{REF}) mode. The feedback circuit consumes $\sim 1\mu$A of bias current. The design trade-off with such low bias current is the delay of the comparator response time. The simulated delay is nearly 400ns that is expected to result a decrease of the regulated valley of the output voltage at different load conditions. The effect of delay is expected to be prominent at higher load condition. Further discussion is provided in the load regulation subsection under measurement results section. The cascode free design allows very low operating voltage of the comparator which in turn ensures that during low voltage self-start condition, the EN signal stays in the right condition to enable the oscillator.

4.4.3 Current Limit Circuit

For high impedance and low output current energy transducers, current limiter circuit is of crucial importance, lest the high inrush current cause severe droop resulting failure during start up. Fig. 11 shows the common gate configured current limiting circuit that compares current sense input (CS) with internally generated current sense reference (CS_{REF}). CS is generated by sampling 5% of the total current flowing through the power FET by a source degeneration resistor (R_1= 15Ω in Fig. 7) in one of the FET fingers. The CS_{REF} is generated by mirroring the reference bias current and pushing it through an on-chip polysilicon resistor. When the sensed current crosses the predefined threshold, i.e., the CS goes above CS_{REF}, the output of the high gain comparator changes state (Positive edge of

I_{LIM} signal is generated). The output is reset at each T_{OFF} period of OSC, ensuring that at the beginning of next cycle the I_{LIM} signal remains at low state.

4.5 Start up operation

The boost regulator can be operated with or without external battery. With an external battery, the system is biased by the battery and the oscillator and other circuits are functional irrespective of the input voltage and hence the system is capable of boosting from very low voltage. With very low input voltage, the boost regulator system must be biased/powered by an external battery of 0.5V or higher (up to 1.2V) in order for the system to operate. The battery provides V_{DD} of the system, hence all control circuitry runs from the battery. The oscillator enables the power FET which continues to turn on and off, and inductor current builds up. Since the input voltage and the biasing V_{DD} is decoupled, the system boosts the available input voltage with the maximum conversion ratio allowed by the oscillator duty cycle. In this condition, the oscillator and other circuit functionality do not depend on the input voltage magnitude as they are controlled by the V_{DD}/battery. Hence the system can boost from extremely low voltage. We report 11.5mV as the smallest input voltage with 660mV regulated output, however, even at lower input voltages (lower that 11mV) unregulated output is available. In the experiment, it is observed that the converter fails to produces any output below an input of 5mV when the inductor current becomes so small that it cannot overcome the node charging capacitor at the switch-schottky node.

When the system is operated without the battery, the V_{DD} is connected with the V_{OUT}, so the system can be biased by its own generated voltage. For the system to work in battery less mode, the input voltage must be high enough so the oscillator and reference generator can start working. When a suitable input voltage (usually more than 300mV) is available, the output voltage follows the input, with certain drop across the schottky diode. Since output is shorted with the V_{DD}, once the critical starting threshold is crossed, the reference generator produces current which in turn starts the oscillator. The starting

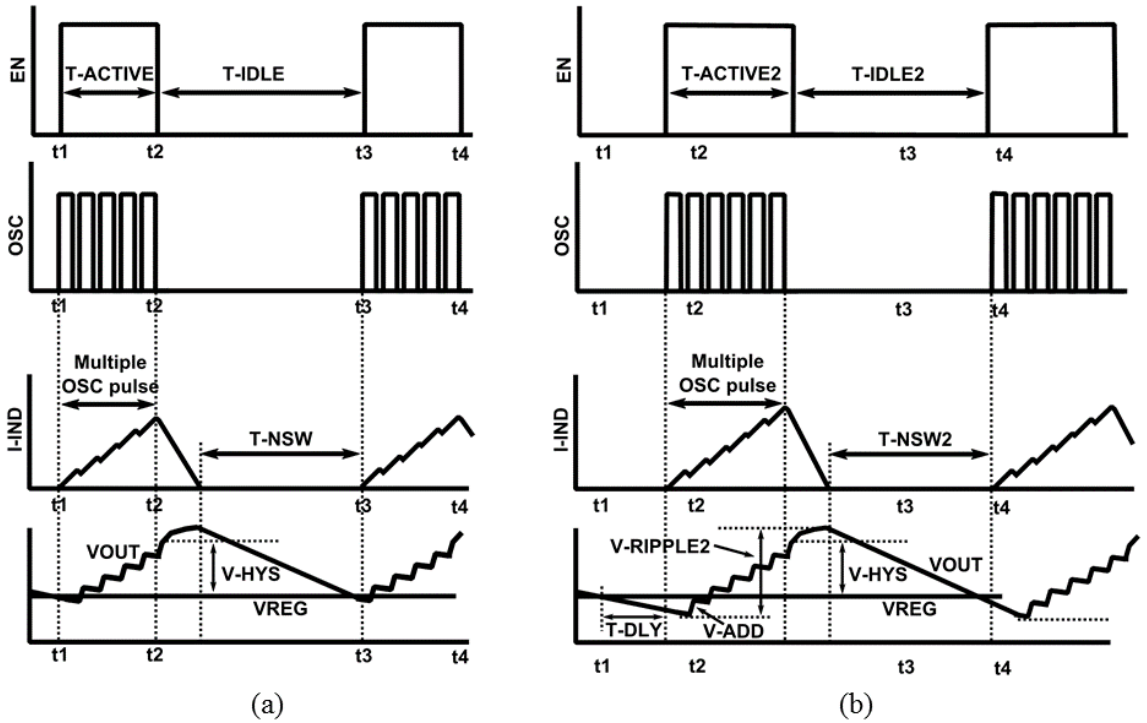


Figure 12: The effect of feedback comparator delay on the ripple magnitude. (a) Ideal case without any feedback delay. The OSC turns on as soon as the output voltage crosses the regulation threshold. (b) The practical case with delay in the feedback comparator. The oscillator turns on a finite delay (TDLY) after the output voltage crosses the regulation threshold. Practical ripple is higher than the ideal ripple by an additional amount (VADD). TNSW refers to the time with no switching events. Total idle time is the sum of TNSW and the time for the peak inductor current to reach zero.

the oscillator is the key to starting the system, since this allows the power transistor to switch and transfer charge to output. At the beginning of this autonomous start up, at every pulse the output rises by a small amount as some amount of charge is transferred to the load. With increasing output which is also the biasing voltage of all circuitry, the reference current, oscillator frequency and power transistor's gate drive increase. This act as a positive feedback mechanism and keep boosting the output voltage until it reaches the regulation level when the feedback loop takes over and keep regulating at that particular voltage level.

4.6 Output Voltage Ripple

Depending on the load and input voltage, if the ripple voltage produced by the converter is more than the designed hysteresis, the converter will run in single pulse operation. On the other hand, if the ripple produces by a single pulse event is smaller than the hysteresis; the converter will run of two or more pulses at every EN high event. At consecutive pulses, the output voltage will build up slowly and eventually cross the hysteresis, resulting the mode transition to idle mode. In the multiple pulse event, the ripple is defined approximately by the hysteresis value. Therefore, it is important to first compute the expression of the maximum ripple for the single pulse event as follows (refer to Fig. 8) for associated conceptual waveform). The inductor peak current at the end of T_{ON} (Oscillator pulse high time) is defined by:

$$I_{PK}=\frac{V_{IN}}{L_{IN}}T_{ON} \tag{13}$$

The time taken to discharge the inductor current to zero after the NFET turns off, is defined by,

$$T_{BOOST}=\frac{I_{PK}}{V_{OUT}-V_{IN}}L_{IN} \tag{14}$$

During T_{BOOST}, the output capacitor is charged by the inductor current and the output voltage increases to a higher value. The maximum increase in the output occurs when load is zero, resulting highest ripple magnitude. In ripple voltage that condition, is defined by,

$$V_{RIPPLE\_CHARGE}=\frac{I_{PK}T_{BOOST}}{2C_{OUT}} \tag{15}$$

Additionally due to the output capacitor's equivalent series resistance (ESR), the initial change in the output voltage is defined by,

$$V_{RIPPLE\_ESR}=I_{PK}R_{ESR} \tag{16}$$

Using (26)-(30) the total ripple can be expressed as,

$$V_{RIPPLE\_SINGLE\_PULSE}=V_{RIPPLE\_CHARGE}+\ V_{RIPPLE\_ESR}\ =\frac{V_{IN}}{L_{IN}}T_{ON}\left(R_{ESR}+\frac{T_{ON}}{CR+C_{OUT}}\right) \tag{17}$$

Where, CR is the conversion ratio ($=\frac{V_{OUT}}{V_{IN}}$) of the regulator.

Equation (31) relates the maximum frequency of operation ($f_{OSC} = \frac{1}{T_{ON}+T_{OFF}} = \frac{D}{T_{ON}} = \frac{0.984}{T_{ON}}$), the output capacitor, input inductor, input voltage and output voltage with the magnitude of the maximum ripple.

The delay in the feedback path might affect the ripple. With a finite delay in the path, the decision point of the feedback comparator may result in an extended idle time (refer to Fig. 12) and the output voltage might fall well below the regulation threshold, before the comparator may turn on the oscillator.

The lowering of output voltage below the regulation threshold level will appear as an added ripple magnitude and with increasing delay in the feedback path, the ripple will increase. This additional ripple happens only with the multi pulse condition. In single pulse condition, although the output might start lower with additional delay, since the peak current is not changing, the change in output voltage will be same as before. Hence the ripple magnitude will be same. However, if the change (ripple magnitude) is less than the hysteresis value, the comparator will not switch to idle mode after one pulse and the converter will move to multi pulse mode. The additional ripple is expressed as,

$$V_{RIPPLE\_FBDELAY}=\frac{I_{LOAD}T_{DLY}}{C_{OUT}} \tag{18}$$

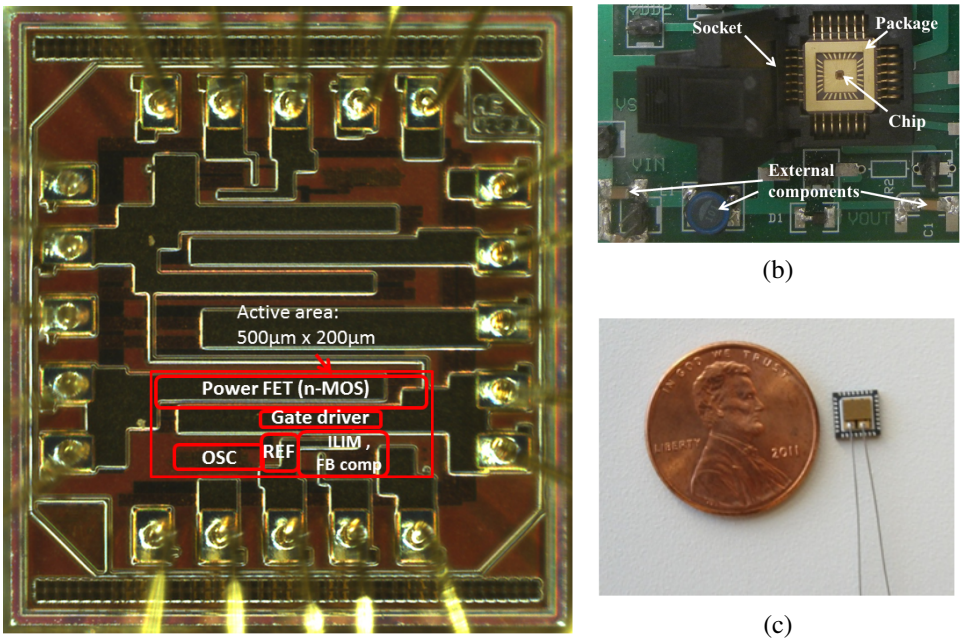
Hence, the practical ripple magnitude in multi pulse operation with finite delay in the feedback is expressed by,

$$V_{RIPPLE\_MULTI\_PULSE}=V_{HYS}+\ V_{RIPPLE\_FBDELAY} = V_{HYS}+ \frac{I_{LOAD}T_{DLY}}{C_{OUT}} \tag{19}$$

Finally, in hysteresis mode controller, the system's overall ripple is defined by the higher of the voltage values between the ripples defined by equation (30) and equation (32).Therefore, the final ripple is expressed by:

$$V_{RIPPLE\_MAX}=\max\left(V_{RIPPLE\_SINGLE\_PULSE}, V_{RIPPLE\_MULTI\_PULSE}\right) \tag{20}$$

The quality of power delivered depends on all of these parameters. As evident from equation (30)-(32), higher frequency of operation can reduce the ripple and improve the power



(a)

(b)

(c)

Figure 13: (a) Die micrograph of the implemented chip, (b) Board photo of the test setup showing the socket, package and external components and (c) photo of the TEG device used as energy source during testing.

quality. Additionally, higher inductor value and higher output capacitor help to achieve lower ripple as well. A low ESR output capacitor also reduces the ripple. Likewise a faster feedback delay and a lower hysteresis value reduce the ripple as well.

4.7 Measurement Results

Fig. 13a shows the die-photo of the test-chip. Active chip circuitry consumes 0.55mm X 0.2mm silicon area. Fig. 13b shows the characterization board, showing the open lid packaged chip revealing die in the center, the 3mm x 3mm LCC 28 package and mounting socket along with the external passive component used for testing. External inductor (100VH, ESR = 240mΩ), input and output capacitors (100VF, ESR = 450mΩ), and schottky diode (V_{FWD}=300mV at 150mA) are used on the board. The resistances of the board and the package traces in the power loop are measured to be 10mΩ and 15mΩ, respectively. The test-chip is measured individually and is also connected with the eTEG to characterize

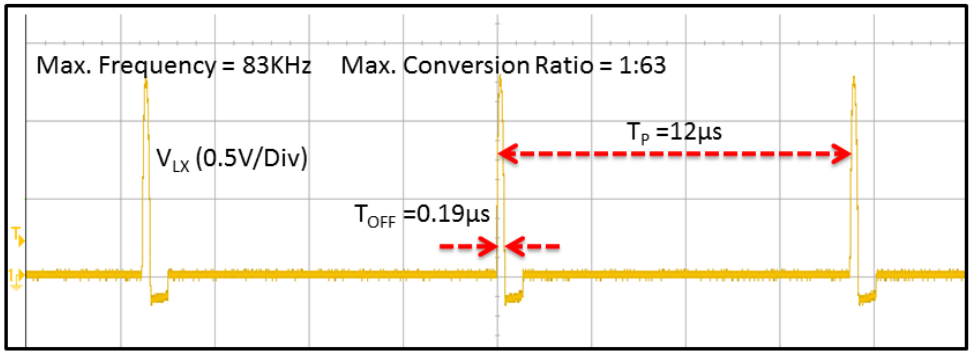


Figure 14: Maximum possible duty cycle generated by the oscillator.

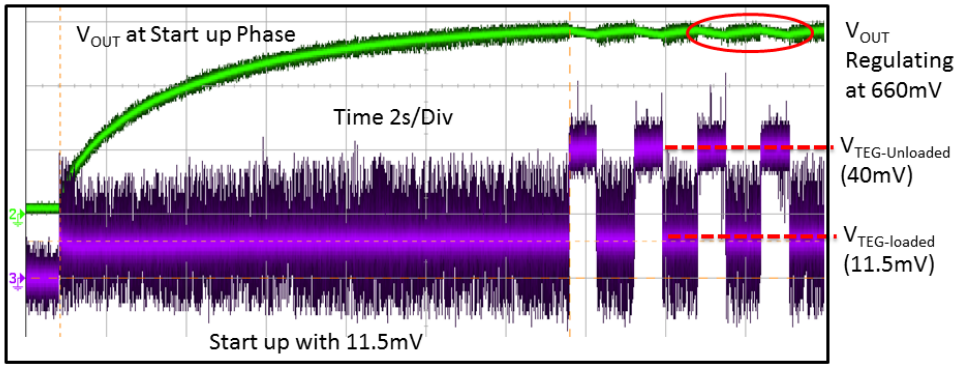


Figure 15: Start up from 11.5mV input votlage and regulation with 1:57 conversion ratio.

the system performance. The chip was tested in two operating mode: first, in the assisted start-up mode where the supply voltage of the control circuits is provided from an external battery; and second, the autonomous start-up mode where the output node itself provides the supply voltage of the control circuits (bootstrapped operation). The objective of measurement is to first verify sub-20mV operation during assisted start-up and subthreshold (˜300mV) operation during autonomous start-up. Next, the performance of the integrated system (test-chip + eTEG) is characterized. The following subsections present the measurement results. A photograph of the eTEG [8] used as the energy generating transducer is shown in Fig. 13c..

4.7.1 Wide Input Operation and Autonomous Start Up

The characteristics of the oscillator and reference circuits are measured to verify the potential of very low input assisted start-up and autonomous start-up at subthreshold voltage.

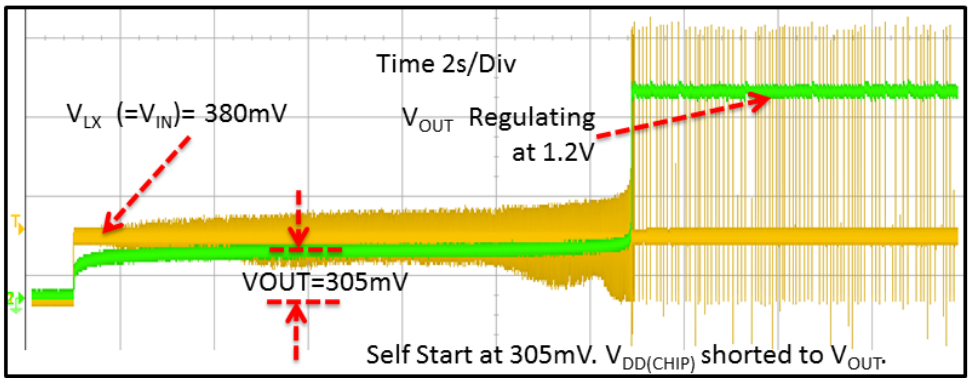


Figure 16: Start up without battery in boot-strapped mode.

The maximum possible duty cycle is estimated by observing the V_{LX} signal during start up phase. Note that V_{LX} depicts the inverse of the internal oscillator's output (OSC) at maximum duty cycle operation. As shown in Fig. 14, the measured maximum possible duty cycle is 98.4% which enables the chip to boost up to 1:63 conversion ratio. Therefore, for a 660mV regulated output we expect the minimum input voltage to be approximately 10.5mV. The maximum possible duty cycle is less than the designed one (98.4%). This can be attributed to the mismatch of capacitors due to parasitic, mismatch of current mirroring and threshold offset of the transistors (especially M_1 and M_6 in Fig. 9).

We next characterize the behavior of the integrated system i.e. the boost regulator connected with the LairdTech eTEG [8]. The potential of energy harvesting from sub-20mV input voltage is verified first using the battery assisted start-up of the booster [the oscilloscope waveform is shown in Fig. 15]. The booster is biased with an external battery of 1V. The oscilloscope waveform shows that the regulator boosts from 11.5mV (corresponds to 2°C temperature difference across the TEG) and regulates the output at 660mV while delivering 10μA load. The noise observed in the source voltage is due to the high internal resistance of the energy source and insufficient input filtering effect. Note that maximum possible conversion ratio (63:1) is more than the regulated one seen in this figure (57:1). The maximum conversion ratio can be achieved by connecting the feedback node to ground

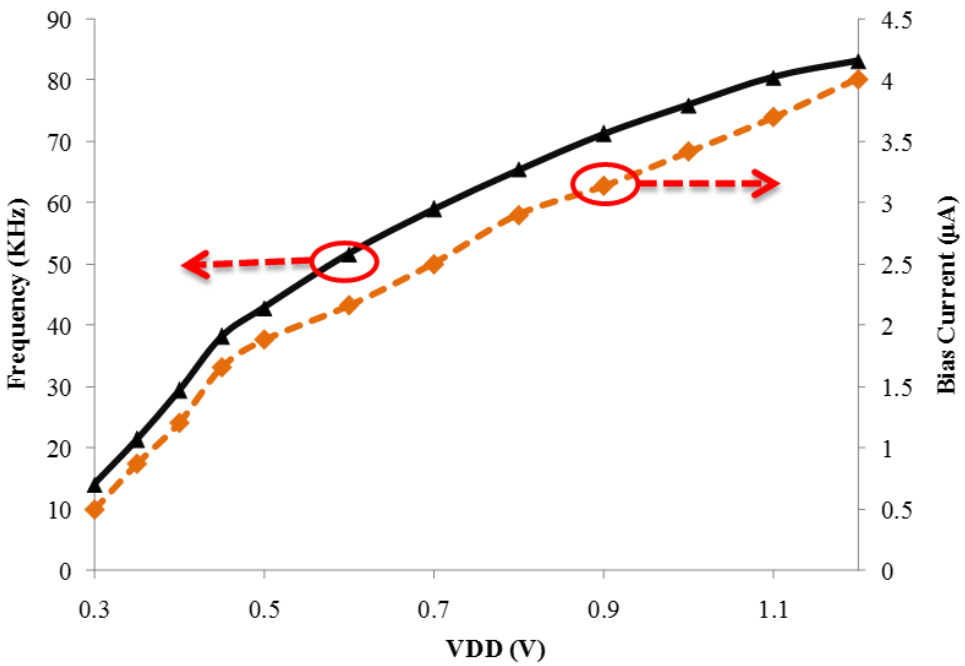


Figure 17: Dependency of oscillator frequency and bias current on biasing voltage.

which forces the converter to operate in open loop condition and results in maximum possible output voltage for any given input. The autonomous start up (without external battery) event in bootstrap topology where the V_{DD} of the chip is shorted to the $V_{OUT}$is verified in Fig. 16. With 380mV at the input, the output voltage reaches 305mV being charged through the input-inductor-schottky diode path and the internal bias generator and the oscillator start up at this voltage, transferring charge to output. Initially, weak gate drive due to lower V_{DD} results higher $R_{DS\,ON}$ (evident from the V_{LX} pin minimum voltage profile during initial phase of start up) and limits inductor current. During this phase charge transfer is very slow, and it takes much longer for the output to increase even by little. However, a slight increase in V_{OUT} helps reduce the nMOS on resistance (V_{GS} increases) and produce more frequent switching (OSC frequency increases), both of which facilitate more charge transfer to output. Final phase of output rises quickly and starts regulating at the externally set value.

Fig. 17 shows the variation of the oscillation frequency with biasing voltage (V_{DD}). The oscillator frequency increases with increasing bias voltage. This is because due to the use of

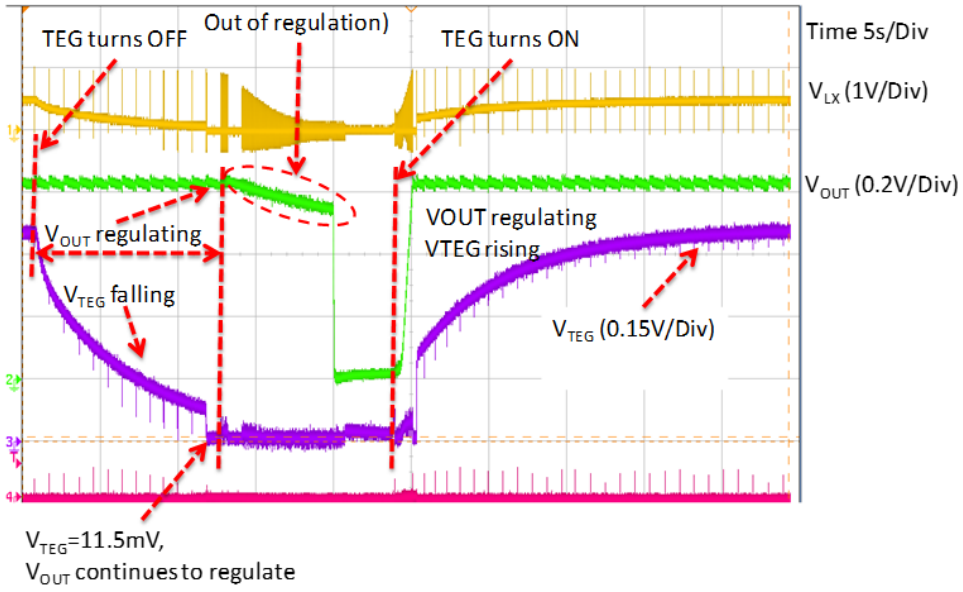


Figure 18: Regulator operation with dynamically varying input voltage.

non-regulated reference circuit, the bias current increases at a higher V_{DD}which results in an increased frequency. The oscillator's duty cycle is measured and found to be constant at all biasing voltages. The measurement results demonstrate that the oscillator functions even at 300mV providing opportunities for very low-voltage autonomous start-up. Moreover, the oscillator can operate over a wide voltage range demonstrating the potential for wide input operation in the autonomous operating mode. The chip exhibits seamless startup and operation in autonomous mode starting from 0.305V to 1.1V (or higher depending on output regulation level) and some of the higher voltage results are presented in the efficiency measurements subsection.

The wide input range of the regulator, along with low input battery assisted startup is shown in Fig. 18. Initially the LairdTech eTEG [8] is turned on and generating 0.5V (V_{TEG}) which is used as the input of the boost regulator. The regulator boosts the voltage and regulates at 0.66V (V_{OUT}). After some time, the TEG is turned off and the TEG output (i.e. input of the booster) starts falling. However, the booster continues to regulate the output at 0.66V even with the falling input voltage, until V_{TEG} falls below 12mV. When input drops below 11.5mV the booster stops functioning and the output drops out of regulation, as seen

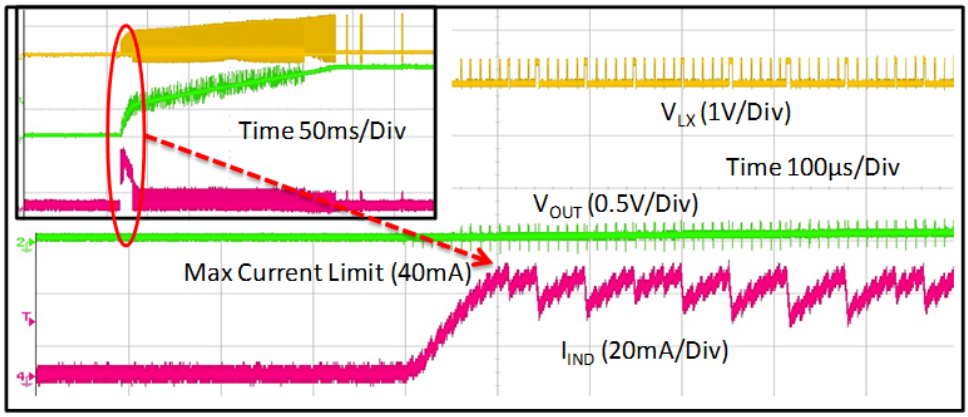


Figure 19: Current limit protection event during start up.

from the figure. Next, the output voltage is completely discharged (through the external load) to reduce the output of the boost regulator to 0V and then the TEG is turned on once again. This ensures that the output of the boost regulator has to rise from zero when V_{TEG} becomes available. As the TEG turns on, V_{TEG} rises slowly (due to the high thermal capacitance that is inherent to the transducer), however output of the boost regulator (V_{OUT}), reaches to regulation level quickly. Fig.18 demonstrates the converter's capability of boosting with wide range of conversion ratios, from 1:57 (11.5mV to 0.66V) to 1:1.3(0.5V to 0.66V), changing the conversion ratio smoothly throughout the whole range. The chip is tested for various input/output ranges verifying that the minimum required input voltage of the booster is 12mV and the maximum allowed input is bounded by the target output voltage.

4.7.2 Boost Regulator Features and Performance

Fig. 19. shows the inductor current profile during start up revealing the over current protection circuits current limiting feature. The inrush current is limited to 40mA as designed. The current limit prevents higher droop of the energy transducers output. On the other hand the current limit circuit puts an upper limit on the maximum deliverable load current.

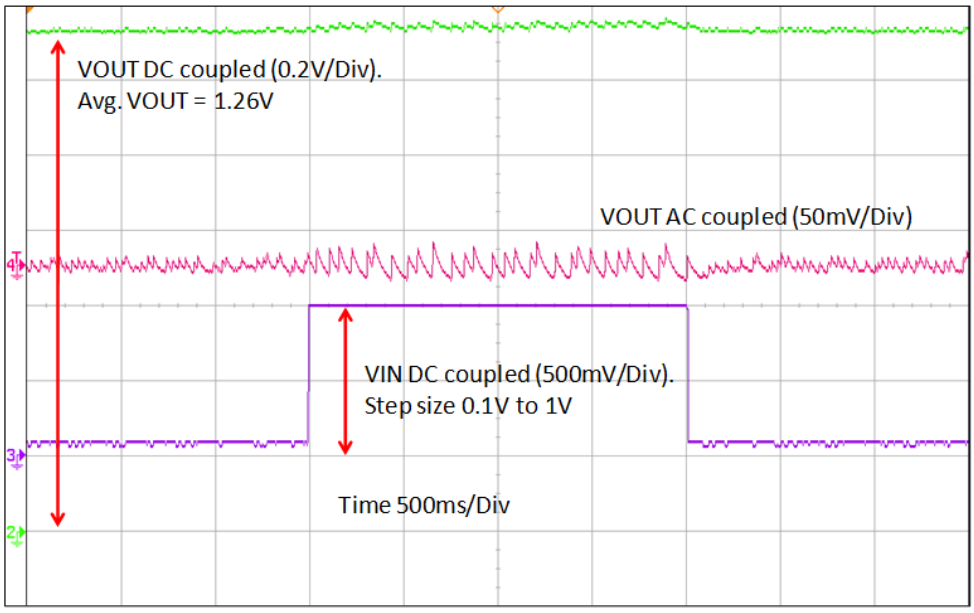


Figure 20: Line regulation performance of the regulator. The regulator goes into more spurious switching as the input increases.

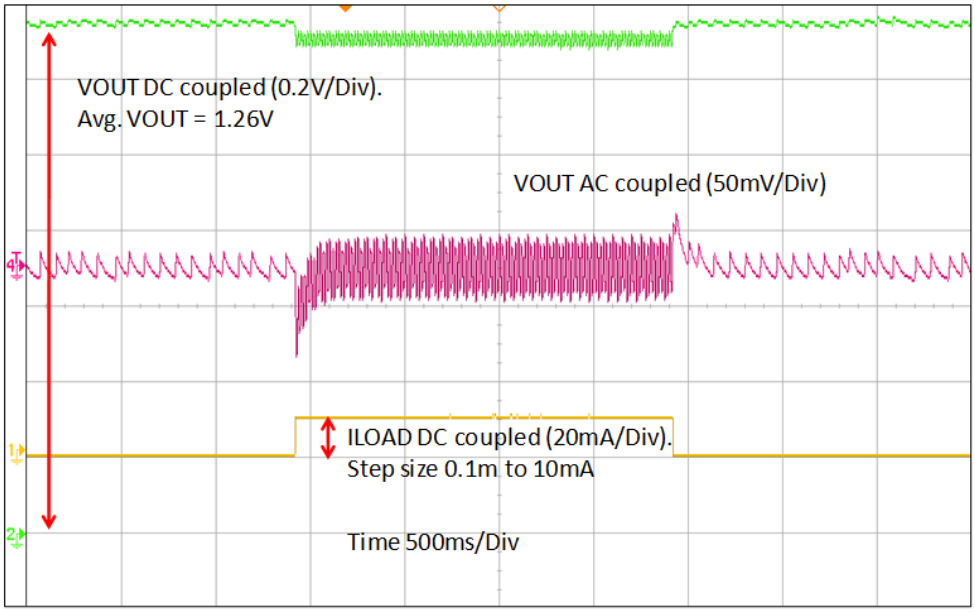


Figure 21: Load regulation performance. With higher load, the regulator switches more frequently. The regulator exhibits a single pole system

4.7.3 Regulation

A good line regulation helps a converter to operate reliably even if the energy field of the transducer (i.e. temperature for the eTEG) varies dynamically. Fig. 20 shows the line

regulation characteristics of the converter. The input step is from 0.1V to 1V with 100μs rise and fall time. With higher lower input voltage frequency of pulses are more because of the lower inductor current resulting output ripples of less than 10mV. When input jumps to 1V, the frequency of pulses reduces because of lower conversion ratio, and ripples increases because of higher inductor current. The DC value of output shifts by 15mV, producing a line regulation of 1.3%/V. Fig. 21 shows the response of the regulator with a load current step. The output load is varied from 100μA to 10mA with both rise and fall time of 10μs. With higher load current the converter switches more often and with lower current the switching becomes sparser. The DC value of output shifts by 40mV at 10mA, producing a load regulation of 0.3%/mA. The operation of this converter is valley controlled; hence the valley of the output is expected to be same regardless of the load condition. However, from Fig.10(b), the valley of ac coupled V_{OUT} is seen to differ from high load to low load condition. This is attributed to the delay of the feedback regulator. At higher load condition, the output voltage falls faster as compared to lower load condition. Since the delay remains fixed at both conditions, output voltage falls farther below the designed threshold at higher load levels before the response time of feedback comparator enables the next pulse. A faster feedback comparator consuming more bias current offers the necessary trade-off for load variation sensitivity of output voltage.

4.7.4 Power and Efficiency Analysis

Efficiency of the regulator is measured at different load and input voltage (with fixed V_{OUT}=1.2V) conditions to understand the power efficacies of the wide input voltage operation and shown in Fig.22. The measured efficiency increases at higher input voltage and higher output load. At or above 10μA load current, the efficiency is higher than 50%, reaching a peak efficiency of 82% at 10mA load current. At 10mA load, the schottky loss contributes ~2.2mW when the converter is delivering 12mW of output power at 1V. The other loss components include the losses in the inductor and capacitor series resistances and the converter bias current loss (including the switching loss).It can be observed from a

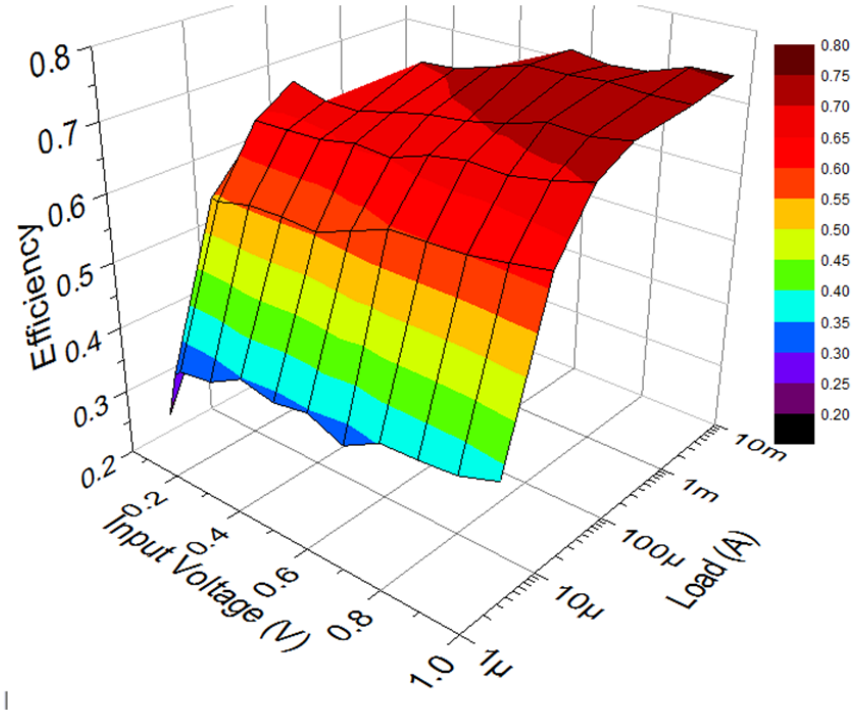


Figure 22: Effiiency profile of the boost regulator with varying load current and input voltage.

standard loss model equation that schottky loss is the major loss contributor as the losses in the ESR of inductor and the NFET R_{DSON} (~178μW), and the bias loss (~4μW) are much less, with the mentioned load and input voltage. The loss components, including the schottky diode loss, decrease with the load current. However, except the forward conduction loss of schottky, other schottky diode associated losses (e.g., capacitive loss of schottky) do not decrease with load current. Thus, although the absolute value of the schottky loss decreases, the ratio of the loss as a percentage of total power delivered increases contributing to the reduced efficiency at lower load current. Hence, at moderate load current levels (~100μA to 10mA), the efficiency reduces slowly with the load current reduction mainly due to the linear reduction in delivered power but sub-linear reduction in the losses. However, the efficiency starts to decrease sharply below ~100μA load current range and reaches below 50% at load current lower than 10μA. This is because although the component losses continue to reduce with the load current reduction even in this region, but the total loss does

not change significantly due to the nearly constant bias loss of the converter. As illustrated in Fig. 23, the converter bias current initially reduces with a reduction in the load current but beyond the 100μA level the bias current does not change much with the load current. For example, at 10μA of load current, the loss in the schottky (~2μW) is smaller than the bias loss (~3.6μW), and the losses in the ESR of inductor and the NFET R_{DSON} (~18nW) are negligible. Hence, in this region the efficiency starts dropping sharply with the load current as the delivered power reduces but the total loss remains nearly constant. At very low output current (1μA) the converter bias consumption (~3.5μA) is more than the power delivered at the output, resulting in less than 25% efficiency.

On the other hand, for constant load current and output voltage, the delivered power does not reduce with a reduction in the input voltage of the boost regulator. Note that a lower input voltage also does not change the schottky diode loss. But as the input voltage decreases, the converter switches more often (pulse frequency increases) to compensate for the increasing conversion ratio, resulting in higher switching loss. Also, with increased conversion ratio with a lower input voltage but constant output voltage (i.e. increased conversion ratio)) and load current, the average input current increases. Hence, the conduction losses in the inductor ESR and the NFET transistor increase. Consequently, due to the increased bias current and losses in the input side components, the efficiency reduces at a lower input voltage.

Fig. 23 shows the bias current profile of the chip (at 1V V_{DD}) as a function of load current. With increasing load current switching becomes more frequent, which increases chip current consumption. The standby current (no load) is roughly 3.5μA and it increases monotonically as the load current increases reaching 6.5μA at 10mA of output current. With increasing load, the ratio of active switching time to idle time increases, which increases overall current consumption, as seen in the result. However, while the load current increases exponentially the bias current increases only super-linearly, suggesting that overall efficiency increases at higher load currents. At low load condition, the constant bias

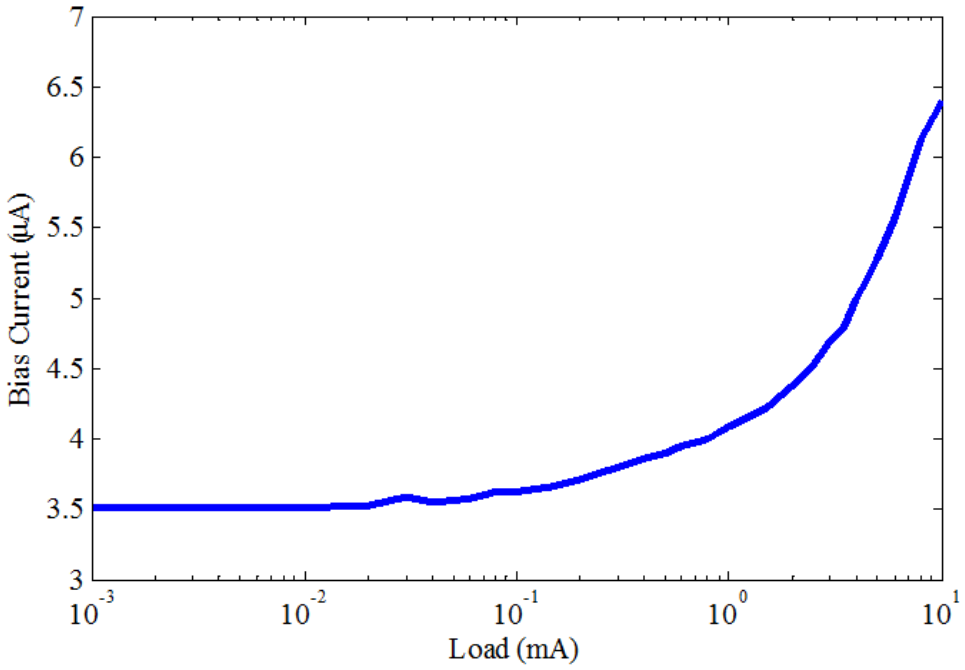


Figure 23: Voltage generated by the TEG and the power delivered at the output of the boost regulator at temperature differential across the two plates of the TEG device.

current reduces the overall efficiency.

Fig. 24 shows the generated power of the eTEG device and the power delivered at the output of the boost regulator as a function of differential temperature across the eTEG device. The output of the regulator is fixed at 0.66V up to 10°C of differential temperature and at 1.2V for temperature difference above that. The peak efficiency at each configuration is plotted with respect to the temperature difference across the eTEG device along with the maximum power delivered by the device and the loaded output voltage of the device. As the temperature increases, the eTEG generates more power; hence the delivered power at the load increases. With higher temperature, i.e., higher voltage at the input, the boost regulator delivers power with around 80% efficiency. The measurement demonstrates potential operating range from 2°C to 50°C of temperature difference while providing regulated output voltage.

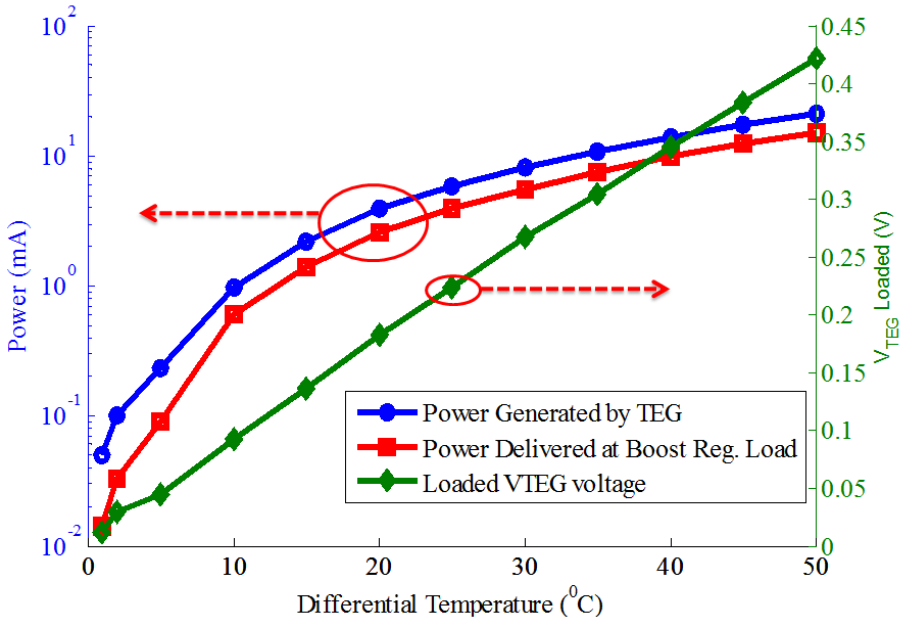


Figure 24: Voltage generated by the TEG and the power delivered at the output of the boost regulator at temperature differential across the two plates of the TEG device.

4.7.5 Discussions on the Stability of the System

The hysteresis or bang-bang controller loop can be broken down in two distinct periods (active and idle period) and due to its discrete feedback nature, the controller is inherently stable. To understand the system's transient stability, i.e., how the system reacts to sudden load change or input change, we analyze the poles in the system and calculated that with the capacitor used (100μF) and with the maximum load current (10mA), the highest load pole is located at 16Hz. At lowest load condition the load pole decreases further, e.g., at 10μA load current, the pole is located at ~0.01Hz. The delay in the feedback path, primarily due to the delay in the feedback comparator delay (300ns) produces a pole at ~1MHz. Since the load pole and the feedback delay poles are far apart, the low frequency load pole dominates and the converter behaves as a single pole system. This is evident from Fig. 21, as the load is stepped high, the output voltage falls below the regulation. To restore the output voltage, the converter starts switching more frequently and the output voltage return

to the regulation level following a typical single pole (RC) response characteristic. From the response time, the pole location is found to be ~5Hz, which matches the theoretical value.

4.7.6 Output Voltage Ripple from Measurement

This converter is characterized with 100μF capacitor with 0.45Ω ESR, 100μH inductor. For an exemplary case, with input voltage of 0.6V and output voltage of 1.2V, the converter produces a ripple magnitude of 33mV using equation (33) – which is found to match the test data. Since the designed hysteresis is 15mV at FB (30mV at output with this example), the actual ripple will be the one calculated by the equation (33), i.e., 33mV. The magnitude of ripple decreases with decreasing input voltage, hence at different operating condition, the ripple will be different. The maximum ripple observed from chip measurement is ~50mV, which is seen in Fig. 21 (AC coupled output voltage).

4.7.7 Comparison with Prior Works

Table 1 compares different attributes of the chip against other reported works on low-power/low-voltage boost converters. The most relevant comparisons are with [28, 34], which also use assisted start-up. Key achievement of this work is the small minimum harvesting voltage (mean=12mV and minimum=6mV) while maintaining peak efficiency of 82%. Moreover, the chip starts up autonomously (battery-less) at 305mV at the output. The corresponding minimum input voltage for self-start is ~380mV, due to the schottky drop from input to the output. These all-electronic self-start voltages are low compared to prior works. It should be noted that, while the minimum self-start voltage at output (~305mV) is a characteristics of the chip, the minimum self-start input voltage value may vary from 380mV depending on the choice of the schottky diode used for the system. This prototype chip delivers maximum output power of 12mW; however with increasing I_{LIM} threshold the power delivery capability can be increased.

Table 1: Comparison chart of this work with prior arts

Item	Carlson JSSC10 [28]	Ramadass JSSC11 [29]	Kadirvel ISSCC12 [34]	Jong-Pil ISSCC12 [30]	This Work
Min. input for Regulated output	20mV	25mV	100mV	30mV	**12mV**
Min. self start	600mV	35mV*	330mV	40mV**	**305mV**
External voltage	Yes	No	No	No	Yes
Regulated Output voltage Range	1.4V	1.8V	3V	2V	0.66V-3.3V
Input range	20mV-250mV	25mV-V_{OUT}	330mV-V_{OUT}	50mV-V_{OUT}	12mV-V_{OUT}
Peak efficiency	75%	60%	92%	61%	**82%**
Max Pout	175μW	300μW	~12mW	N/A	**12mW**
Process	0.13μm	0.35μm	N/A	0.13μm	0.13μm
Area	0.12mm^2	4.2mm^2	N/A	0.09mm^2	0.1mm^2
*Requires Motion Activated Sensor. ** Requires Negative-V_{TH} MOSFET.					

4.8 Summary

This chapter presents a boost converter to harvest energy over a wide input voltage range. Analog current based oscillator that produces high duty cycle facilitates energy harvesting from sub-20mV input. Wide input and output range and high efficiency make the presented converter an attractive candidate for various energy harvesting systems including bio-medical, wireless sensors, wearable electronics and low range transmitter/receiver etc. We believe the proposed design is most suitable for energy harvesting applications where transducer's output field varies widely and often goes to very low voltage. Further, the capability of fully autonomous startup with sub-threshold voltage provides a solution for extending the operating life in the case of battery failure or complete discharge of the storage element.

CHAPTER 5

BOOST REGULATOR WITH REDUCED BIAS CURRENT

This chapter discusses the analysis, design and development of the bias gating technique that improves the operating efficiency of regulators specially running with Pulse-Frequency Modulation (PFM) architecture. We will first discuss the basic concept of bias gating technique and how it can be integrated with a PFM mode regulator. Later in the chapter, the prototype chip designed with the proposed bias gating technique is presented with silicon results.

5.1 Introduction

Advanced transducers can produce appreciable (10s of μW) power from small energy fields [8] . Effective energy harvesting from these power sources requires boost regulators with low operating input voltage, low standby current and high efficiency [28–30, 34]. Boost regulators with digital control blocks with sub-μA bias currents have been presented [28, 34]. However, designing regulators with all-analog control blocks and sub-μA bias remains challenging as low bias current of the analog blocks degrade the regulator's performance. This chapter presents autonomous bias gating to achieve ultra-low standby current in pulse frequency modulated (PFM) boost converter with all-analog control (Fig.25). The Feedback Comparator (FC) and the Reference Generator (REF) are required during all the modes of operation of a PFM regulator; but the Oscillator (OSC), the Zero Current Comparator (ZCC), and the Current Limit Comparator (CLC) are only required during the charging (active) mode of the output and are not essential in the discharging (idle) mode. The proposed regulator gates the bias currents of OSC, ZCC, and CLC by turning off digital switches (bias gating) during the discharging mode. The bias gating is performed autonomously using the already available feedback signal in the regulator. The autonomous gating of the bias currents during the idle mode reduces standby and

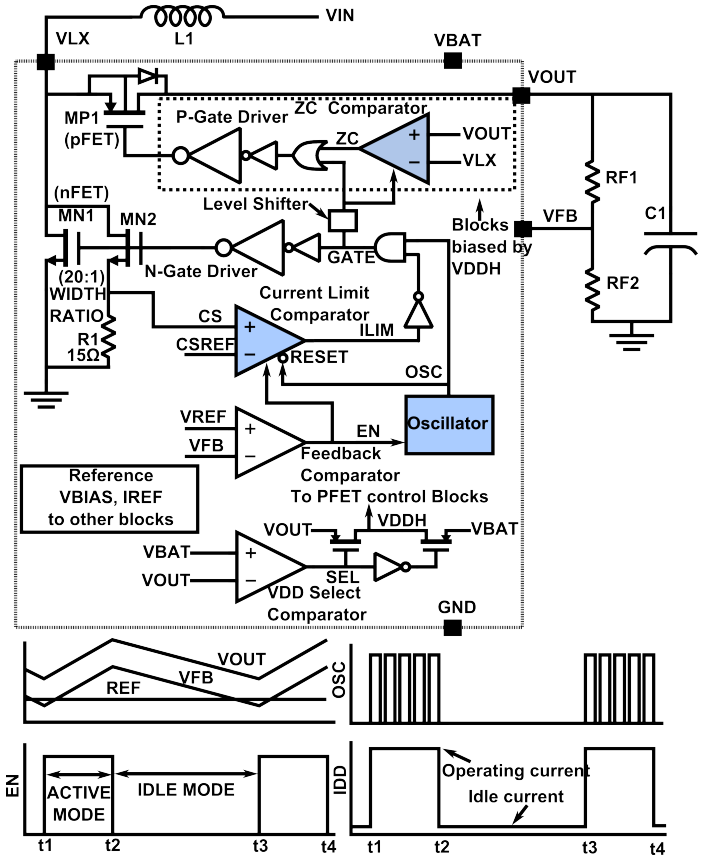


Figure 25: Block diagram of the proposed PFM mode regulator with the bias gating technique. The bias gated circuit blocks are shaded.

average operating current, while still maintaining performance during active mode. The autonomously bias gated PFM boost regulator is demonstrated in 130nm CMOS technology. The bias currents of the non-bias gated blocks are reduced to 10s of nA region. A high duty cycle analog oscillator enables boosting from very low input voltage. The measurements demonstrate a total bias current of 110nA at 1V, a sub-300mV all-electronic autonomous battery-less startup voltage, and high (> 80%) efficiency at both heavy (10mA) and light (10μA) load conditions

5.2 Analysis of Bias Gating Technique in a PFM Architecture

As discussed in Section 4.2, a PFM boost converter switches between the active mode (when OSC and switches operate) and the idle mode (when OSC remains off, so are the

switches). The feedback comparator (FC) senses the output through the external resistor divider, compares it with internally generated reference, and generates the EN signal. When VFB falls below V_{REF} (i.e., V_{OUT} falls below the regulation level), EN goes high (active mode), turning on the oscillator. The OSC signal then propagates through the power FET drivers and enables the inductor to build up current and charge the output capacitor. Once output rises above the regulation point, EN goes low (idle mode). During this mode, no switching occurs and output discharges under the given load. In conventional systems all the operating circuit blocks are biased all the time. In this proposed technique, henceforth called as bias gating technique, based on the fact that some circuit blocks do not make decisions at certain time intervals, those can be shut down without losing the performance. The challenges remain in identifying those blocks, turning them off when they are not required and turning them back on before their decision are to be made. To identify such blocks for a given system we first present a boost regulator system as shown in Fig. 25. This synchronous mode PFM boost regulator consists of several blocks those are identified as non-operating blocks during the idle mode and marked with shade in the figure. The oscillator (OSC),the current limit comparator (CLC), and the zero current comparator (ZCC) are such blocks and during idle mode their bias currents are cut off (i.e., bias gated) using the EN signal. In addition, within the active mode, the OSC circuit is always partially bias gated, and the ZCC is bias gated when the pFET is off as illustrated later. The REF, FC, and VDD-Select Comparator are not bias gated since they remain essential in all modes. The operating current of the chip is the weighted average of the current levels in active and idle modes (ideal operation waveform in Fig. 25).

5.3 Impact of Bias Gating on Power and Efficiency

The simulated bias currents of the individual blocks are shown in Table 2, with and without bias gating. The asynchronous converter is similar to the synchronous one except the

pFET switch, eliminating the current associated with the supply selection and level shifting. The total idle current for the synchronous one is 110nA while the asynchronous one consumes 80nA. Simulated chip currents with and without the bias gating are shown in Fig. 26 across different load current. At higher load, the active mode time to idle mode time ratio increases, thereby increasing the chip current. The peak consumption is limited by the continuous switching condition (no idle time). With bias gating, the initial current consumption is much lower (~1.5X as compared with non-bias gated); however, at higher load the extra switching energy associated with the gate/parasitic capacitances of the bias gating transistors becomes important. The circuits are designed to ensure the bias gating remains energy-efficient until 40mA of load, which is designated by the crossover point in Fig. 26.

The bias gating technique helps reduce overall current while meeting specific delay requirements to manage efficiency and functionality of the booster. A higher delay in the ZCC results in negative inductor current (i.e., discharges the output) which degrades the efficiency. The delay of CLC circuit causes overshoot in the inductor current resulting in higher output ripple and potential malfunction. It is worth noting that the bias gating does

Table 2: Bias current chart of key circuit blocks in non-bias gated and bias gated condition

Circuit Block	Active Mode * (Non-bias gated) Current (nA)	Idle Mode (Bias gated) Current (nA)
OSC	215	3
ZCC	27	9
CLC	18	9
FBC	18	18
REF	25	25
V_sel	30	30
Driver **	16	16
* Excluding switching current. ** Primarily consists of leakage current.		

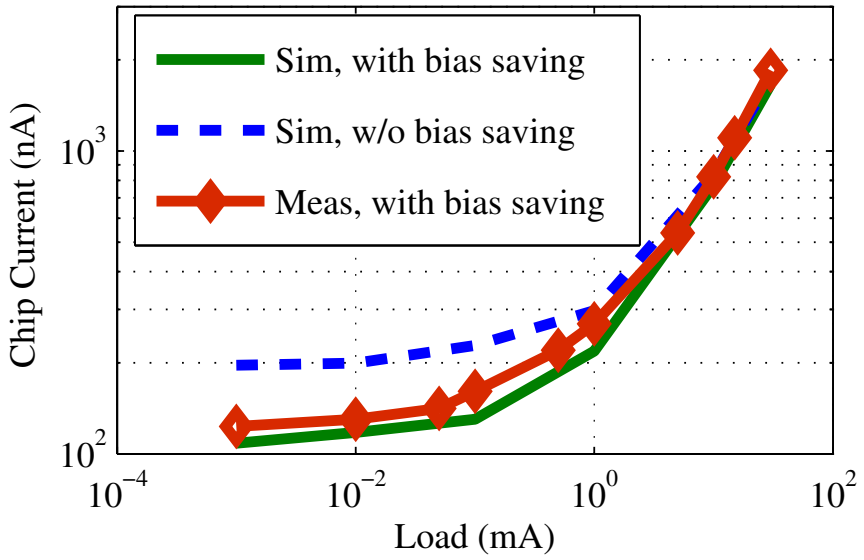


Figure 26: Effect of bias gating on total chip current measured data matches with simulation

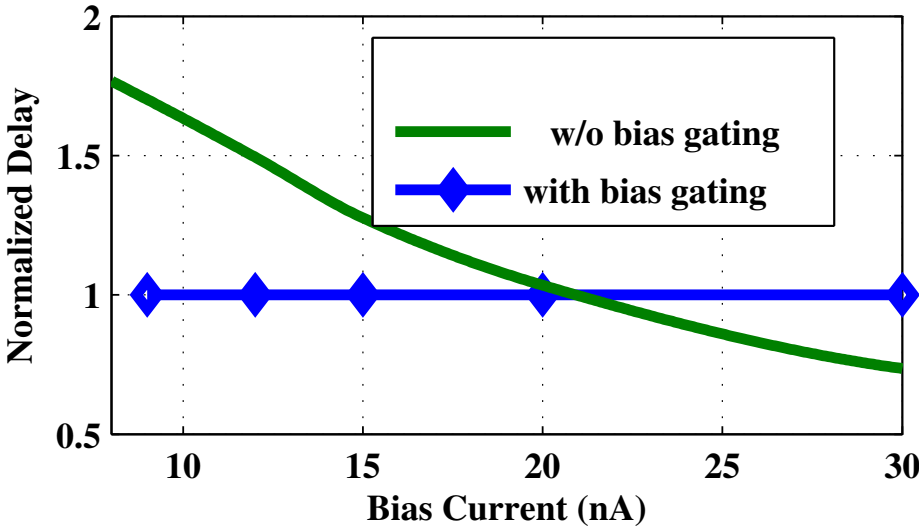


Figure 27: Effect of bias gating on the delay of ZCC (simulation)

not affect the delay since the decisions are generated only in active mode (higher bias current). If the standby power reduction is to be achieved solely by reducing the bias current (in all conditions), the delays of these blocks would have been degraded significantly as illustrated in Fig. 27 and Fig. 28.

The total idle current for the synchronous one is 110nA while the asynchronous one consumes 80nA. Simulated chip currents with and without the bias gating are shown in Fig.

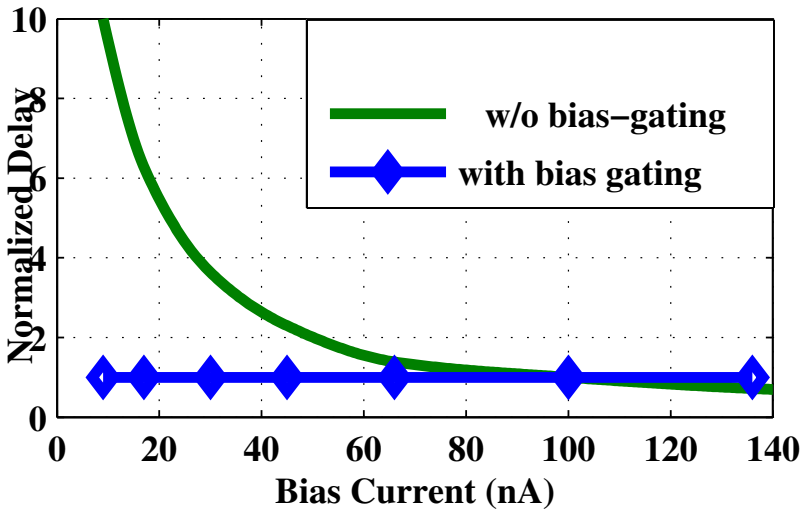


Figure 28: Effect of bias gating on the delay of CLC (simulation)

26 across different load current. At higher load, the active mode time to idle mode time ratio increases, thereby increasing the chip current. The peak consumption is limited by the continuous switching condition (no idle time). With bias gating, the initial current consumption is much lower (~1.5X as compared with non-bias gated); however, at higher load the extra switching energy associated with the gate/parasitic capacitances of the bias gating transistors becomes important. The circuits are designed to ensure the bias gating remains energy-efficient until 40mA of load, which is designated by the crossover point in Fig. 26. The bias gating technique helps reduce overall current while meeting specific delay requirements to manage efficiency and functionality of the booster. A higher delay in the ZCC results in negative inductor current (i.e., discharges the output) which degrades the efficiency. The delay of CLC circuit causes overshoot in the inductor current resulting in higher output ripple and potential malfunction. It is worth noting that the bias gating does not affect the delay since the decisions are generated only in active mode (higher bias current). If the standby power reduction is to be achieved solely by reducing the bias current (in all conditions), the delays of these blocks would have been degraded significantly as illustrated in Fig. 27 and 28.

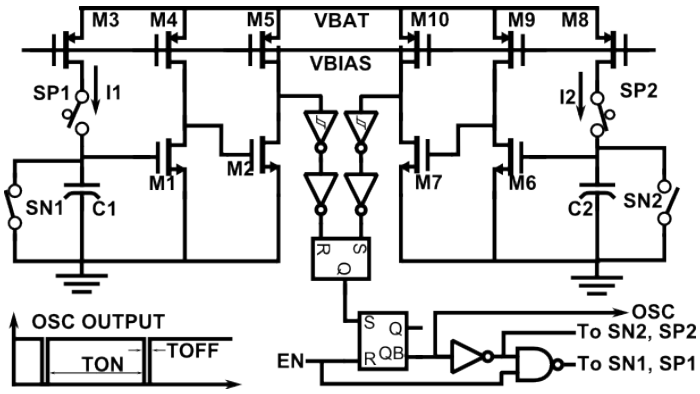


Figure 29: Oscillator schematic with bias gating

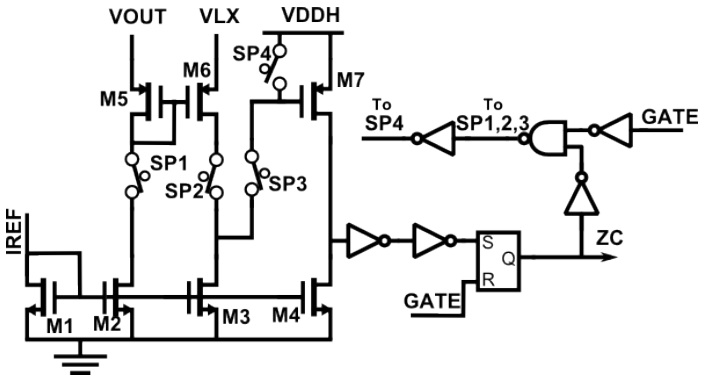


Figure 30: Zero current comparator schematic with bias gating

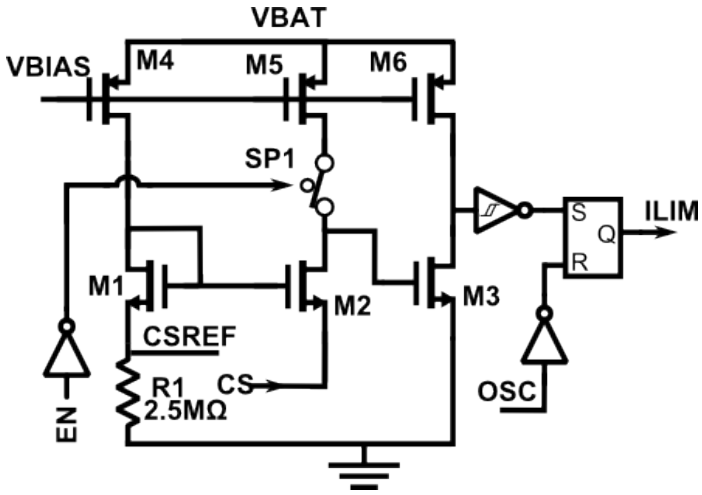


Figure 31: Current limit comparator schematic with bias gating

5.4 Design of the Bias Gated Blocks

5.4.1 Oscillator with bias gating technique:

Fig. 29 shows the high duty cycle analog oscillator (OSC) block with two symmetric half-circuits. This circuit is similar to one shown in Fig. 9 except this one has bias gating technique implemented and provides a EN pulse masking to prevent abnormal pulse truncation. The circuit operates by alternatively turning on I1 and I2 to charge capacitor C_1 and C_2, generating T_{ON} and T_{OFF} periods respectively. The on-time to off-time ratio is determined by I_1/I_2 (=2.5) and C_1/C_2 (=28, 4.2pF and 0.15pF on-chip capacitors) and designed to be ~70. The design ensures that once the TON phase is initiated, it only terminates on its own or by the current limiter circuit – but not by the negative edge of EN (asynchronous signal). Without this masking, in certain conditions, the OSC may produce higher frequency and lower duty cycle. Note that during active mode, one-half of the circuit or the other is always bias gated and during idle mode both halves are bias gated. The duty cycle of the oscillator is insensitive to all PVT condition as described in Section 4.3.

5.4.2 Zero Current Comparator:

The Zero Current Comparator (ZCC), shown in Fig. 30, generates the output (ZC) to turn off the pFET (MP1 in Fig. 25) preventing reverse current through the inductor. The GATE signal is generated by OSC and ILIM, and serves as the bias-gating signal for the ZCC. The ZC signal turns the pFET off and the remaining current flows through the body diode of the pFET. All currents, except the M1 current, are cut off (bias gated) when either ZC or GATE is high. This occurs during the idle mode and within the active mode when pFET is off. The diode-connected device (M1) is not bias gated to reduce the circuit settling time at the beginning of each ZCC active phase.

5.4.3 Current Limit Comparator:

The Current Limit Comparator (CLC) circuit is essential to clamp inrush and over current through the inductor [50, 51]. As shown in Fig. 31, CLC compares inductor current level

[via CS, sensed at nFET MN2 (Fig. 25)] with the local reference, CS_{REF}. When CS goes above CS_{REF}, I_{LIM} changes state to high and turns off the nFET (MN1-2 in Fig. 25). This circuit is bias gated in the idle mode using EN signal and switch SP1. The current through the diode-connected device (M1) is not cut off during idle mode to keep the CS_{REF} available and the amplifier ready at the beginning of next EN pulse to minimize the settling time.

5.4.4 Reference and Bias Current Generator:

An open loop, diode based, supply independent volt-age Reference Generator (REF) is used ([49]). The gate voltage of the diode-connected device (M3) is shared to replicate bias currents all blocks (VBIAS in Fig. 29, Fig. 30, Fig. 31). The elimination of the closed loop reference and temperature correction is justified by the fact that in many operations the variation of ambient temperature is small.

5.4.5 Feedback Comparator:

As shown in Fig. 10, the Feedback Comparator (FC) compares a fraction of output voltage, VFB with internal reference V_{REF}. The output (EN) goes high when VFB goes below V_{REF}. The cir-cuit is designed with hysteresis to regulate the valley of the output voltage.

5.4.6 V_{DD} Select Comparator:

The battery voltage and the output regulation range are decoupled to ensure wide output range in the battery assisted mode. To achieve this goal, the V_{DD} Select Comparator is designed to select the higher voltage between the external V_{BAT} and the generated V_{OUT} as the biasing voltage for all high voltage circuits (V_{DDH}) (Fig. 25). This circuit ensures that the pFET driver receives the highest potential of the whole system to turn the transistor completely off. The circuit is not required in the self-powered mode (battery-less mode, V_{OUT} shorted to V_{BAT}), however, then the operating range of output is limited to 1.2V due to the use of low-voltage devices.

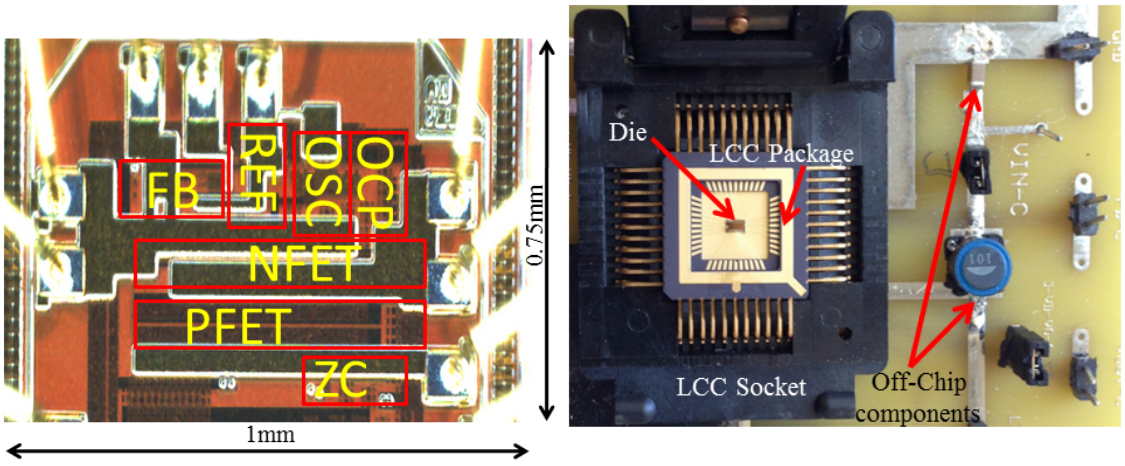


Figure 32: (a) Chip micrograph marking different circuit blocks and (b) Board photo of the setup showing die, package, socket and external components on the PCB.

5.5 Results

Fig. 32a shows the die-photo of the test chip. The fundamental oscillation frequency of the converter is 100kHz. The measured nFET and pFET resistances of the power stage are 400mΩ and 900Ω, respectively. Test board shown in Fig. 32b is used to measure performance parameters of the packaged (LCC44) die mounted on a socket. Parasitic resistances include the board trace (in power loop) (20m) and the socket resistance (25mΩ). External inductor (100μH, R_{ESR}=240mΩ) and input/output capacitors (both, 100μF, R_{ESR}=450mΩ) are used. All measurements are performed using the socket and the board; hence results include all associated (parasitic and ESR) losses. The characterizations are performed with dies from typical process corner and at room temperature with a V_{BAT} = 1V as default biasing. The test-chip includes a buck-boost regulator to demonstrate the scalability of cascaded converter to generate multiple voltage domains.

Fig. 33(a) shows the all-electronic autonomous (battery-less) startup of the regulator, showing the converter bootstraps itself from 265mV at the output. The zoom in view of startup phase, in Fig. 33(b), shows the operation of the current limit protection scheme. Since the regulator is biased by its own generated output, the delay of the current limit

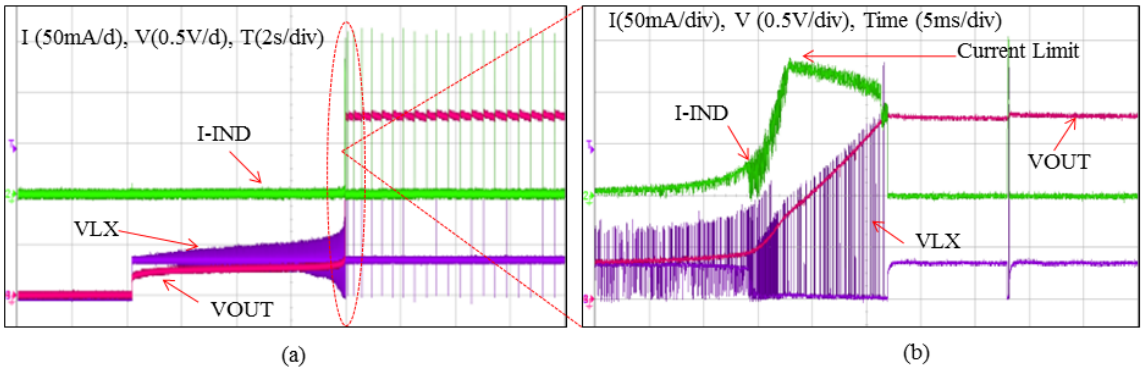


Figure 33: Operation waveforms (a) Autonomous (battery-less) startup with 265mV at output, (b) current limiting during start up event.

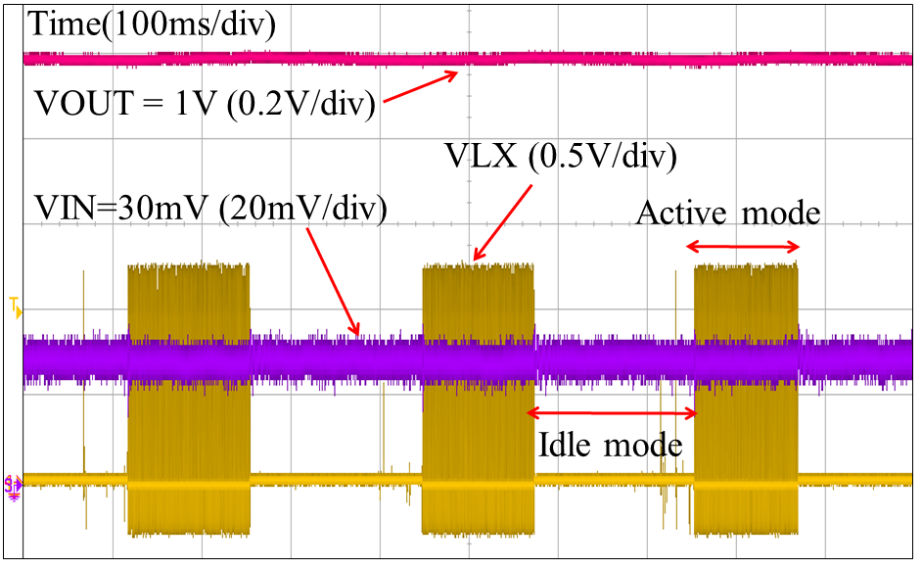


Figure 34: Activity during regulator operation. Clearly shown are active and idle regions. During active phase the regulator consumes bias current but while idle, bias current in selective blocks are gated (cut off) to improve efficiency.

circuit decreases with higher output voltage hence the threshold is seen to move slightly down-ward.

Fig. 34 shows a regulated output at 1V from 30mV input, delivering 10A while toggling between the idle and active modes. Fig. 35 shows the highest conversion ratio (62:1) operation while boosting from 50mV input to 3.1V output. Measured minimum VIN for boosting is 8mV, gen-erating a 0.45V unregulated output (not shown here). Fig. 36 shows the load regulation and Fig. 37 shows the line regulation characteristics. The measured

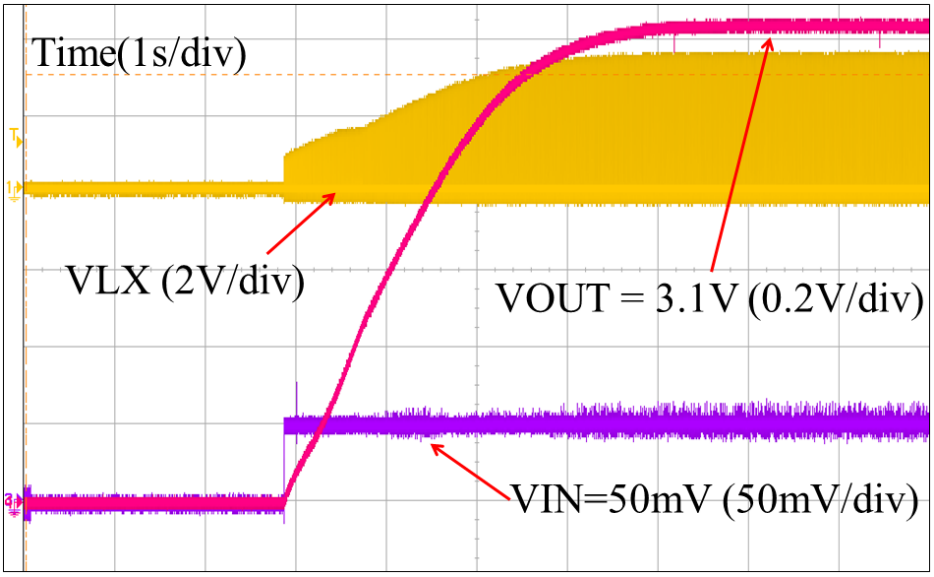


Figure 35: Operation from low input voltage. The regulator is able to generate 3.1V from 50mV input thus exhibiting 62x conversion ratio.

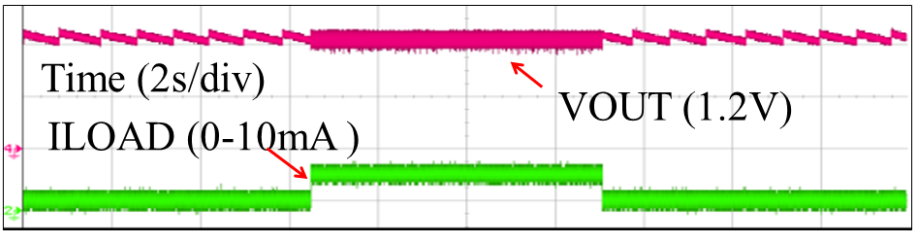


Figure 36: Load step response.

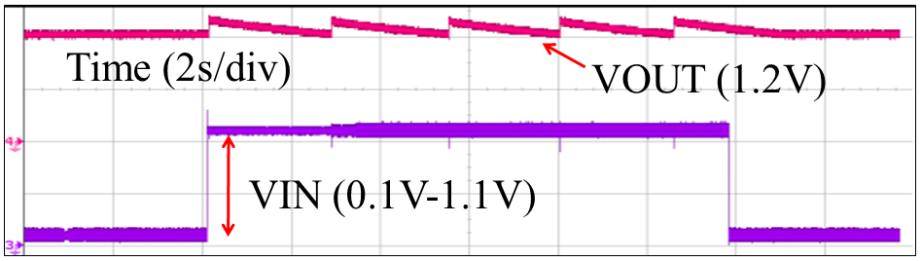


Figure 37: Input voltage step response.

maximum ripple (at highest input and lowest load) is 125mV.

5.5.1 Efficiency Measurement:

Fig. 38 shows the measured current consumption of the chip with different load. As expected the chip bias current increases with higher load current and higher conversion ratio

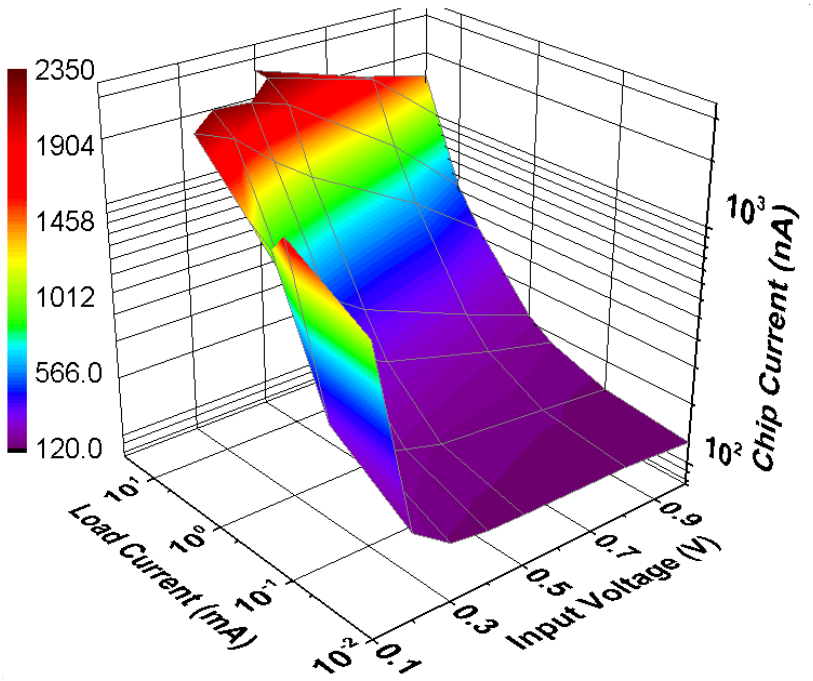


Figure 38: Bias current profile at different load current and input voltages.

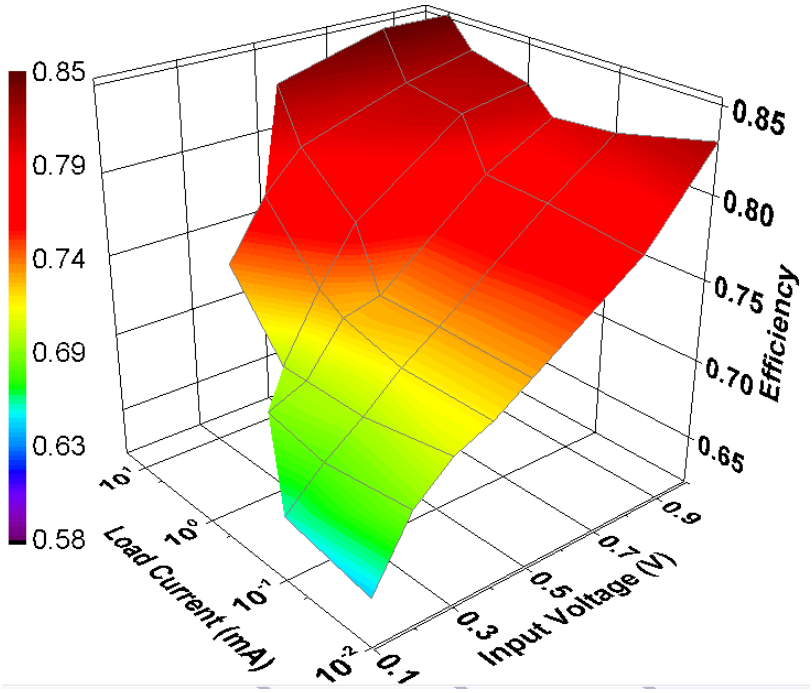


Figure 39: Efficiency profile at different load current and input voltages.

(more switching). With higher V_{SRC}, the measured minimum chip bias current at the lightest load is 120nA and increases to 2.2μA at maximum load. Fig. 39 shows the efficiency of

Table 3: Comparion chart of this work with prior arts

Item	Carlson JSSC10 [28]	Kadirvel ISSCC12 [34]	Ramadass JSSC11 [29]	Jong-Pil ISSCC12 [30]	This work
Min. VIN (w/ V_{OUT}=1V)	20mV	100mV	25mV	30mV	30mV
Min. self start	600mV	330mV	35mV[1]	40mV[2]	265mV
Bias current	1.1μA	150nA[3]	N/A	N/A	110nA[4]
V_{OUT}	1.4V	3V	1.8V	2V	0.78V-3.3V
Input range	20mV-250mV	100mV-V_{OUT}	25mV-V_{OUT}	50mV-V_{OUT}	30mV-V_{OUT}
Peak efficiency	0.75	0.92	0.6	0.61	0.85
Topology	Sync.	Sync.	Sync.	Async.	Sync.
Max Pout	175μW	~12mW	300μW	N/A	33mW
Process	0.13μm	N/A	0.35μm	0.13μm	0.13μm
Area	0.12mm^2	N/A	4.2mm^2	0.09mm^2	0.2mm^2

[1]Requires Motion Activated Sensor. [2]Requires Negative-VTH MOSFET.
[3]Total bias current is 330nA, the charger (boost) consumes 150nA.
[4]Total bias current in 110nA, the booster without V_{DD}_select is 80nA.

the converter (V_{OUT}=1.2V). The efficiency increases at high load current and lower conversion ratio. The measured peak efficiency is 89% with 10mA and 83% with 10μA of load current.

5.5.2 Performance Summary and Comparison:

Table 3 summarizes the characteristic and compares this work with other state of the art works. This work achieves 110nA bias current and 265mV all electronic startup. The bias gating technique helps to reduce the idle mode bias current by more than 20 fold as compared with the fully active non-bias gated condition.

5.6 Summary

The prototype chip presented in this chapter demonstrates the application of bias gating in reducing stand-by and operating power of a boost regulator. A PFM boost regulator with autonomous bias gating is presented where bias currents of selected analog circuit blocks are cut off during the output discharging phase to reduce standby current consumption. The demonstrated test-chip in 130nm CMOS achieves very small bias current (110nA at 1V) and maintains high efficiency across wide load, input, and output region. The maximum delivered peak output power is 33mW. The presented regulator is effective for energy harvesting systems such as wireless sensor nodes which exhibit long intervals of low-power mode but also moderately high peak power.

CHAPTER 6

CASCADED MULTI-STAGE BOOST REGULATOR

This chapter discusses different aspects of cascaded boost regulator system design including the effect of intermediate node on efficiency.

6.1 Introduction

Self-powered wireless sensor nodes operating with energy harvested from environmental sources are critical in various applications [9,14,46]. The advanced micro-scale transducers (e.g., Thermoelectric Generator (TEG) or Photovoltaic (PV) cells) can generate power in the order of ˜100μW from very low energy field; however, often produce very small output voltage in the range of 5mV-50mV [8]. Hence, to utilize the full potential of these DC transducers, boost regulators are required to generate usable voltage from the transducer output. The RF blocks in wireless sensor node pose intriguing challenges for the regulators. RF blocks are normally duty-cycled through active power state (during transmit/receive mode, most of the blocks are active, consume ∼10mW) and stand-by power state (only few of blocks are active during this period, consume ∼1-10μW) [13, 15, 16, 38–41, 52]. For improved energy efficiency, the regulator needs to be designed with order of magnitude lower biasing current than the standby current of the RF blocks. Further, the relatively high (∼3V) operating voltage of the RF blocks mandates high conversion ratio boost regulators for harvesting from very low voltage [28, 29, 34, 53] . For example, powering a 3V RF system from a 10mV input requires 300X conversion ratio, which is well beyond the capabilities of majority of the on-chip boost regulators. Additionally, high conversion ratio reduces the efficiency of the regulators [28, 53]. Therefore, methodologies to achieve very high (∼300X) conversion ratio and to improve efficiencies at high conversion ratios are of critical importance.

Majority of the reported boost regulators' [28–30, 34–37, 53–57] self-power consumption

fall in the same range (~1μA) of the standby power of the RF units; indicating the need for improvement. The conversion ratios are in the orders of 20-90 have also been reported [28–30, 34–36, 53, 54]. For example, Carlson et al. [28] reported a conversion ratio of 50 using a shift register based ring oscillator; Ramadass et al. [29] reported 1:72 boost ratio using on-chip clock generator; and Jong-Pil et al. [30] reported a conversion ratio of 30. Our separate work [58] presents a high duty cycle oscillator to achieve 1:63 conversion ratio in the boost converter. However, these prior designs do not simultaneously achieve sub-200nA bias current and > 100X conversion ratio.

6.2 Development of a cascaded two stage boost regulator system

This paper presents a boost regulator system for powering RF blocks through energy harvesting from low voltage DC transducers. The primary goals are to reduce the bias current and to reduce the operating input voltage range (i.e. to achieve higher conversion ratio). The key design innovations are stated below.

** A multi-stage boost regulator is presented where the first stage boosts the input voltage to an intermediate level, which is then boosted to the final target using the second stage. This innovation addresses the challenge of high conversion ratio to sustain 3V output from very low input voltage*

** The efficiency of the system is analyzed to show the superiority of the multi-stage regulation over a single-stage design for very high conversion ratio. An effective way to further improve the efficiency by optimally controlling the intermediate node voltage is presented.*

A test-chip for the multi-stage boost regulator is designed in 130nm CMOS. The measurement demonstrates regulated output of 3V (suitable for RF blocks) from as low as 10mV of input. The overall bias current of the multi-stage regulator is 190nA. The efficiency management with intermediate node control is verified through measurement showing 9% improvement in efficiency while harvesting from low (~100mV) input.

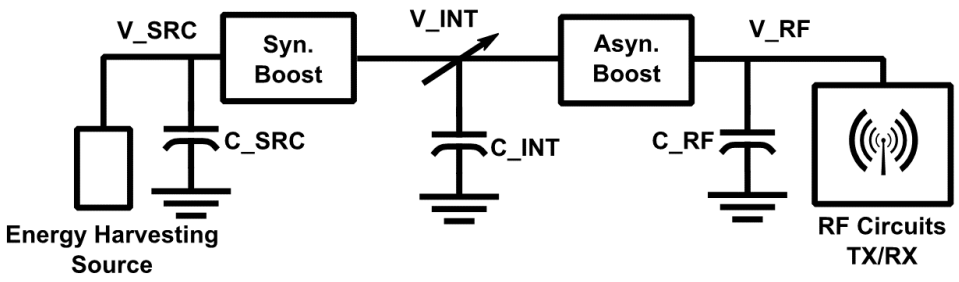


Figure 40: Proposed system block diagram showing variable intermediate node with cascaded boost to supply RF load.

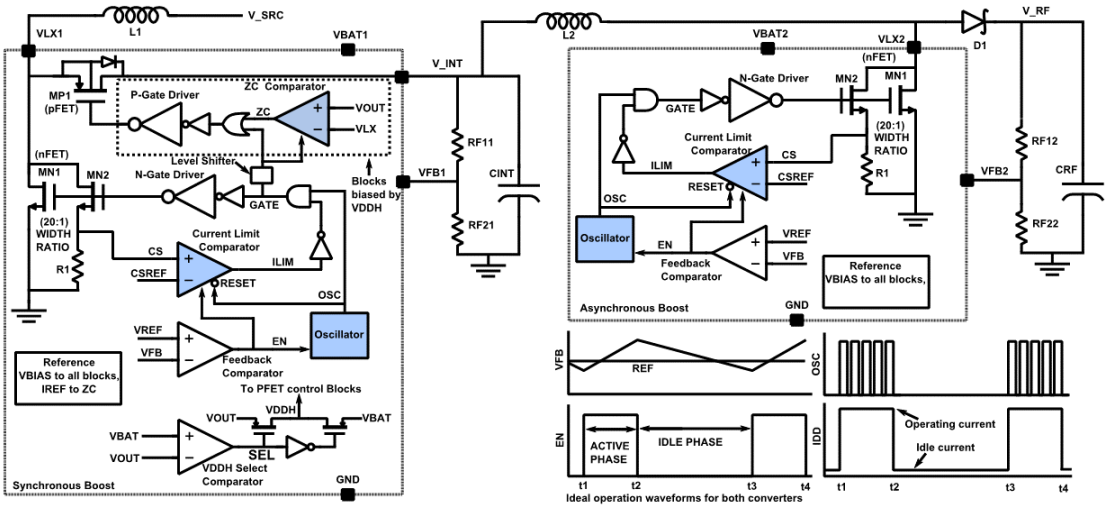


Figure 41: Block diagram of the cascaded system. Both synchronous and asynchronous stages are shown. Shaded blocks are bias gated.

6.3 System Architecture

Fig. 40 shows the functional block diagram of the system using two-stage cascaded boost regulators to generate the RF supply (V_{RF} = 3V. Generate up to 3.3V, limited by the technology) from a very low input. The design sustains the peak power for the standard transmission/reception (TX/RX) time of low-power trans-receivers [38,40,41,52]. The intermediate node voltage (V_{INT}) is modulated to control the efficiency. The boost stages are designed with pulse frequency modulation (PFM) architecture. The primary advantages of the PFM

over PWM are the reduction of the self-bias loss, especially during low load operations, and simpler analog control blocks. While the PWM mode converter keeps switching at all load conditions, the PFM mode skips pulses during low load conditions and by combining the bias-gating technique, the PFM topology becomes more efficient than the PWM topology in light-load conditions that this design is targeted for. In terms of transient response, the PFM produces first-order RC waveform while PWM generally has second or third-order response depending on the design of the compensation network. Consequently, the design of the PFM control is much simpler allowing lower power operation of the booster; however, the PWM designs' transient responses are usually faster (achieved through polo-zero compensation and other aided feedforward techniques) than those of the PFM designs. The first stage of this proposed system is designed using the synchronous topology (additional pFET switch and associated circuits) and the second stage is designed with asynchronous topology (external Schottky). The architecture is motivated by the current drive of the two stages. For a given load (I_{LOAD}) current the first stage drives a higher output current (I_{INT}), and hence, synchronous topology helps reduce the conduction loss. The conduction loss is less critical in the second stage as it drives less current and since the RF mostly remains in idle mode ($\sim$10s of μW of power). As the asynchronous topology eliminates the pFET switch, the switching loss (less gate drive) and bias current (simpler control circuit) are reduced.

Prior works on the multi-stage regulator for energy harvesting consisted of a first stage booster generating an unregulated intermediate voltage followed by a buck regulator supplying low-voltage ($\sim$1V) [34,35] where the minimum input voltage is limited by the maximum conversion ratio of the boost stage. In this proposed cascaded system, multiplication of conversion ratios of subsequent stages significantly extends the input range. Unlike the prior works where the intermediate node is left un-regulated (for the purpose of maximum power point tracking (MPPT), which is not included in this design), the proposed system regulates the intermediate node to optimally divide conversion ratio across two stages and

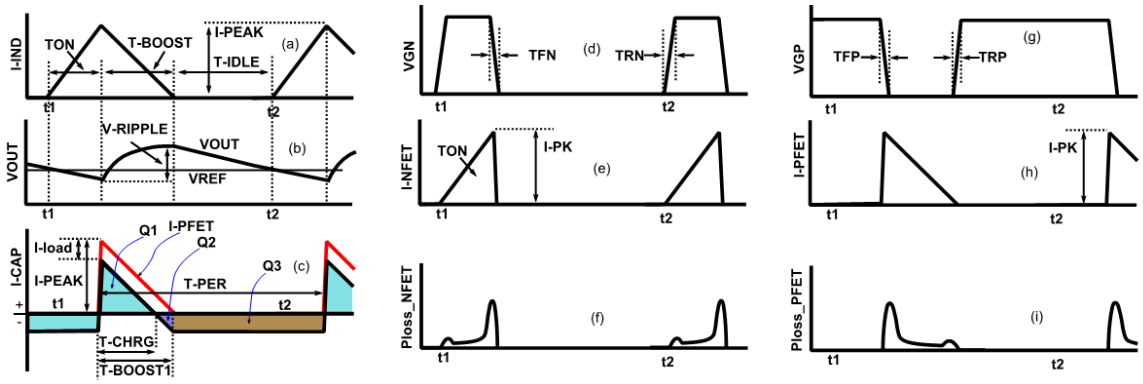


Figure 42: Different operation waveform and loss components for the PFM mode boost regulator running in single pulse discontinuous conduction mode (DCM).

improve the overall efficiency. It is possible to implement MPPT in this design, however because of the device breakdown issues the intermediate node has to be clamped at 3.3V in such implementation.

Fig. 41 shows the functional block diagram of the proposed cascaded regulator showing both asynchronous and synchronous PFM boost regulators [58,59] . The regulator can start-up and operate either with an external battery or a capacitor with stored energy connected to VBAT (battery assisted mode) or with VOUT connected to VBAT (self-powered or battery-less mode). The main power stage and drivers are designed with 3.3V devices to enable wide output range (0.78V to 3.3V). A VDD-Select Comparator circuit is designed that helps regulate output above the battery voltage. The control blocks are designed with low voltage (1.2V) devices to reduce area and bias power consumption.

6.4 Efficiency Analysis of the Cascaded System

To analyze the effect of conversion ratio on the cascaded system efficiency we develop a detailed model of the converter efficiency. For given input and inductor value, we first calculate the slopes (positive and negative) of the inductor current during two phases of boost operation,

$$m_{pos} = \frac{V_{IN}}{L_{IN}} \tag{21}$$

$$m_{neg} = \frac{V_{OUT} - V_{IN}}{L_{IN}} = \frac{V_{IN}}{L_{IN}} (k-1) = m_{pos}(k-1) \tag{22}$$

Where k is the conversion ratio (=V_{OUT}/V_{IN}). The peak current of the inductor at the end of oscillator on time (T_{ON}) is defined by,

$$I_{PEAK} = \frac{V_{IN}}{L_{IN}} T_{ON} = m_{pos} T_{ON} \tag{23}$$

Boost time is the time it takes for the inductor current to reach zero.

$$T_{BOOST} = \frac{I_{PEAK}}{m_{neg}} = \frac{T_{ON}}{(k-1)} \tag{24}$$

The inductor current pattern is shown in Fig. 42(a). To calculate the accurate timing related to charging time of the output capacitor, we refer to the charge flow details in the capacitor as shown in Fig. 42(c) .The charge flow in capacitor is divided by three regions; when the capacitor stores charge (Q1), when the current flow reverses (Q2), and when it is supplying the load (Q3). Note that the positive axis denotes the current going into the capacitor. The equation for reverse time is defined by

$$T_{REV} = \frac{I_{LOAD}}{m_{neg}} \tag{25}$$

The equation for charging time is then defined by

$$T_{CHRG} = T_{BOOST} - T_{REV} = \frac{I_{PEAK} - I_{LOAD}}{m_{neg}} \tag{26}$$

The ripple voltage (shown in Fig. 42(b) is created by the amount of the charge that gets stored in the capacitor. The average capacitor charging current during the charging time is defined by,

$$I_{CHRG} = \frac{I_{PEAK} - I_{LOAD}}{2} \tag{27}$$

And ripple voltage is then defined by,

$$\mathrm{V_{RIPPLE}} = \frac{I_{CHRG}}{C_{OUT}} T_{CHRG} = \frac{(I_{PEAK} - I_{LOAD})^2}{2\, C_{OUT}\, m_{neg}} = \frac{(I_{PEAK} - I_{LOAD})^2}{2\, C_{OUT}\, m_{pos}\, (k-1)} \tag{28}$$

$$T_{IDLE} = \frac{\mathrm{V_{RIPPLE}}}{I_{LOAD}} * C_{OUT} = \frac{(I_{PEAK} - I_{LOAD})^2}{2\, I_{LOAD}\, m_{pos}\, (k-1)} \tag{29}$$

Note that the idle time is the time when the converter is bias gated. The period of pulse repetition of the PFM converter is then the sum of the idle time, boost time and the on time of the oscillator

$$T_{PER} = T_{ON} + T_{BOOST} + T_{IDLE} \tag{30}$$

$$a = \frac{T_{ON} + T_{BOOST}}{T_{PER}} = \frac{T_{PER} - T_{IDLE}}{T_{PER}} \tag{31}$$

Where α is the top-level activity factor; and is the scaling factor that determines the biasing loss.

The dominant loss components of a switching regulator are hard switching losses in nFET and pFET, the resistive losses in nFET, pFET, inductor, and other combined series resistances in the traces and bond wires, parasitic capacitance charging losses in power FETs and other active devices, and bias loss of the chip.

Hard switching losses occur each time the power FETs turn-on or turn-off. Once the power FETs turn on, they incur resistive losses. Due to the inherent discontinuous nature of the current shape the losses during nFET turn-on and pFET turn-off are negligible and hence omitted (since current is approximately zero is these cases). The power loss profiles of the nFET and pFET are shown in Fig. 42(g),(i).

The equation for hard switching loss during nFET turn-off is adopted from [60] and is defined by the following equation,

$$P_{HSW\_N\_OFF} = \left\{ \left(\frac{V_{BAT} I_{PEAK}}{2} \right) T_1 + \left(\frac{(V_{OS} - V_{BAT})\, I_{PEAK}}{6} + \frac{V_{BAT} I_{PEAK}}{2} \right) T_2 \right\} \frac{1}{T_{PER}} \tag{32}$$

Where, V_{OS} is the overshoot of nFET gate voltage. The summation of nFET gate miller capacitor discharge time (T_1) and time for the device current to reach zero (T_2) is the total fall time of the nFET gate voltage T_{FN} (i.e., $T_{FN}=T_1+T_2$), as defined in [60].

The equation for hard switching loss during pFET turn-on is defined by the following equation, which can also be used for the Schottky diode turn-on loss.

$$P_{HSW\_P\_ON} = \frac{V_{OUT} T_{FP} I_{PEAK}}{6\, T_{PER}} = P_{HSW\_D\_ON} \tag{33}$$

Where T_{FP} is the fall time of the pFET gate voltage. The equations for conduction losses for power FETs' and the Schottky diode are calculated from the RMS current values flowing through the devices. The triangular shapes of the device currents shown in Fig. 42(e, h) help derive the following equations of the conduction losses,

$$P_{CON\_N} = I_{PEAK}{}^2 \left(\frac{T_{ON}}{3\, T_{PER}} \right) R_{DS\_N} \tag{34}$$

$$P_{CON\_P} = I_{PEAK}{}^2 \left(\frac{T_{BOOST}}{3\, T_{PER}} \right) R_{DS\_P} \tag{35}$$

$$P_{CON\_D} = \sqrt{\left(\frac{T_{BOOST}}{3\, T_{PER}} \right)}\, V_{FWD\_SCKY}\ \ I_{PEAK} \tag{36}$$

The equations for conduction losses due to inductor's series resistance is calculated by the RMS value of the triangular current shown in Fig. 42(a) and the ESR of the inductor, and is defined by,

$$P_{CON\_ESR\_L} = \ I_{PEAK}{}^2\, R_{ESR\_L} \left(\frac{T_{ON} + \ T_{BOOST}}{3\, T_{PER}} \right) = \ \frac{a}{3}\, I_{PEAK}{}^2\, R_{ESR\_L} \tag{37}$$

To calculate the ESR loss in the capacitor we fist calculated the combined RMS value of the current flowing through the ESR. Referring to Fig. 42(c), the combined RMS value is calculated from the values in the three regions and is defined by the following equation,

$$I_{RMS\_COUT}{}^2 = \ (\ I_{PEAK} - \ \ I_{LOAD})^2 \left(\frac{T_{CHRG}}{3\, T_{PER}} \right) + \ I_{LOAD}{}^2 \left(\frac{T_{REV}}{3\, T_{PER}} \right) + \ I_{LOAD}{}^2 \left(1 - \frac{T_{BOOST}}{T_{PER}} \right) \tag{38}$$

The RMS value of the capacitor is then used to calculate the resistive loss in the ESR of the capacitor,

$$P_{CON\_ESR\_C} = \ I_{RMS\_COUT}{}^2\, R_{ESR\_COUT} \tag{39}$$

The loss associated with active and idle mode bias consumptions are defined by,

$$P_{LOSS\_BIAS} = \left(\sqrt{a}\ \ I_{LOSS\_ACTIVE} \ + \sqrt{(1-a)}\ I_{LOSS\_IDLE} \right)\ V_{BAT} \tag{40}$$

Active mode loss comprises of active mode bias current and transistor switching losses while idle mode loss current comprises of idle mode bias current only

Each of the loss components are calculated for both synchronous and asynchronous cases (except for pFET loss for synchronous only and Schottky diode loss for asynchronous only), and summed up to find the total losses of each converters as expressed by the following equations.

$$P_{LOSS\_SYN} = P_{HSW\_N\_OFF\_SYN} + P_{HSW\_P\_ON\_SYN} + P_{CON\_N\_SYN} + P_{CON\_P\_ASYN} + P_{CON\_ESR\_L\_SYN} + P_{CON\_ESR\_C\_SYN} + P_{LOSS\_BIAS\_SYN} \tag{41}$$

$$P_{LOSS\_ASYN} = P_{HSW\_N\_OFF\_ASYN} + P_{HSW\_D\_ON\_ASYN} + P_{CON\_N\_ASYN} + P_{CON\_D\_ASYN} + P_{CON\_ESR\_L\_ASYN} + P_{CON\_ESR\_C\_ASYN} + P_{LOSS\_BIAS\_ASYN} \tag{42}$$

The individual stage losses are then used to find the corresponding stage efficiencies and these efficiencies are then multiplied to get the combined cascaded efficiency. This loss model is used to analyze the cascaded system with fixed total conversion ratio but variable intermediate node. Changing the intermediate node translates to conversion ratio change for both converters in opposite directions; i.e., increasing intermediate node translates to increasing conversion ratio for the first stage and decreasing conversion ratio for the second stage. Fig. 43 shows efficiency profiles of the individual converters as well as the two stage cascaded system. The peaking of the cascaded system efficiency profile indicates that the overall efficiency can be maximized by optimized control of the intermediate node voltage for two stage cascaded system. The efficiency profile for different input voltage are shown in Fig. 44. For a fixed output voltage, as the input voltage increases, the peak efficiency increases since the overall conversion ratio is decreasing. Also the peak point shifts to higher intermediate node voltage. Fig. 45 shows the combined cascaded efficiency as a function on conversion ratio. The efficiency profiles of the individual converter (synchronous and asynchronous) are also shown. The cascaded efficiency is found by multiplying efficiencies of the individual stages at any conversion ratio and by plotting the product at the square of that conversion ratio. For example, individual efficiencies at

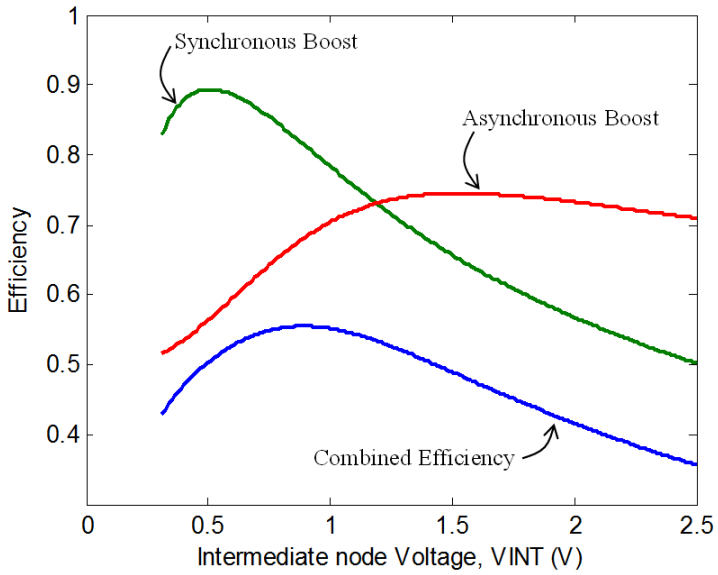


Figure 43: Effect of changing the intermediate node voltage on the cascade two-stage converter efficiency as found from the model. Also shown are the individual stage efficiencies.

conversion ratio 9 is used to found the cascaded conversion ratio at conversion ratio of 81. Being the product of the individual efficiencies, the cascaded efficiency starts lower at low conversion ratio but results higher efficiency at higher conversion ratio as compared with individual stages due to the quadratic increase of its overall conversion ratio.

6.5 Start-up and Stability

The boost regulator can be operated with or without external battery as explained in detail in [25, 26]. With an external biasing voltage of range 0.5-1.2V, it can boost from as low as 10mV input, because the internal circuit operation is independent of the input level in this condition. On the other hand, when starting up without the external battery, the system depends on the input voltage to bias itself; hence a higher input (minimum of 305mV) is required.

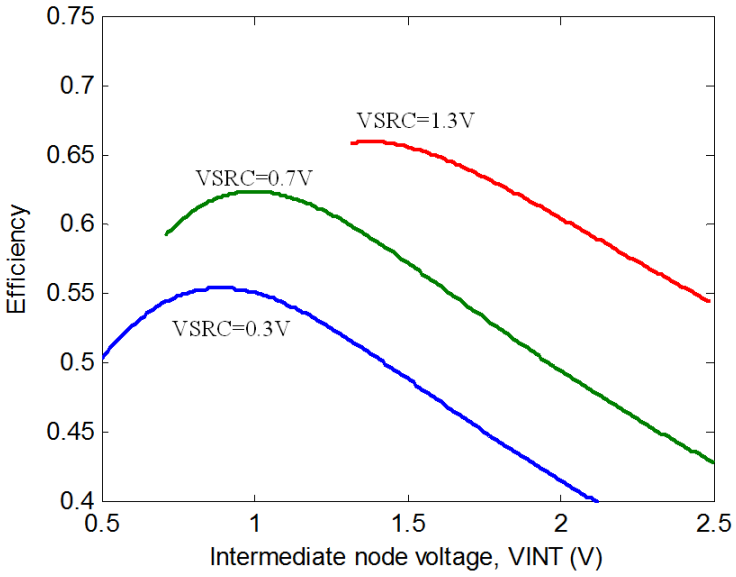


Figure 44: Effect of different input voltage on the combined efficiency as found from the model.

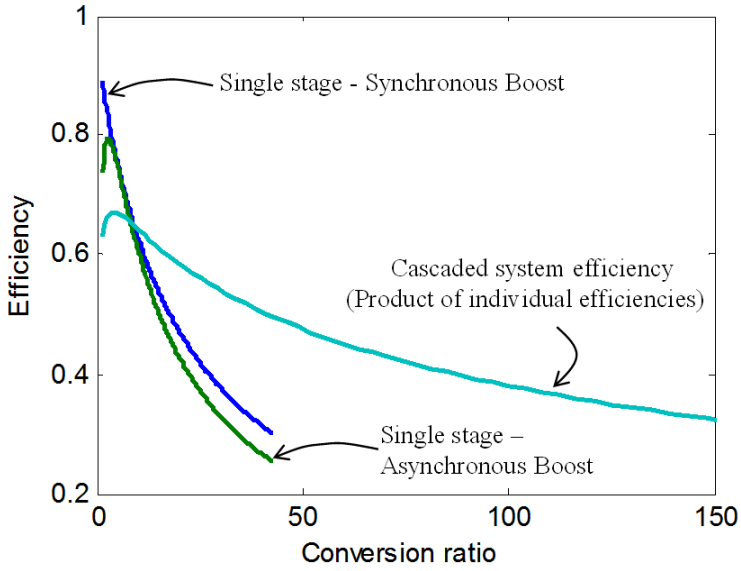


Figure 45: Cascaded stage efficiency as a function of conversion ratio, calculated from the model. Although generated from the product of individual efficiencies, cascaded system results better efficiency at higher conversion ratio due to the quadratic increase of its own conversion ratio.

6.5.1 Cascaded System Start-Up

In the cascaded configuration, during the startup of the second stage, the intermediate node voltage might be depleted to a low level due to the large inrush current flowing from the input to the output resulting in start-up failure. If the source voltage is high enough, the first converter can simultaneously transfer enough charge to the intermediate stage to prevent such failure. However, with a very low source voltage, this may not happen. To prevent such failure, at very low input voltage the second stage is turned on after the intermediate node has reached a minimum threshold. This sequenced start-up ensures that the inrush current of the second stage does not cause the intermediate node voltage to droop below the minimum required input voltage of the second stage. Therefore, the start-up of the proposed system are: (i) the *simultaneous startup* of the two stages when source voltage is higher than 150mV; and (ii) the *sequenced startup* for less than 150mV source voltage and the second stage is switched only after the V_{INT}>200mV. $C_{INT}$and C_{RF} are chosen to be 10mF and 100uF, respectively.

6.5.2 System Stability and Cross- Ripple

This design ensures that the system stability is not affected by the implementation of the bias gating or cascading multiple stages. For the single stage, the load pole, introduced by variable load (0 to 30mA) and output capacitor (100μF), varies from the origin to 50Hz. With the designed bias current, the feedback path, including the bond pad capacitance and delays of the FB, OSC and drivers, introduce another pole at ˜30 kHz. The bias gating in the OSC does not affect the pole location any further because with or without the bias gating, the circuit has the same delay (capacitors' initial conditions are same in both cases in of the oscillator). Since the second pole is far from the load pole, the transient stability is not affected and the converter behaves like a single pole system with the dominant load pole. For the cascaded system, we see that the each regulator feedback network controls its own loop only, hence there is no contention between the multiple loops and each regulator can be considered as isolated system. However, the output ripple of the first blocks appears as the

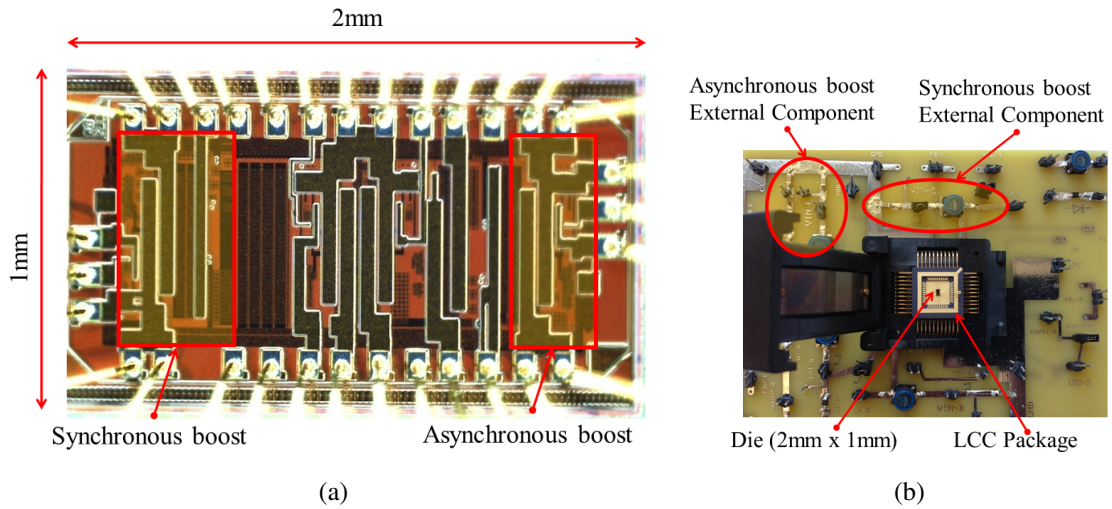


Figure 46: (a) Die (2mmx1mm) micrograph showing the two different boost circuits and (b) Board photo showing external components on the PCB.

input noise for the second stage. The switching noise is in the order of switching frequency or higher (100 kHz or more), and the inductors/capacitors used are 100μH/100μF; resulting an attenuation of -72dB at 100 kHz – hence the noise is well suppressed. For shared V_{DD}, the noise generated at V_{DD} is common to all regulators; i.e., noise generated by one regulator is seen by the others, however, this noise does not affect the regulation or stability of the system.

6.6 Measurement Results and Discussions

Fig. 46a shows the die-photo of the test chip. The cascaded configuration is achieved by externally connecting the synchronous and asynchronous boost regulators. The oscillation frequency of each converter is 100 kHz. The measured nFET and pFET resistances of the power stages are 400mΩ and 900mΩ, respectively. The test-board shown in Fig.46b is used to measure performance parameters of the packaged (LCC44) die mounted on a socket. Parasitic resistances include the board trace (in power loop) (20mΩ) and the socket resistance (25mΩ). External inductor (100μH, R_{ESR}=240mΩ) and input/output capacitors (both, 100μF, R_{ESR}=450mΩ) are used. All measurements are performed using the socket

and the board; hence results include all associated (parasitic and ESR) losses. Table III provides the summary of the performance parameters for the individual blocks in this system. The characterizations are performed with dies from typical process corner and at room temperature with a V_{BAT} = 1V as default biasing. The test-chip includes a buck-boost regulator to demonstrate the scalability of cascaded converter to generate multiple voltage domains.

6.6.1 Start-up and Transient Measurement

This chip demonstrates start up from 10mV input when biased by an external battery. Fig. 47 shows the startup of the single stage boost regulator generating 510mV from 10mV input. Fig. 48 shows the battery-less startup of boost regulator. From measured data, the minimum self-start input voltage is found to be 305mV (265mV at V_{OUT}). The switching events at V_{LX} node indicates the internal oscillator activity, and the as the oscillator keeps running the output builds up. The increasing output also acts as the biasing of the system. This positive feedback system keeps increasing V_{OUT} until it reaches the regulation point. Fig. 49 shows the cascaded system startup from 10mV. The intermediate node is started up as shown in Fig. 49 and once the V_{INT} is stabilized, the later stage is turned on. The building up of the final output is seen as well as the droop in the V_{INT} due to charge transfer. The charge is replenished eventually from the input which is not shown here. Fig. 50 shows the simultaneous startup of the cascaded system showing both voltage domains. The intermediate node voltage rises slower than the VRF due to higher output capacitance.

6.6.2 Efficiency Measurement

The efficiency of the cascaded system is measured at different input voltages (V_{SRC}) and at different V_{INT} levels and shown in Fig. 51. The peak efficiency point shifts to higher V_{INT} at higher input voltage. Fig. 52 shows the improvement of efficiency by varying the intermediate node as compared with a fixed (at 1.75V) intermediate node. The V_{INT} is varied to adjust the conversion ratios to find the peak efficiency point at every input voltage. As much as 9% efficiency improvement can be achieved at 300mV input voltage

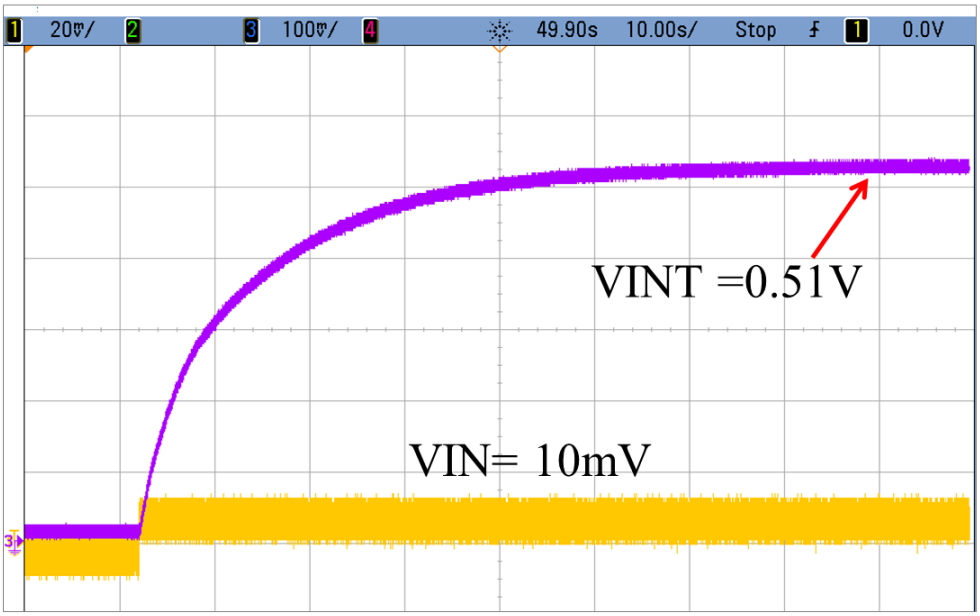


Figure 47: Single stage start up from 10mV input. The VDD is biased from a 1V battery.

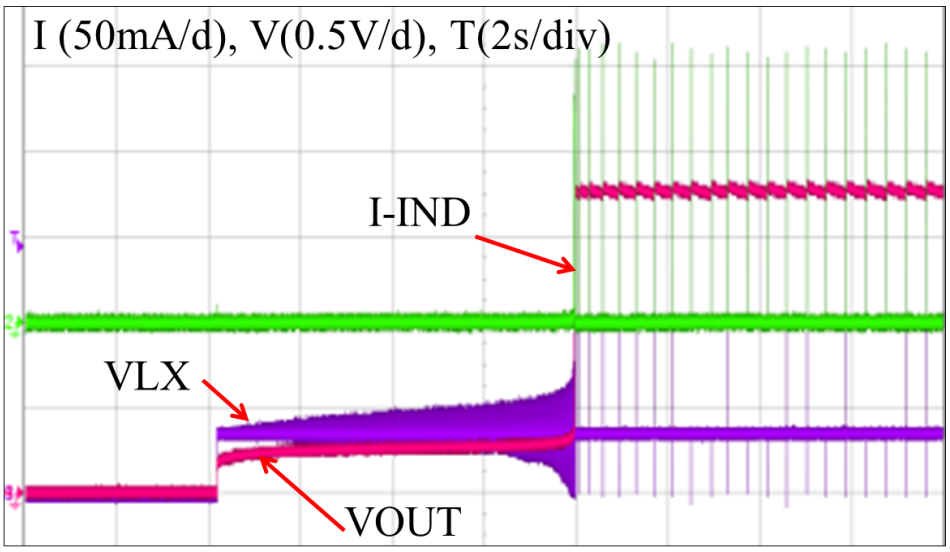


Figure 48: Single stage start up without any battery. The system is connected in boot-strapped and biases own VDD from the generated VOUT.

by adjusting the V_{INT}, as seen in the figure. The potential improvement, as compared with fixed V_{INT} increases as input is reduced further. Fig. 53 shows the efficiency of the cascaded converters at different load conditions. The efficiency is measured with a fixed output voltage and variable input voltages with continuous high (3mW), medium (1.5mW)

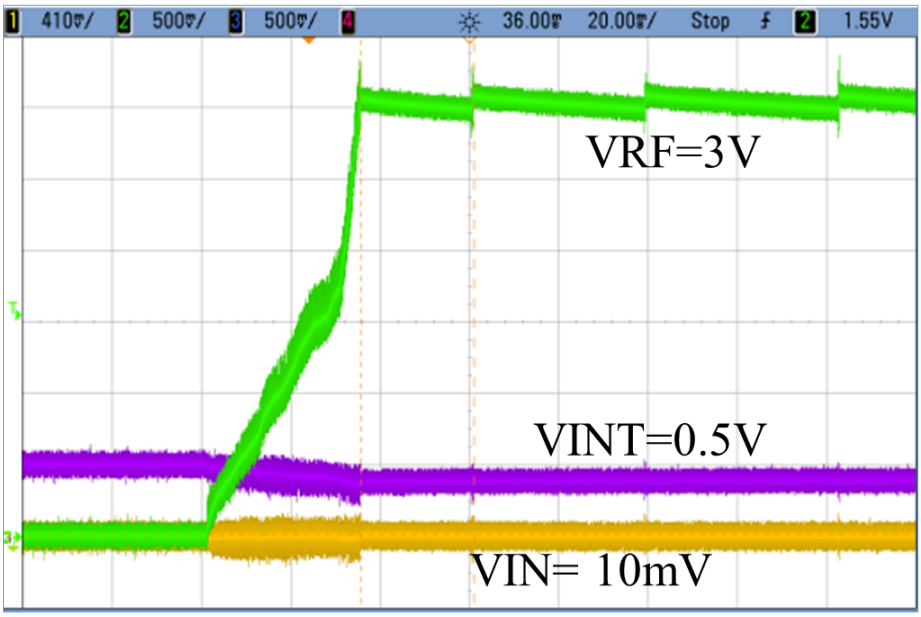


Figure 49: Cascaded start up where the 2nd stage starts up after 1st stage has already started. The system generated 3V at the 2nd stage output from 10mV input at the first stage input.

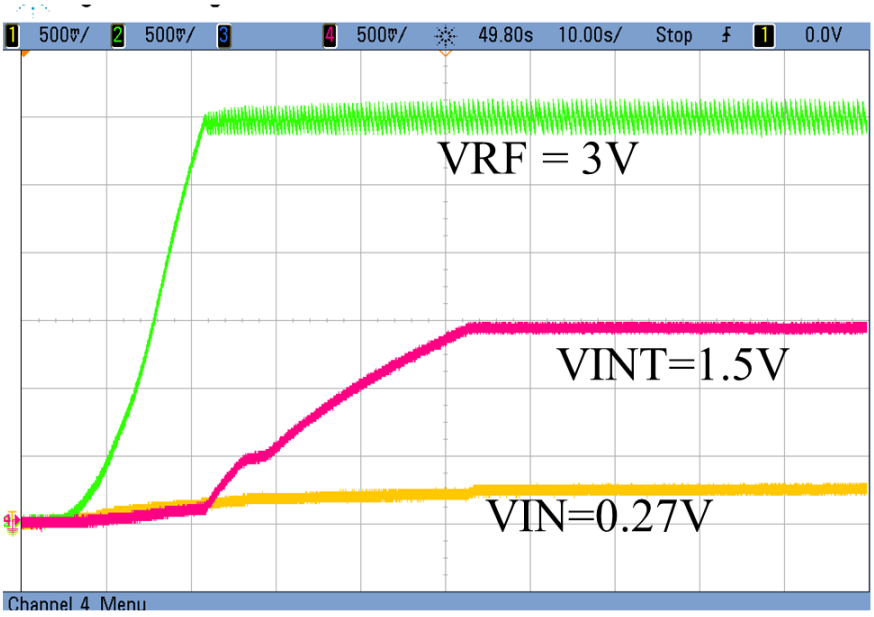


Figure 50: Cascaded start up with both stages start up simultaneously. Due to larger capacitance, the VINT rises slower than the VRF.

and low (0.1mW) load conditions. The intermediate node voltage is adjusted at each input voltage to maximize the efficiency at each conversion ratio.

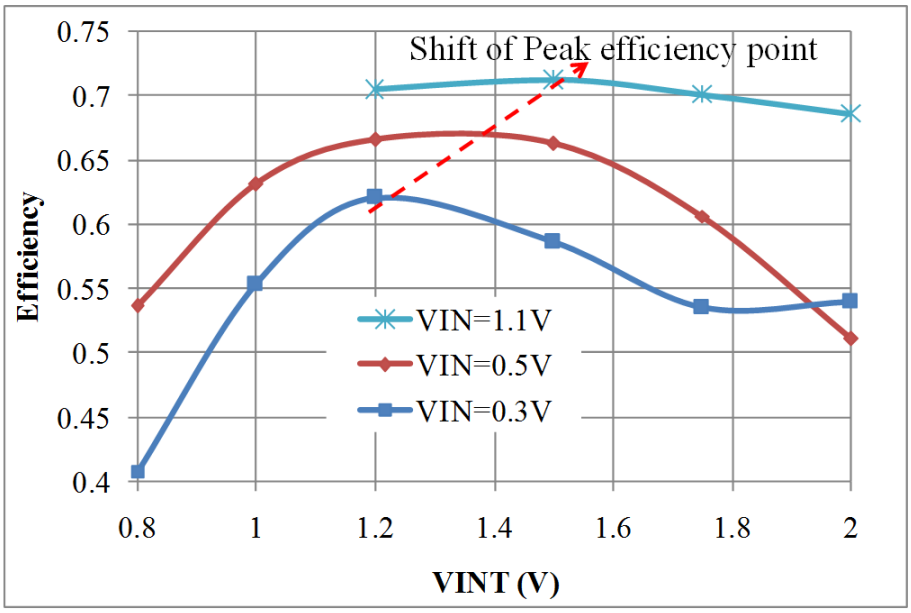


Figure 51: Measurement data showing the effect of intermediate node control on cascaded system efficiency.

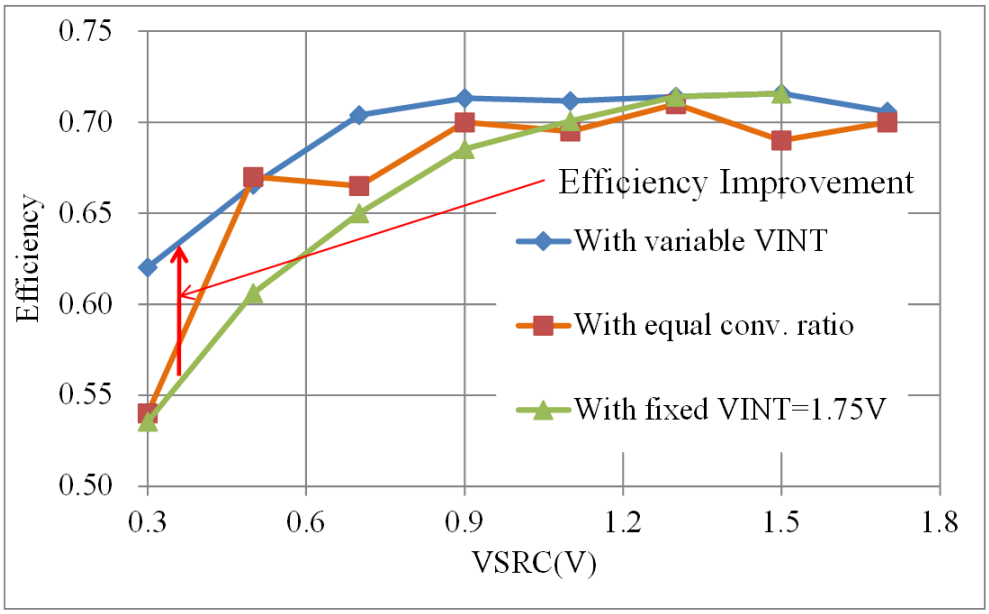


Figure 52: Measurement data showing the effect of fixed and variable (optimized) intermediate node voltage on cascaded system efficiency. Also shown is the efficiency profile for equal conversion ratio.

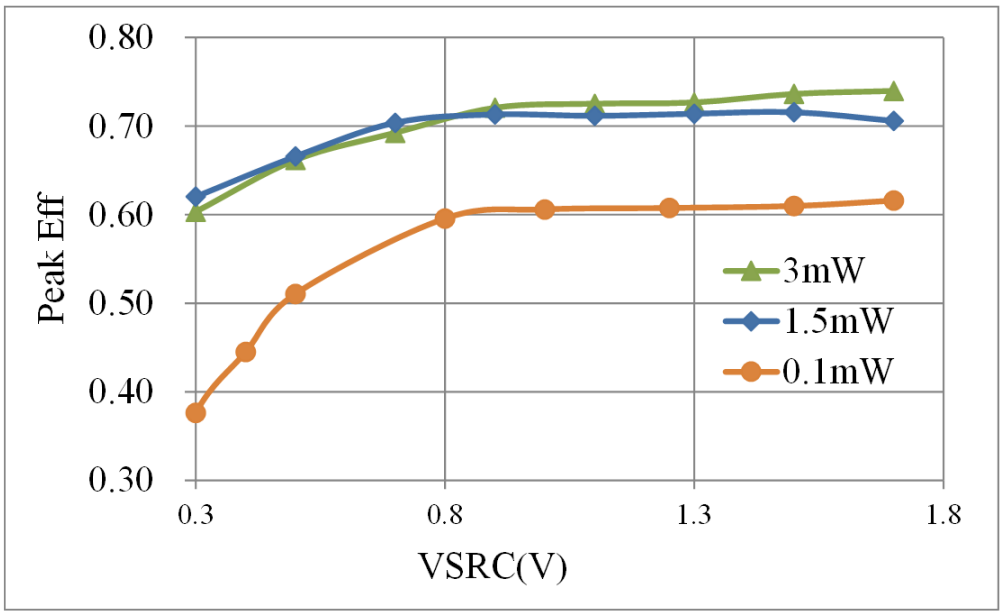


Figure 53: Measured efficiency profile of the cascaded system with different load

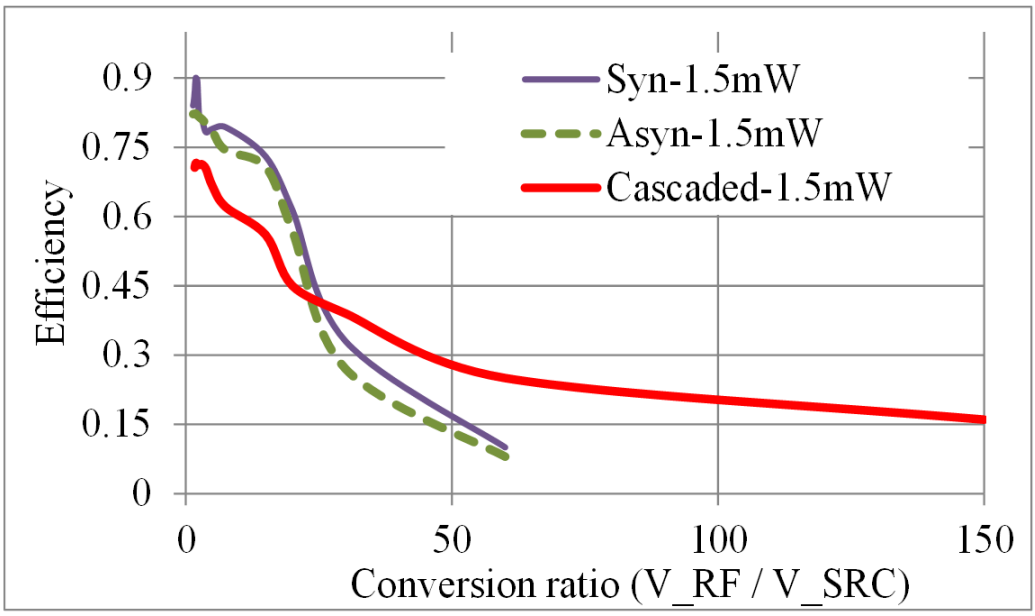


Figure 54: Measured efficiency profile of the cascaded system plotted as a function of the conversion ratio.

6.6.3 Transient Behavior

Fig. 55 shows the load transient behavior of the cascaded system. The system is subjected to a pulse RF load of 33mW. During the peak load, the intermediate node drops to accommodate for the lost charge which recovers once the load decreases. 33mW of RF power

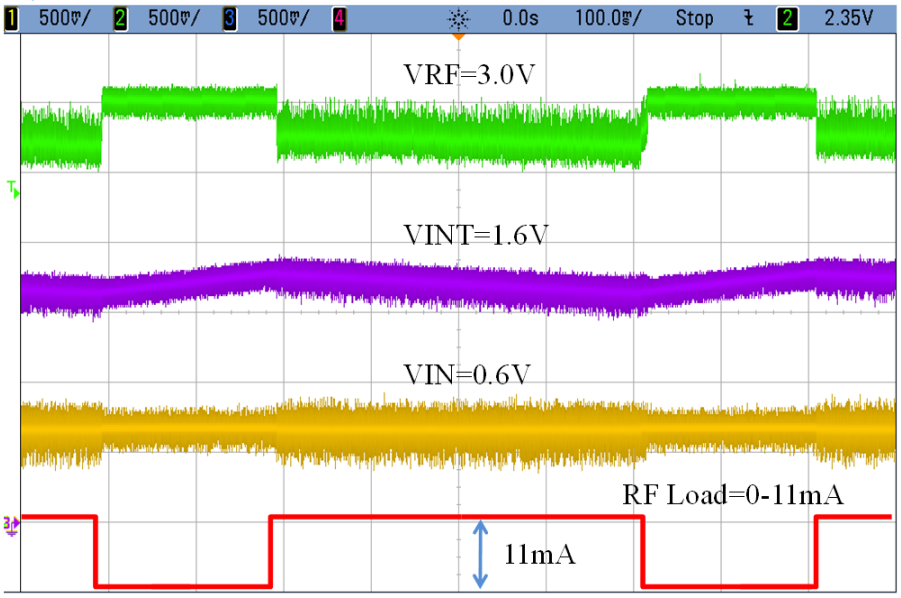


Figure 55: Measured RF pulse loading of the cascaded converter stage. From a relatively higher input voltage, burst RF loading up to 33mW can be delivered up to 400ms. During the high load condition, the intermediate node droops indicating charge depletion, however when the load decreases, VINT recovers.

allows reliable transmission for up to 20m with 1Mbps [40]. Fig. 56 shows a comparative view of the transient responses in cascaded dual stage converter and single stage converter. The input (0.4V) and output (2.3V) voltages are same for both systems. As seen in the figure, when a higher load is applied the converter goes to a more active state, having more ripple and more switching activities. Due to the increased load, the output capacitor discharges quickly and the feedback delay produces more ripple, however the peak of output voltage remains same. The single stage has more switching activity due to the fact that it's achieving the same conversion ratio with just one stage while the cascaded converter is achieving the same ratio in two stages. Except the switching activity change, there is no noticeable difference between the transient responses.

6.6.4 Performance Summary and Comparison

Table IV summarizes the characteristic and compares this work with other state of the art works. This work achieves conversion ratio of up to 300 and consumes only 190nA for the

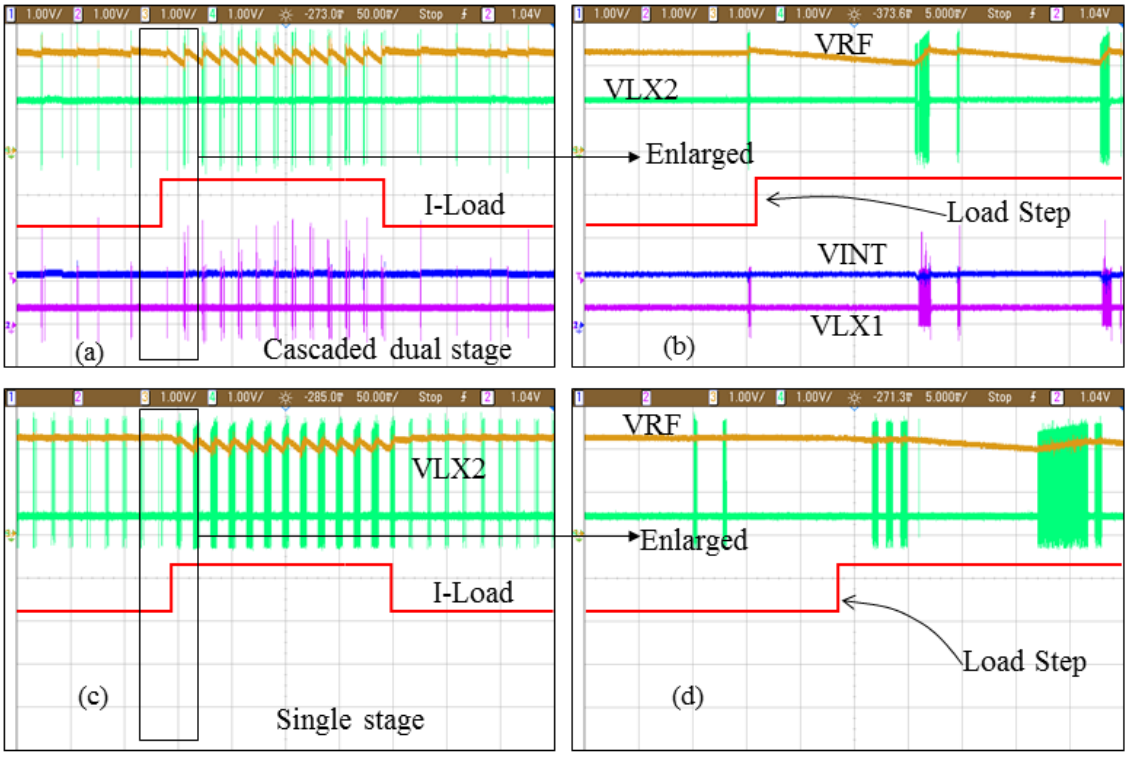


Figure 56: Measured comparison of load transient behaviors (30A-300A load step) of cascaded two stage boost regulator (a),(b) and single stage boost regulator (c),(d). The right side figures are the enlarged views of the marked portion of the left side figures. The input voltages are same for both system, hence the single stage goes through more switching activities. The ripple increases during higher load current both systems. The response patterns are similar in both conditions.

whole system, which is in par with isolated single stage converter. The synchronous boost regulator reaches peak efficiency of 89% while the cascaded system achieves a combined peak system efficiency of 72% (at V_{SRC} = 1.1V) and delivers up to 33mW of RF power. The system is capable of harvesting from 10mV input and autonomously operates from 265mV input voltage. The key achievements of the proposed design are ˜300X conversion ratio, 10mV input voltage, and 190nA bias current.

6.6.5 Future Work: Maximum Efficiency Tracking

Fig.54 shows the efficiency of the cascaded configuration (optimal point) along with standalone efficiencies of the first and second stage converter. The higher conversion ratio (50-150) is only achievable by the cascaded system and produces higher efficiency than single

Table 4: Comparison chart of this work with prior arts

Item	Carlson JSSC'10 [28]	Kadirvel ISSCC'12 [34]	Ramadass JSSC'11 [29]	Jong-Pil ISSCC'12 [30]	Bandyopadhyay JSSC'12 [54]	**This work**
Min. VSRC	20mV	100mV	25mV	30mV	20mV	**10mV**
Min. self start	600mV	330mV	35mV	40mV	N/A	**265mV**
Bias current	1.1μA	[a]150nA	N/A	N/A	N/A	[b]**190nA**
VOUT	1.4V	3V	1.8V	2V	1.8V	**0.78-3.3**
Conversion Ratio (Max.)	50	33	72	30	90	**300**
Peak efficiency	75%	92%	60%	61%	64%	**72%**
Min. VSRC	20mV	100mV	25mV	30mV	25mV	**10mV**
Max Pout	175μW	12mW	300μW	N/A	1.3mW	**33mW**
Process	0.13μm	N/A	0.35μm	0.13μm	0.35μm	**0.13μm**
Area	0.12mm^2	N/A	4.2mm^2	0.09mm^2	[c]25mm^2	0.62mm^2

[a]Total bias is 330nA. Boost reg. consume 150nA.
[b]Syn. Boost 110nA, Asyn. Boost 80nA.
[c]Total chip area. Active area is smaller.

stage. In the intermediate conversion ratio range (30-50) the cascaded system exhibits better efficiency than the individual systems. At low conversion ratio (1 to 30), however the cascaded system exhibits lower efficiency than single stage due to the efficiency multiplication of two stages. To harvest the benefit of the both the cascaded stages in high conversion ratio and singe stage at low conversion ratio, we propose a potential future extension of this work. A possible extension of this work is of the reconfigurable converter architecture to track the maximum efficiency using a single additional power transistor is shown in Fig.57. With an input voltage sensing circuit (shown as comparator), this transistor can be turned on (to bypass the second stage) when the source voltage is higher than a predefined low

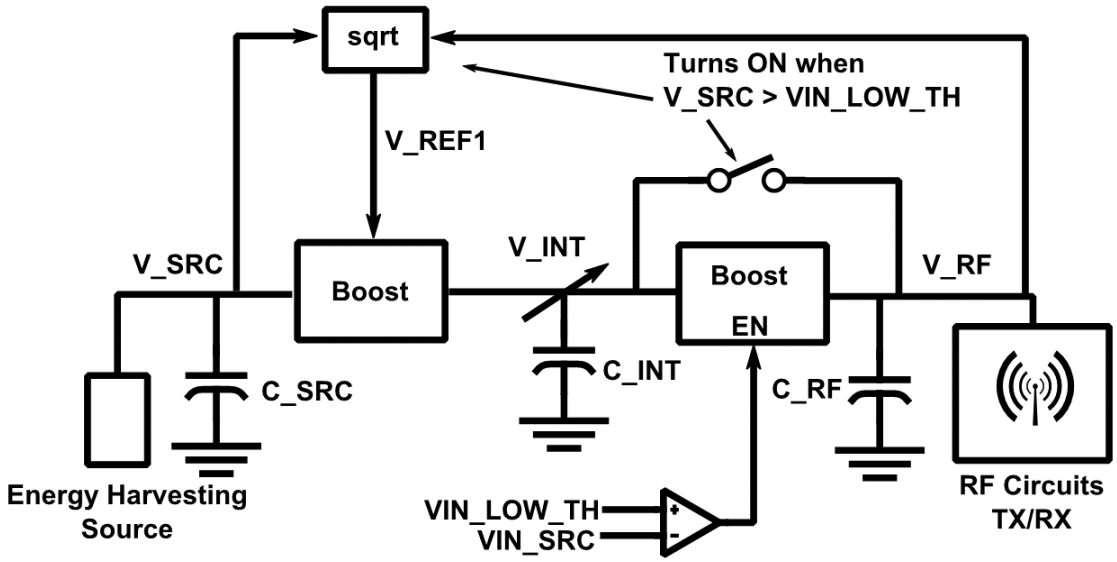


Figure 57: Future extension of the proposed cascaded converter to track maximum efficiency across varying conversion ratio. This is achieved by switching from the cascaded mode to single stage mode at lower conversion ratio (i.e. at higher input voltages). Additionally, in two stage cascaded configuration, VINT is dynamically regulated by a square-root circuit that divides the conversion ratio equally among two stages.

input voltage threshold to convert to a single stage system. The cross-over conversion ratio (above which the cascaded stage results higher efficiency) can be calculated offline or on-line using loss sensing. On the other hand, at lower input voltage, when the system is operating in two stage cascaded configuration, the V_{INT} is dynamically controlled to track the peak efficiency point by dividing the conversion ratio equally among two stages. The equal division of the conversion ratio is achieved by the square-root circuit that produces the reference voltage (V_{REF1}) for the first stage boost regulator. The value of V_{REF1} is the square root of the product of the source (V_{SRC}) and output (V_{RF}) voltages. As shown in Fig. 57, when V_{INT} is controlled at the square root value of the product of input-output voltages, the resulting efficiency follows closely with the condition when V_{INT} is optimized at every point. While the square-root method may not provide maximum efficiency at all points, this technique can be used for the ease of design complexity as opposed to online peak efficiency point tracking operation where V_{INT} needs to be optimized at every point.

6.7 Summary

This chapter presents circuit design and system control techniques to design boost regulator with very low bias current and high conversion ratio. The high conversion ratio is achieved using cascaded PFM boost regulator stages where each stage is designed with an innovative high-duty cycle oscillator to achieve high conversion ratio. A circuit technique, namely, autonomous bias gating is presented to reduce the bias current of the PFM boost stages. The bias gating conditionally cuts down bias current of selected analog blocks without sacrificing performance. The concept of intermediate node control is demonstrated to improve efficiency of the cascaded converters by optimally distributing the conversion ratio between the cascaded stages. The test-chip demonstrates a two stage cascaded boost converter with 190nA bias current and capable of harvesting from 10mV input voltage to generate up to 3V to supply RF blocks in WSN applications. The proposed boost regulator couples the circuit techniques for efficient design of individual stages with system level control of the cascaded stages. The presented design methodologies are useful for converters requiring very high conversion ratio while supplying intermittent load currents. Such converters can harvest from photovoltaic cell, thermoelectric generator or other non-oscillatory energy transducers and power remote wireless sensor node electronics.

CHAPTER 7

CASCADED MULTI-STAGE BOOST REGULATOR WITH A SINGLE INDUCTOR

This chapter discusses a single-inductor-cascaded-stage topology for boost regulator that time-multiplexes a single inductor to achieve multi-stage regulation.

7.1 Introduction

High conversion ratio boost regulators are crucial for self-powered electronics to harvest energy from very low input voltages [28–30, 34, 61]. Prior works rely on duty-cycle control of the on-chip digital [28, 34] or analog oscillators [58] to achieve high conversion ratio. Due to design complexity and challenges in creating very high duty oscillators, reported conversion ratios are limited to less than 75x [28–30, 34, 58, 61] . Alternative approaches of cascading multiple regulators can achieve higher conversion, but requires multiple inductors increasing system's footprint.

The design presented in this chapter achieves higher (120x) conversion ratio using a lower duty cycle (~60x) oscillator. The key design innovation is to time-multiplex a single inductor using one-nFET-two-pFET power stage to achieve higher conversion ratio. Additionally, use of the autonomous bias gating in Pulse-Frequency Modulation (PFM) mode regulator minimizes the self-power consumption and improves efficiency.

7.2 System Architecture and Circuit Design

7.2.1 Architecture

Fig. 58(a) shows the architecture of the proposed regulator. The inductor and the capacitors are external while all other devices are on chip. The system boost from V_{SRC} to V_{OUT} through the intermediate node V_{INT}. The control circuit operates the transmission gates ($XG_{1,2}$) to alternately boost from source voltage (V_{SRC}) to the intermediate voltage (V_{INT}, controlled by MP_1) and then from V_{INT} to the final output (V_{OUT}, controlled by MP_2).

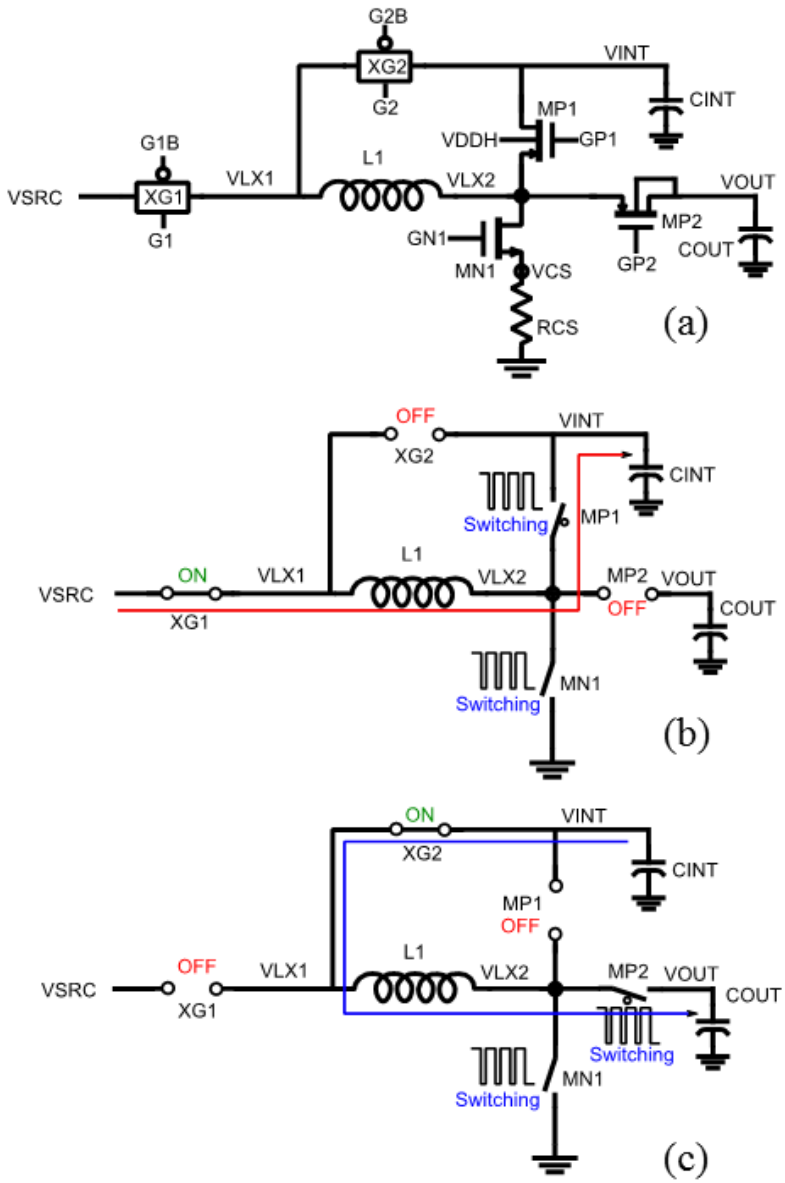


Figure 58: (a) Proposed regulator with key elements shown, (b) V_{INT} charging phase (Phase 1) and (c) V_{OUT} charging phase (Phase 2). Arrow indicates the direction of the energy flow in each phase of operation.

Different switch configurations during the V_{INT} charging phase (phase 1) are shown in Fig. 58(b) while, Fig. 58(c) shows the switch settings during the V_{OUT} charging phase (phase 2). The inductor and the nFET switch MN_1 are similar to a regular boost regulator and are used in time-multiplexed way in both phases of operations. Instead of a single pFET switch as in a conventional boost regulator, this proposed design has two pFET switches ($MP_{1,2}$)

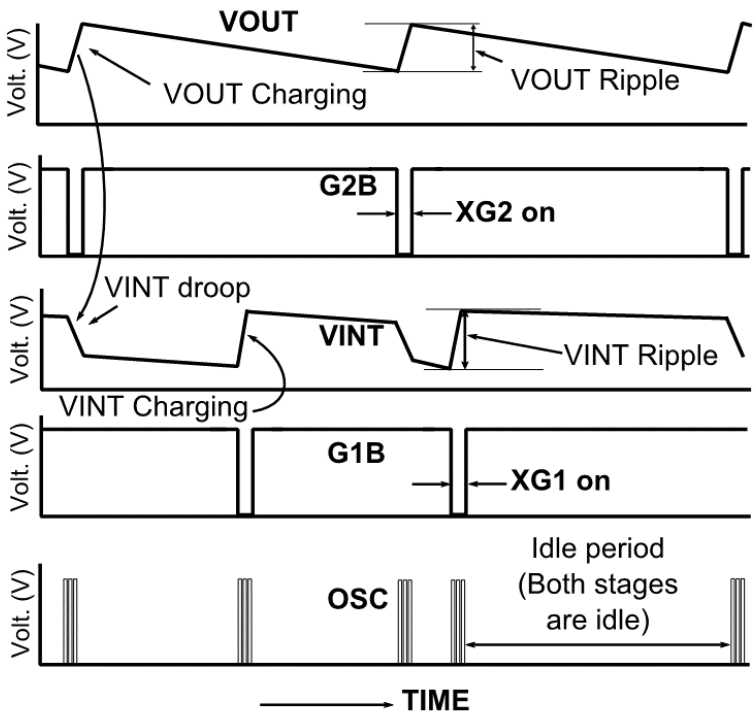


Figure 59: Ideal operation with key waveforms.

to isolate the intermediate node from the final output.

7.2.2 Operation Principle

Fig. 59 shows ideal waveforms of the regulator operation. Both V_{INT} and V_{OUT} are set to regulate autonomously. These are monitored through the feedback sensors and charging is activated when they fall below the corresponding regulation levels (when XG_1 and XG_2 are turned on). During the energy transfer from V_{INT} to V_{OUT}, the V_{INT} undergoes droop (shown in Fig. 59) while at other time the V_{INT} discharges due to finite leakage current at that node. It is worth noting that V_{INT} is not supplying any additional load. The PFM control uses a single oscillator to enable the multi-phase operation. The oscillator activity resembles overall system activity profile.

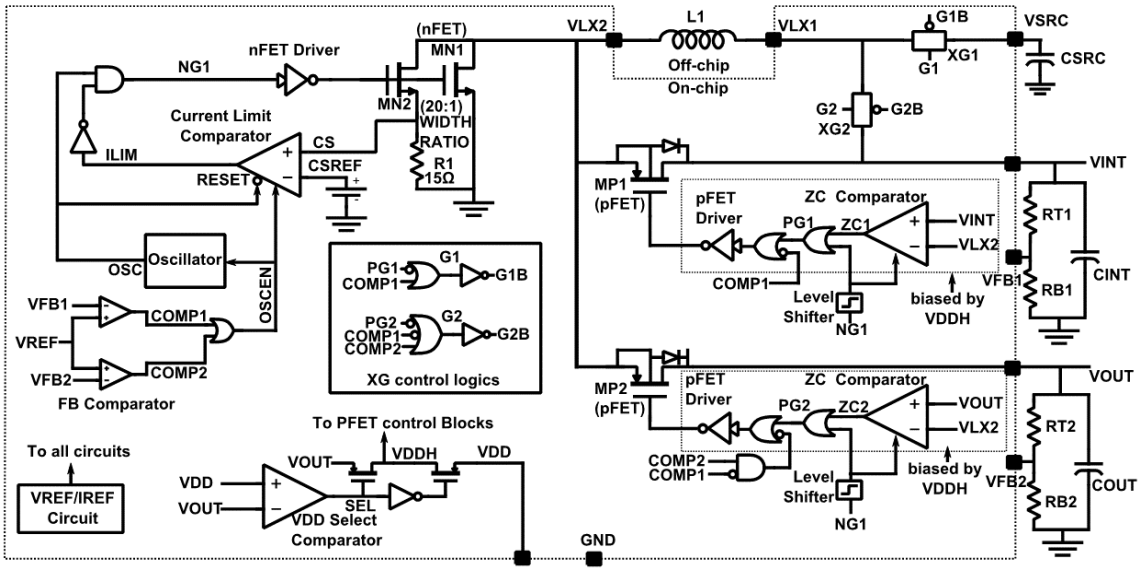


Figure 60: Block diagram of the proposed boost regulator.

7.2.3 Block Diagram

Fig. 60 shows the complete block diagram of the regulator. The regulator consists of two feedback comparators, comparing V_{INT} and V_{OUT} (through externally sensed feedback signals, $V_{FB1,2}$) with the internal reference (V_{REF}). The outputs of the comparators are used to generate the OSCEN signal which enables the high duty (98.4%) cycle oscillator. The oscillator (OSC) and the current limit (ILIM) signals create the nFET gate signal (NG_1). The NG_1 and zero current ($ZC_{1,2}$) detection signals generate gate drives for switches $MP_{1,2}$. Switch MP_1 is enabled when $COMP_1$ is high; but switch MP_2 is enabled only when $COMP_1$ is low and $COMP_2$ is high, ensuring the priority of charging V_{INT} before V_{OUT}. The transmission gates, the power FET logics, and the drivers are biased from the highest voltage (V_{DDH}) of the system generated by an internal V_{DD_SEL} circuit by hot-swapping the higher of the two voltage rails (V_{DD} and V_{OUT}). During the inductor current discharge phase of the boost operation, the ZC comparators turn off the pFETs, preventing reverse current. Separate ZC circuits are used for MP_1 and MP_2.

7.3 Key Design Challenges

The proposed regulator behaves as a cascaded two stage boost regulator however since only one inductor is used, the 'time-multiplexing' brings out several design challenges for this topology. This subsection discusses the design challenges and techniques to overcome those.

Transmission gate management: The transmission gates, XG_1 and XG_2 are turned on alternately during first and second phases of operation, respectively. Due to the inherent asynchronous nature of the comparators' output, the transmission gates might turn off before the inductor current reaches zero, letting current flow through the body-diodes of $XG_{1,2}$; thereby reducing the efficiency and injecting substrate noises. To prevent these adverse effects, the transmission gates are turned off only after the inductor current has reached zero. The zero current comparator (discussed in sub-section *E*) senses the zero crossing of the inductor current and is embedded in pFET gate signals ($PG_{1,2}$). These signals are directly used to control the transmission gates which turns off only after the zero crossing event is detected.

Inductor usage priority management: The shared inductor requires a priority assignment and management for the individual power stages. In 'phase-1' the inductor is used to transfer charge from the C_{SRC} to C_{INT} (initial transfer) while in 'phase-2' the inductor transfers charge from C_{INT} to C_{OUT} (final transfer). Since the final transfer is only useful when the C_{INT} is properly charged, the initial transfer is given higher priority for the inductor usage. This also manages the start-up condition since C_{INT} must be charged before the C_{OUT} in order for C_{OUT} to receive any charge from C_{INT}. The priority is managed by the combinational logics whose outputs generate G1/G1B and G2/G2B as shown in Fig.3.

7.4 Key Circuit Blocks

Two feedback comparators, one for each phase, are designed with 50mV hysteresis. A single V_{REF} circuit generates a voltage independent bias current and a VBE based voltage

reference. A single oscillator is used and is designed with two symmetrical capacitive charging circuit with constant bias current. These aforementioned circuits are presented in [58]. A single current limit circuit is used with the inductor to sense the inductor current when the nFET is on and truncates the nFET on-time if the current exceed 100mA. A zero current (ZC) detection circuit is shown in Chapter 5 Fig. 30 . The circuit is active when the nFET signal GATE is low, which turns on the switches SP_{1-3} and turns off SP_4. The circuit works a common gate amplifier with two input signals (potential at LX and V_{OUT} nodes). As the current through the pFET decreases, the LX node goes below V_{OUT} and zero current is detected (ZC goes high). This turns off the pFET and also toggles the switches SP_{1-4}, thereby cutting the current through current mirrors M_{2-4}. This condition prevails remained enforced throughout the idle time. To reduce the wake up settling time of the circuit, the diode-connected nFET M_1 is kept on which constitutes the only bias consumption during the idle time for this block.

7.5 Bias Gating

When the output of a phase rises above the regulation level, the corresponding feedback comparator goes low putting that phase into its idle mode. The idle modes of the phases overlap when both outputs are above regulation levels. The idle times are utilized to cut the bias current of selective blocks (bias gating) and reduce self-power consumption [58]. The feedback comparator circuit, reference generator and the V_{DD_SEL} circuits are not bias gated. The bias gating is applied to oscillator, current limit comparator, and zero current circuits. These circuits run on high bias current and performance when making decisions while saving power when idle. The bias gating is realized using activity of individual phases and the system. The current limit circuit and the oscillator are used in both phases, hence are bias gated only when both phases are idle. The zero current detection circuits are dedicated, hence circuit is active only when the corresponding pFET remains on, and is bias gated at all other times. The settling times for all blocks are designed to ensure fast

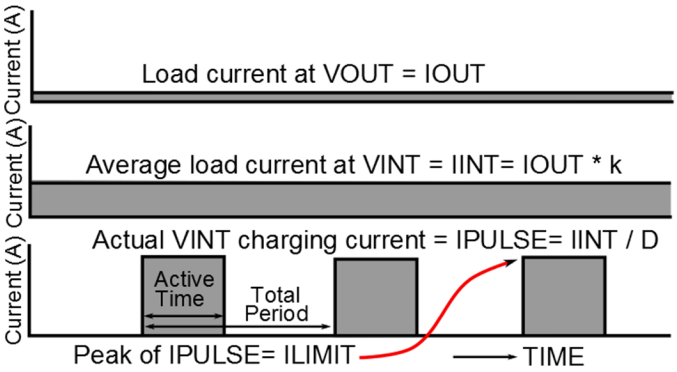
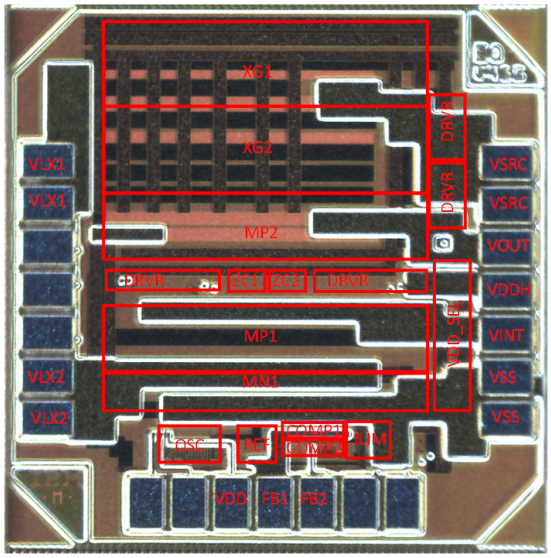


Figure 61: Effect of load current on the output current of the first phase. Here, $k = V_{INT}/V_{OUT}$, and D is the duty ratio (active time to total period)..



Parameter	Value
Die size	1mm x 1mm (Active area = 0.6mm x 0.7mm)
Max. Bias current (Full switching)	5.2µA (Idle bias current = 140nA)
ILIM threshold	100mA
ZC threshold	5mA
OSC frequency	100KHz
Input capacitor (at VSRC)	100µF
Inductor	100µH
CINT	1000µF
COUT	100µF
MN1 R_{DSON}	400mΩ
MP1/MP2 R_{DSON}	400mΩ
XG1/XG2 R_{DSON}	200mΩ

Figure 62: Die photo and key parameters.

decision-making after waking up.

7.6 Stability

The two operational phases of this design work in time-multiplexed way. Hence, in each phase the system can be viewed as an isolated PFM mode regulator running in discontinuous conduction mode (DCM). A DCM system has two poles and one zero whose locations depend on the load current, input and output voltages, output capacitor and the inductor [62]. The load pole dominates such a system. Hence, the output current (I_{OUT}) determines the dominant pole of the second phase. The average load current of the first

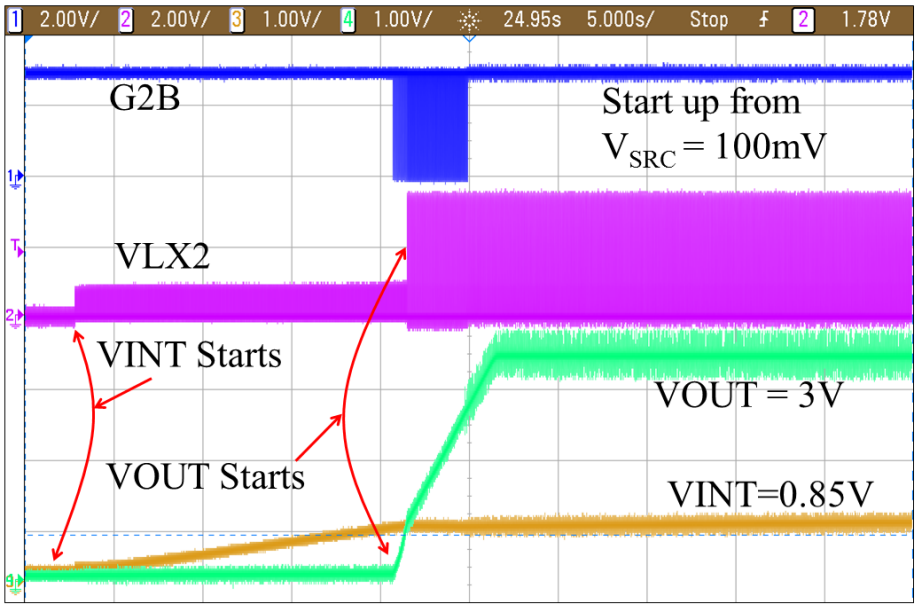


Figure 63: Start up from 100mV input.

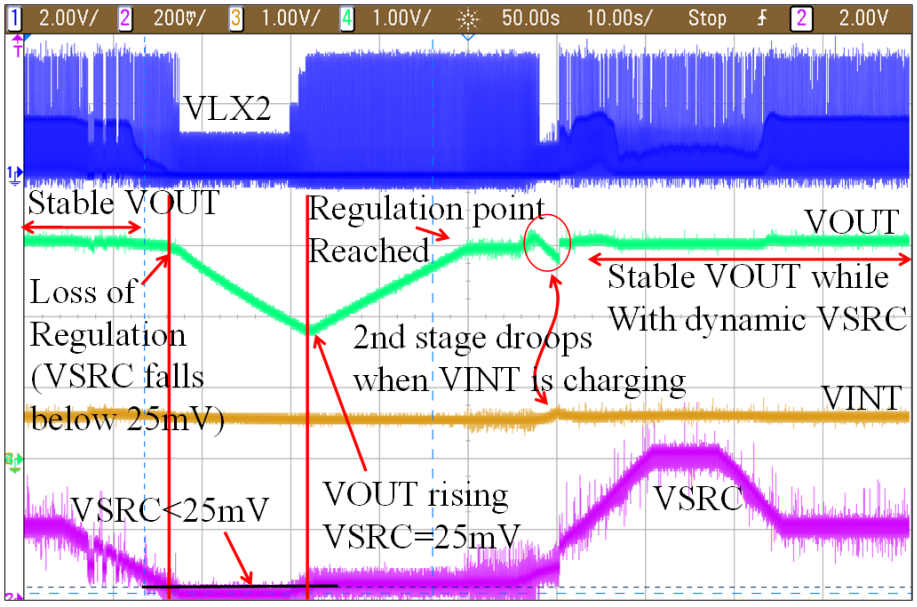


Figure 64: Operation with dynamic source voltage.

phase is higher due to the voltage boost factor [I_{INT}=I_{OUT}×(V_{OUT}/V_{INT})] (shown in Fig. 61). To deliver the average current I_{INT}, the first phase experiences a pulsating current with peak as: I_{PULSE}=I_{INT}/D= I_{OUT}×(V_{OUT}/V_{INT})/D, where, D (duty ratio) is the ratio of active time to total period (shown in Fig. 61). However, the maximum allowed current is limited to a predefined threshold, I_{LIMIT} by design. Therefore, given a load current, the first phase's

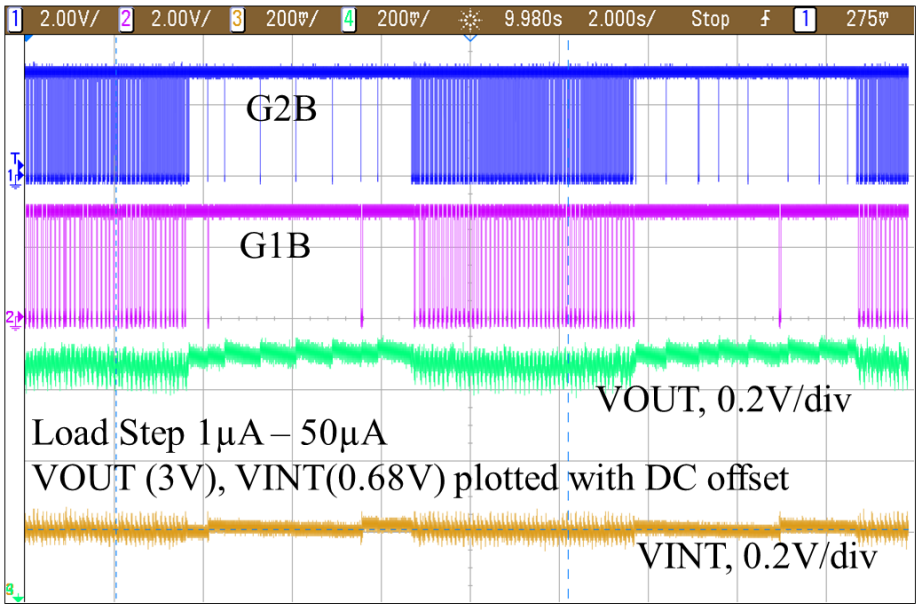


Figure 65: Load regulation performance of the regulator. The activity pattern change with load; the activity increases as the load is applied and decreases when the load is removed.

dominant pole is determined by either the I_{PULSE} or I_{LIMIT} whichever is lower. For example,, in a typical operation with V_{SRC}=50mV, V_{INT}=500mV and V_{OUT}=3V with 50μA load current, the ESR values shown in Fig. 6, and I_{LIMIT} of 100mA, the calculated pole-zero are: in Phase 2, p_1=0.3Hz (load, C_{OUT}, Conv. ratio), p_2=2.3MHz (ESR_{COUT}, duty ratio, Conv. ratio) and z_1=210KHz (ESR_{COUT}, duty ratio) and, in phase 1, p_1=70Hz, p_2=2.3MHz and z_1=210KHz. As expected, in each phase the poles are separated far apart and hence in each phase the regulator behaves as a single pole system with p_1 as the dominant pole. The time multiplexing ensures the poles of the two phases do not interact with each other and the system exhibits a single pole behavior.

7.7 Measurement Results

The chip is fabricated in 130nm CMOS. Measurements are performed in typical conditions (room temperature and V_{DD}=1V, V_{DDH}=3V) and include the parasitic losses of the PCB, socket (PLCC), and package (LCC28). The die photo is shown in Fig. 62 along with the key internal and external parameters.

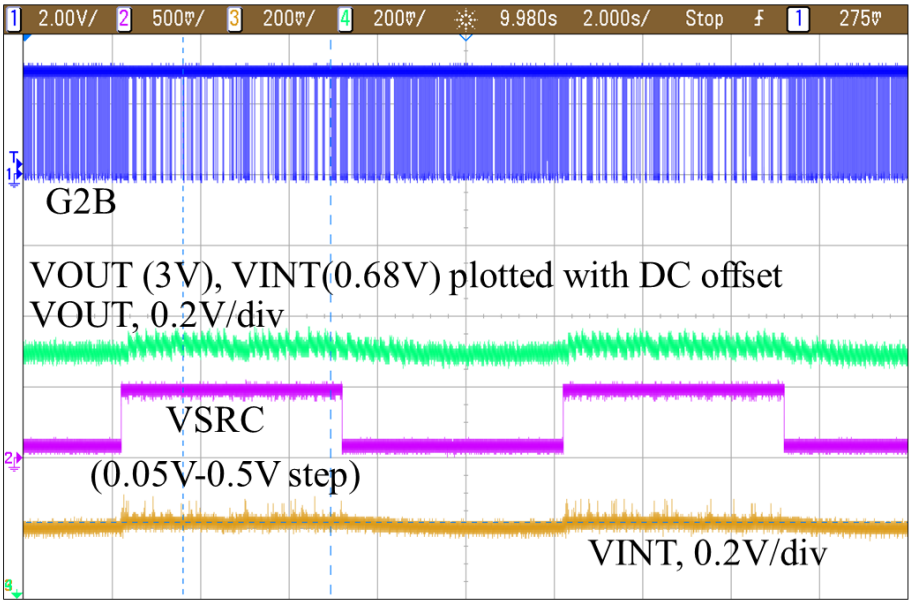


Figure 66: Input voltage step response or line regulation characteristic of the regulator. Similar to the load step response, the input step also changes the activity pattern. With higher input voltage the activity decreases.

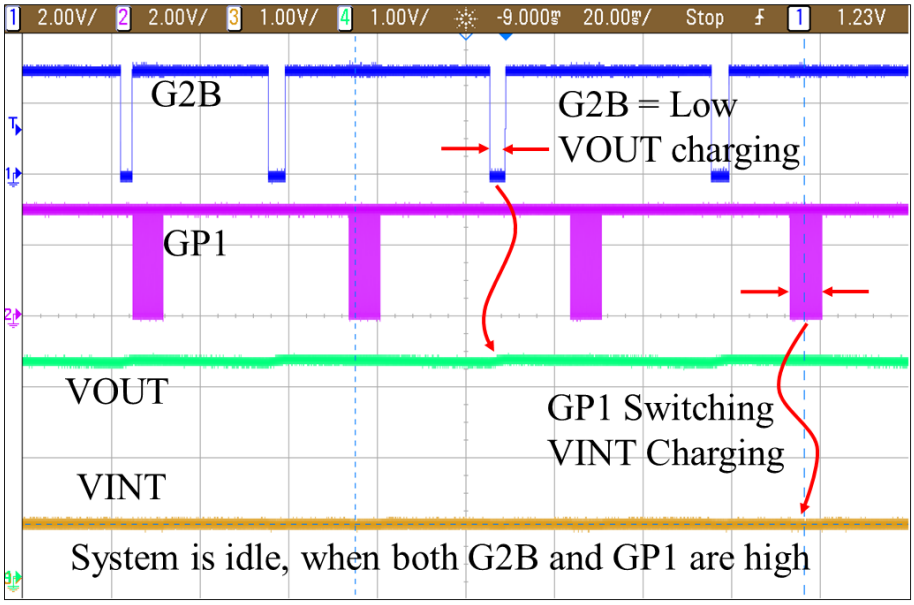


Figure 67: Phase 1 and phase 2 operation is light load condition. The mode transition happens with idle time in between.

7.7.1 Start up and Operation with Dynamic Input

Fig. 63 shows the startup of the system from 100mV input. During startup, which is managed by the priority circuit, V_{INT} is seen (Fig. 63) to charge up before V_{OUT} starts

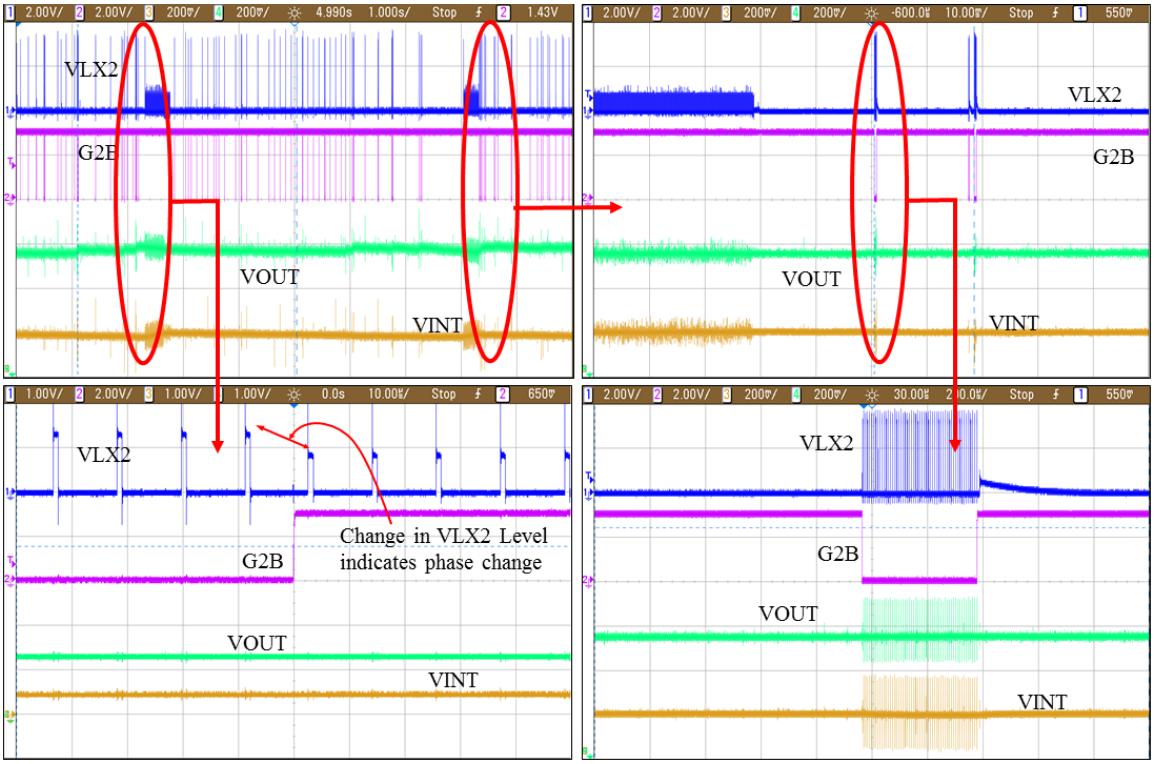


Figure 68: Regulator operation showing different events. To regulate both V_{INT} and V_{OUT}, the regulator dynamically switches between phase 1 and phase 2 operation. Top-left corner shows a typical snapshot of operation. Top-right shows the magnified view when the regulators makes a phase 1 to phase 2 transition with an idel time in between. The operation in phase 2 is further zoomed in and shown in bottom-right which reveals multiple activity during phase 2. A direct transition from phase 2 to phase 1 is shown in bottom-left corner. The level change in V_{LX2} node indicates the mode transition which happens without any idle time in between. The regulator is capable of making both way transition in between phase 1 and phase 2 with or without idle time.

charging. The change-over point is indicated by the change in V_{LX2} amplitude. Fig. 64 shows the operation with varying input voltage, where 120x conversion ration operation is shown (25mV to 3V).

7.7.2 Transient Characteristics

Fig. 65 shows the load transient response of the regulator. With higher load the activity of the both phases are seen to increase. The peak ripple at V_{OUT} is measured during load conditions and is less than 50mV. The input voltage step response is shown in Fig. 66. The regulator exhibits higher activity factor when input is lower.

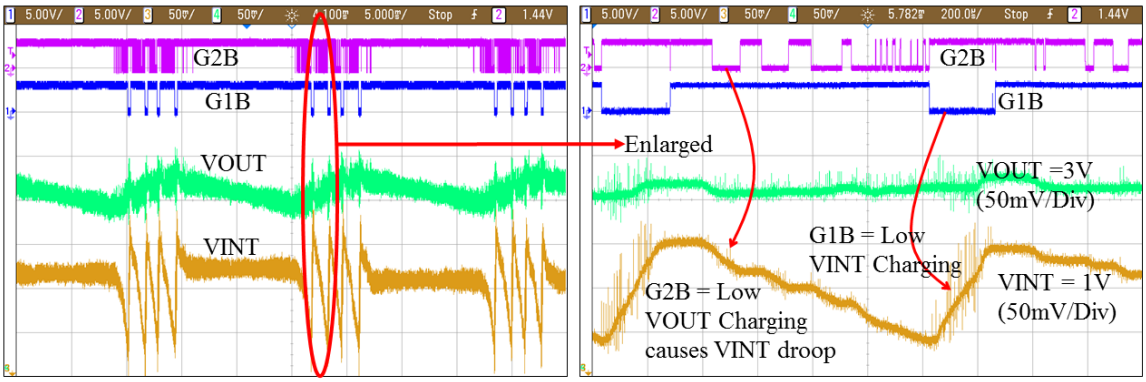


Figure 69: The charging of V_{OUT} and V_{INT}. The regulation controller charges both nodes alternately. The loading of V_{OUT} to V_{INT} is shown in the enlarged view of this operation.

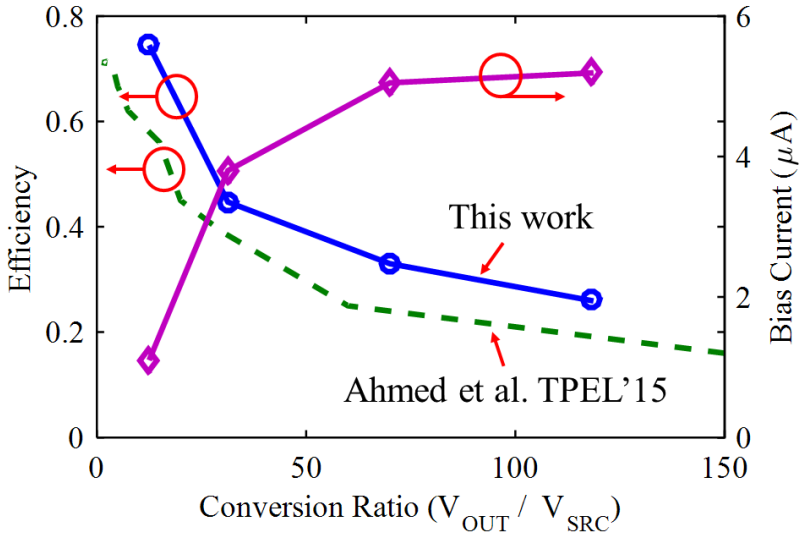


Figure 70: Efficiency profile of the regulator with conversion ratio. Also shown is the bias current profile.

7.7.3 Regular Operation

Fig. 67 shows the regulator operation with light-load condition. The regulator exhibits long idle times in between two active regions. Additionally, the mode transition happens with idle time in between the phase transitions, i.e., the regulator goes from phase 1 to idle period and then goes into phase 2 followed by another idle period. Regulator is capable of making the transition both with and without idle time in between. Fig. 68 shows a detail operation which shows both types of mode transition. contiguous (no idle time in between),

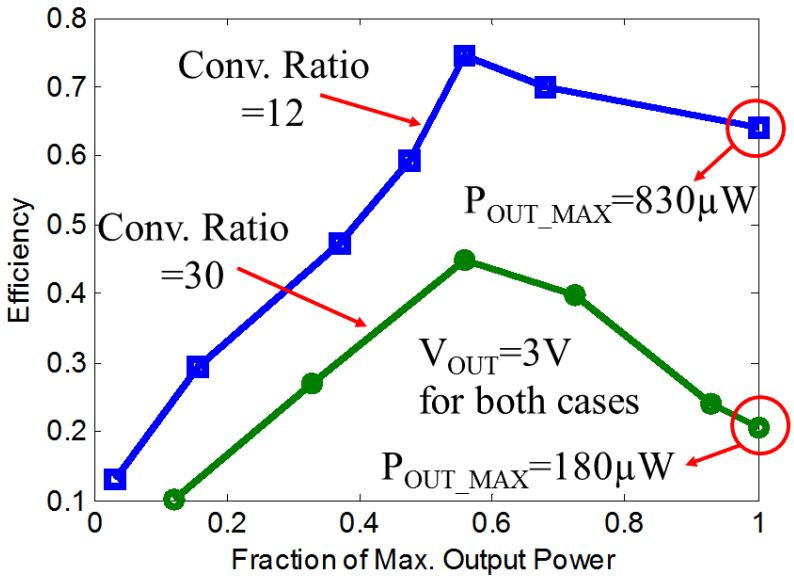


Figure 71: Efficiency profile of the regulator with load variation.

and non-contiguous (transition with idle period in between). A contiguous mode transition event is enlarged in top-right corner. Bottom-right portion further enlarges the view to reveal multiple switching events in phase 2 operation. A contiguous mode transition case is zoom in and shown in bottom-left corner. The mode transition occurs without any idle time in between and the change of phase is evident from the level shift of the V_{LX2} node.

Fig. 69 shows the ripple of both V_{INT} (100mV) and V_{OUT} (50mV). V_{INT} hysteresis is kept greater to accommodate for the loading from V_{OUT}. The droops in V_{INT} due to successive V_{OUT} loading are shown in the enlarged view.

Fig. 70 presents the efficiency and bias current profile with conversion ratio. At higher conversion ratio the activity factor increases which results in more switching loss, hence the efficiency degrades. Fig. 71 shows the efficiency profiles with different output power. The plot is shown for two different conversion ratios and with normalized power. The peak efficiency is achieved at mid-load condition, and the efficiency improves with lower conversion ratio. Table 5 shows comparison chart with prior works on the boost regulators. This work achieves lower bias consumption and higher conversion ratio as compared with other reported works.

Table 5: Performance comparison chart with prior single stage high conversion ratio boost regulator works

Item	ISSCC '14 [61]	ISSCC '12 [34]	ISSCC '12 [30]	JSSC '11 [29]	JSSC '10 [28]	This work
Min. VSRC	20mV	100mV	30mV	25mV	20mV	**25mV**
Bias Current/Power	544 pW	150 nA *	-	-	1.1μA	**140nA**
V_{OUT}	1.1V	3V	2V	1.8V	1.4V	**3V**
Conv. Ratio**	55 ***	33	30	72	50	**120**
Peak Eff.	53%	92%	61%	60%	75%	**74%**
Max Pout	4nW	~12mW	N/A	300μW	175μW	**830μW**
Process	0.180μm	0.35μm	0.13μm	0.35μm	0.13μm	**0.13μm**
Area	1.52mm^2	-	0.09mm^2	4.2mm^2	0.12mm^2	**0.42mm^2**
*Total bias is 330nA. ** Inductive boost only. ***Maximum conversion ratio.						

7.8 Summary

A high conversion ratio boost regulator topology is presented. The proposed topology time-multiplexes a single inductor between two power stages in a two-stage cascaded regulator system. This topology helps to achieve a conversion ratio higher than that is achievable solely by the duty cycle of oscillator in single stage. The system architecture can be scaled to even higher conversion ratios by adding more stages in the design, while using only one inductor. A prototype IC fabricated in 130nm demonstrates the functionality of the proposed topology. Enabled by the proposed topology, the IC harvests from as low as 25mV input. Widened harvesting input range makes this design suitable for energy extraction from sources those produce low energy fields. The bias current is reduced using bias gating technique, making this regulator suitable for low power systems those run with intermittent short bursts of high powers as found in many wireless sensors or IoT applications.

CHAPTER 8

SINGLE-INDUCTOR MULTI-OUTPUT REGULATOR WITH COMBINED ENERGY HARVESTING AND POWER DELIVERY

This chapter discusses the design of a combined energy harvesting and multi-domain power delivery circuit using a single inductor.

8.1 Introduction

Energy harvesting has emerged as a key technique to power distributed sensor nodes. With increasing functionalities embedded in small devices, the demand for energy, volume and weight efficient power management units have grown significantly. Specific application spaces such as the wireless sensors and Internet-of-Things devices require power management units (PMU) to harvest and locally store environmental energy [30, 63–66]. Small devices deployed in remote sensor applications often have multiple types of circuitry, including analog, digital, RF and memory. These circuits have different power demand and activity profiles. To supply power efficiently to these circuit blocks, it is essential to have multiple voltage domain those can operate simultaneously. Additionally, because of the different system constraints, it is crucial to minimize the number of passive components (inductors) to reduce cost, volume and weight of the design.

This chapter presents an on-chip highly integrated power management system that can harvests energy from low input voltage and generates multiple regulated power supply, using a single external inductor. The design and operation of a boost regulator for energy harvesting and multiple output buck regulator for simultaneous multi-domain power delivery are discussed. Both the boost and the buck regulator use the only inductor in the system using an autonomous on-chip time multiplexing controller. The boost regulator harvests energy from the sensor to charge the on-board storage (super capacitor or battery) using maximum power point tracking. The stored energy is then delivered to the three

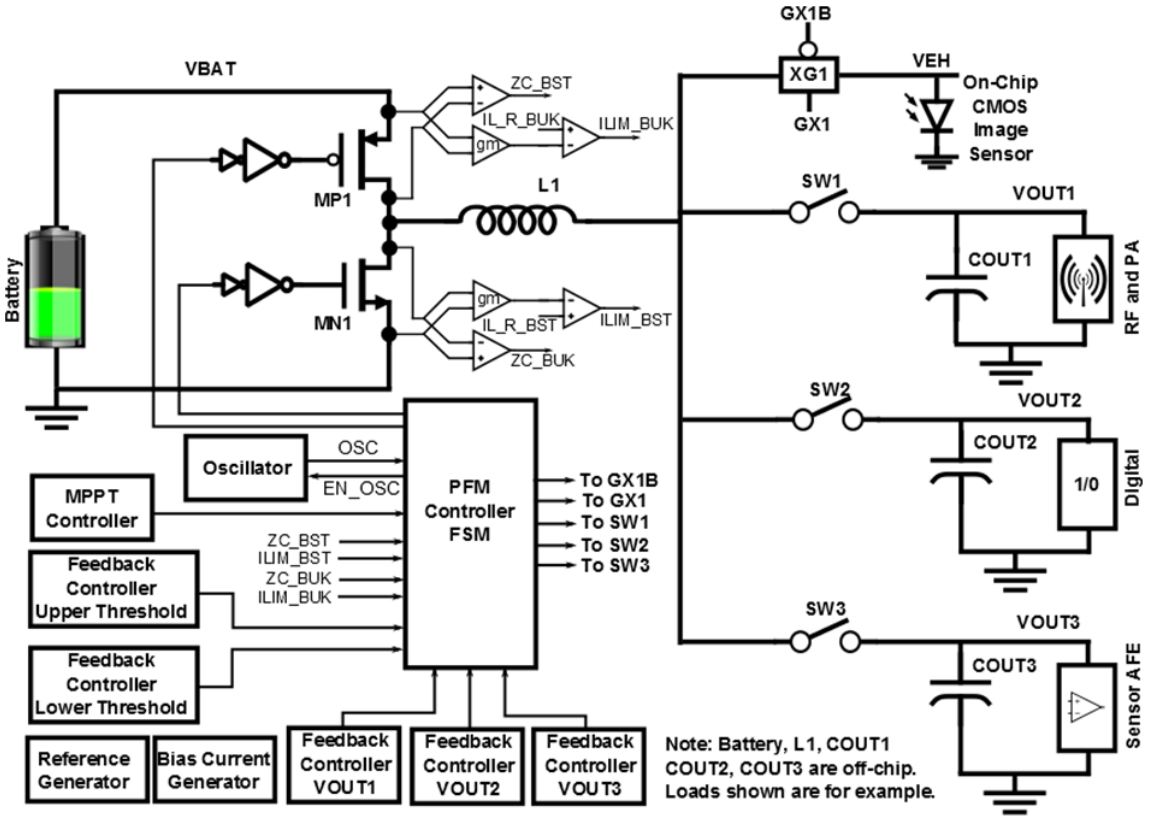


Figure 72: Architecture of the power management unit with energy harvesting and voltage regulation.

load domains by a Single Inductor Multiple Output (SIMO) buck regulator having three independently controlled outputs. A test-chip is demonstrated in 0.13μm CMOS technology. The measurement results demonstrate successful energy harvesting and generation of multiple regulated outputs voltage domains.

8.2 Architecture Discussion

Fig.72 shows the power management circuit block diagram consisting of the energy harvesting and the power delivery system that uses a single inductor and a single power stage. The circuit operates in two modes; (1) harvesting energy (boost operation) and (2) power delivery (buck operation). Both the boost and buck operation are performed using the pulse frequency modulation (PFM) scheme controller. The following subsections discuss the design details of the boost and the buck regulator. The control circuits are powered by V_{BAT}

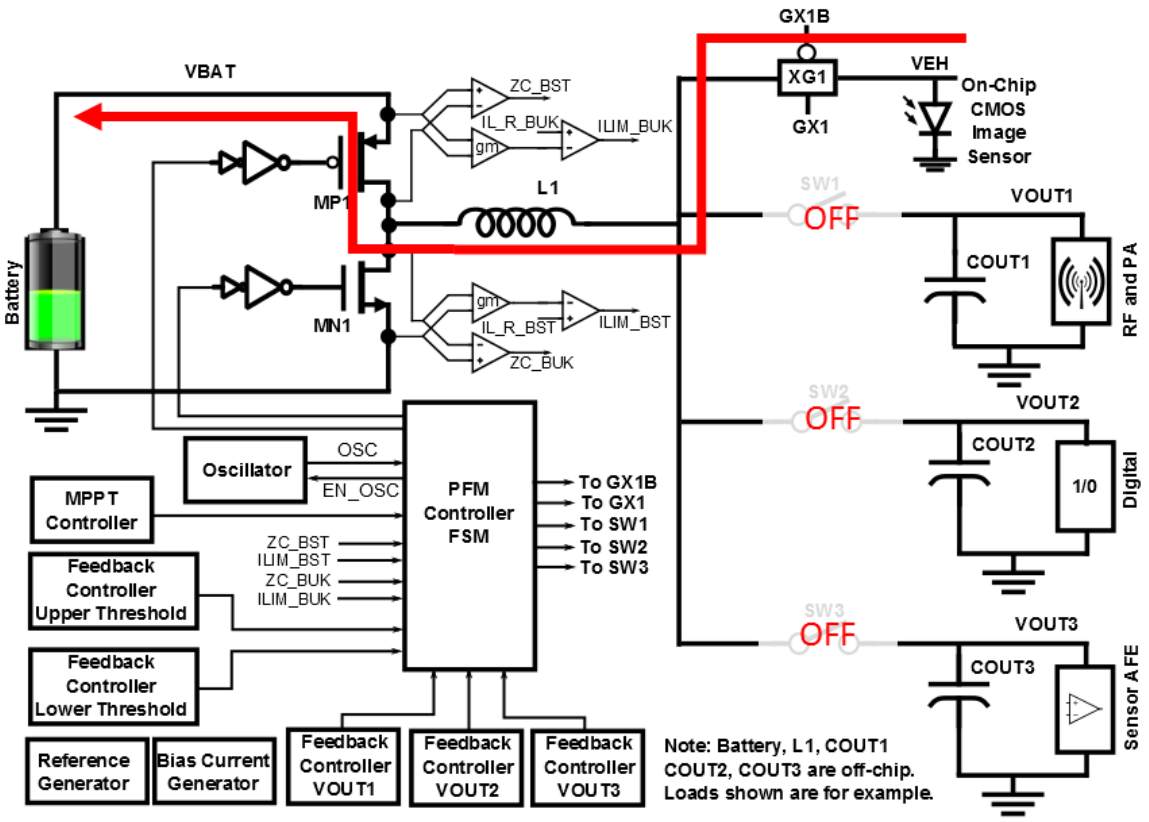


Figure 73: Boost operation. Transmission gate XG1 is on for the duration of boost operation while MP1 and MN1 switch in complimentary manner. The SIMO switches for buck (SW1, SW2, SW3) remain off during boost operation. The arrow indicates the flow of charge

allowing harvesting from very low voltage when $V_{BAT} > 0.37V$.

8.3 Energy Harvesting Mode: Boost Operation

8.3.1 Operation Description

During harvesting, the system configures itself as a boost regulator to transfer energy from V_{EH} to V_{BAT} node. At the beginning of this phase, the transmission gate XG1 is turned on which connects the energy source V_{EH} to one end of the inductor. The other ened of the inductor is connected to V_{LX} node where switch devices MN1 and MP1 are connected too. The feedback network senses the output voltage and if it is lower than the desired regulation level, the internal oscillator is turned on. The oscillator in turns controls switch MN1 and MP1 to build current through the inductor and transfer charge from V_{EH} to V_{BAT}

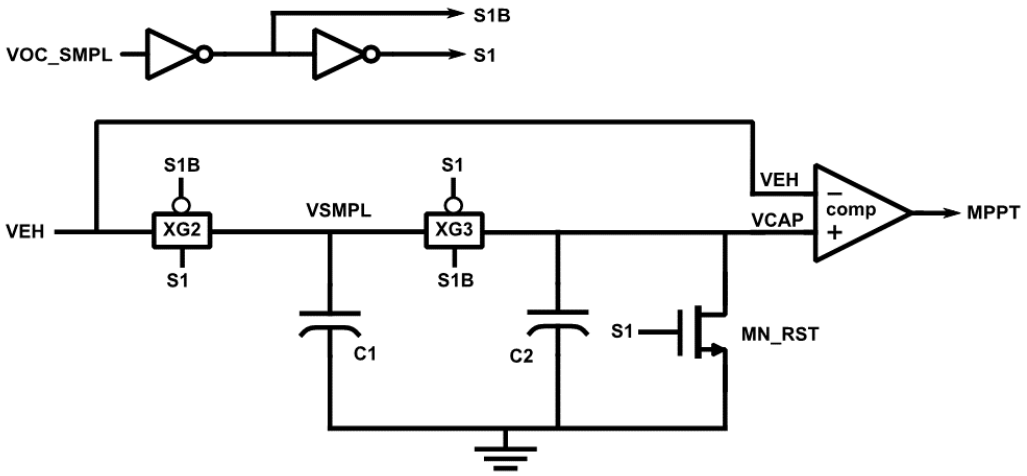


Figure 74: Maximum power point tracking circuit.

pulse by pulse basis. The switch configuration is shown in Fig.73

8.3.2 Current Detection

The current through both MN1 and MP1 are monitors for over current protection and for zero crossing detection, respectively. The current limit circuit triggers when the MN1 current exceeds the predefined limit. The circuit consists of a '*gm*' amplifier followed by a comparator. The comparator compares the sensed current value against an internally generated reference IL-R-BST to detect the over current event and generates the signal ILIM-BST when it happens. The current through MP1 is monitored for detecting the zero crossing event. Once the inductor current goes to zero during the boost phase (inductor current discharge phase), it is required that the device MP1 be turned off as soon as the inductor current reaches zero. If MP1 remains on after the inductor current reaches zero, the inductor current will become negative hence flow backward and steals the charge from the battery. This undesired phenomenon decreases efficiency. The zero current detection circuit observe the voltage across MP1 and generates ZC_{BST}, which is then used to turn off MP1.

8.3.3 Maximum Power Point Tracking controller

With varying input energy fields, ambient energy transducers produce variable amount of energy. Maximum power point tracking enables a system to harvest the maximum possible energy from a source with dynamically varying generated power. Several maximum power point tracking (MPPT) mechanisms have been reported [30, 67–77]. In this design we incorporate a technique of open circuit sensing based MPPT. The circuit for MPPT is shown in Fig.74. The controller receives an external open circuit sensing signal VOC_{SMPL}; when this signal is 'high', it turns off the transmission gate XG1 (shown in Fig.73) thereby isolating the V_{EH} from internal circuitry. At the same time, the signal also turns on the transmission gate XG2 to sample the open circuit voltage at V_{EH} in capacitor C1. During this sampling time, transmission gate XG3 is turned off to isolate the comparator input from the sampling capacitor. The capacitor C2 is kept at ground potential during this time by the resetting switch MN-RST. When VOC_{SMPL} goes 'low', transmission gate XG1 and XG3 are turned on, XG2 is turned off and the switch MN-RST is also turned off. The sampled voltage VSMPL at capacitor C1 is now connected to completely discharged capacitor C2. Depending on the value of this two capacitors, the final voltage at VCAP node is settle to a new value. The initial charge stored in the capacitor C1,

$$Q_{initial} = C_1 V_{sample} \tag{43}$$

After charge redistribution, both the capacitors are connected in parallel and the relation between final voltage and final charge is,

$$Q_{final} = (C_1 + C_2) V_{final} \tag{44}$$

Since the amount of charge stored before and after the charge redistribution must remain same ($\mathrm{Q}_{initial} = \mathrm{Q}_{final}$), we find,

$$V_{final} = \frac{C_1}{C_1 + C_2} V_{initial} \tag{45}$$

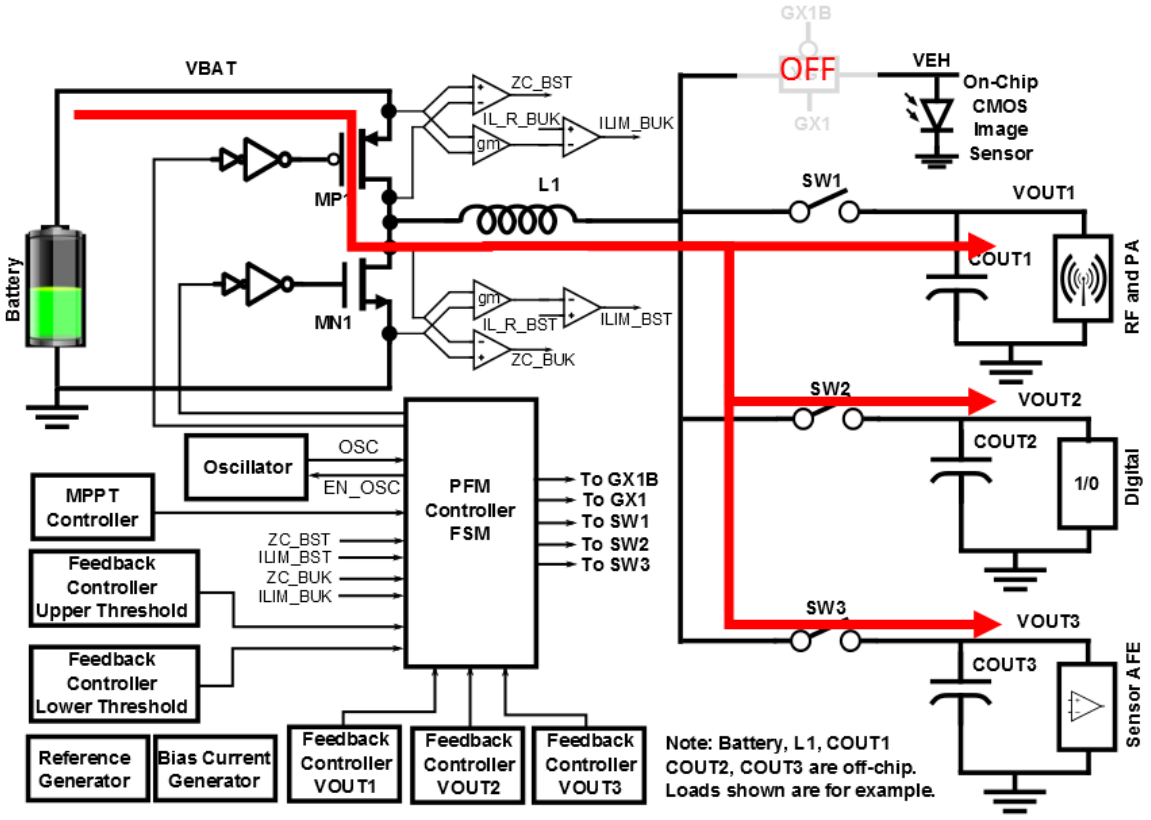


Figure 75: SIMO Buck operation. Transmission gate XG1 is off for the duration of buck operation while MP1 and MN1 switch in complimentary manner. Additionally, SW1, SW2 and SW3 operate in exclusive scheme. The arrow indicates the flow of charge.

Depending on the value of these capacitors the voltage that appears at the VCAP node (V_{final}) can be programed to any value. For this design the capacitors C1 and C2 are same, hence the final voltage is half of the sampled V_{EH}.

Since the comparator's positive input is connected at the VCAP which remain static until the next 'high' appears on VOC_{SMPL} while the negative input receives the dynamically varying instantaneous V_{EH}; the output of the comparator, MPPT remains 'low' so long as the V_{EH} remains higher than VCAP. Because at every pulse the regulator demands current from the source, due to the finite resistance, the apparent value at the V_{EH} drops. In this design, as the VCAP is set at 50% of the sampled V_{EH}, the regulator keeps loading the V_{EH} until it has dropped to 50% of the sampled V_{EH}. At that point, the comparator generates a 'high' at the output. A high MPPT ceases the boost operation until V_{EH} goes above the 50%

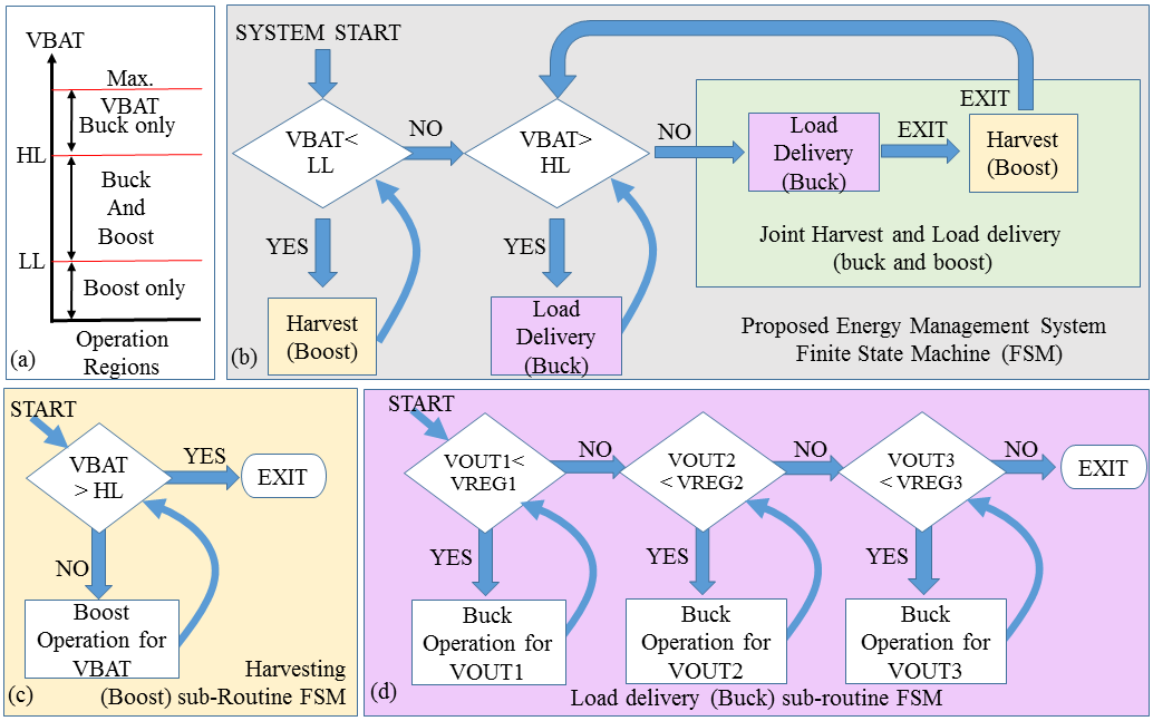


Figure 76: (a) Battery management regions , (b) Flow chart of the power delivery unit including battery management, (c) Boost operation sub-routine and (d) buck operation sub-routine showing the priority among the different outputs.

level. This 50% fractional MPPT simplifies the algorithm while harvesting approximately 70% of the peak power from any energy source that emulates a photovoltaic cell.

8.4 Multi Domain Power delivery using SIMO buck

8.4.1 Operation Description

During buck operation, energy is delivered from V_{BAT} to the load at V_{OUT1}, V_{OUT2}, V_{OUT3} using the single inductor multiple output (SIMO) topology. In the SIMO-buck method, each load switch (SW1, SW2 or SW3) is controlled by a feedback comparator and are exclusive to each other. Hence at any moment, only one switch can be turned on while other two must remain off. The feedback controllers operate in hysteresis mode and in valley control method. The SIMO-control also isolates all the outputs from the energy source during the boost operation by turning the transmission gate XG1 off. The switch configuration is shown in Fig.75

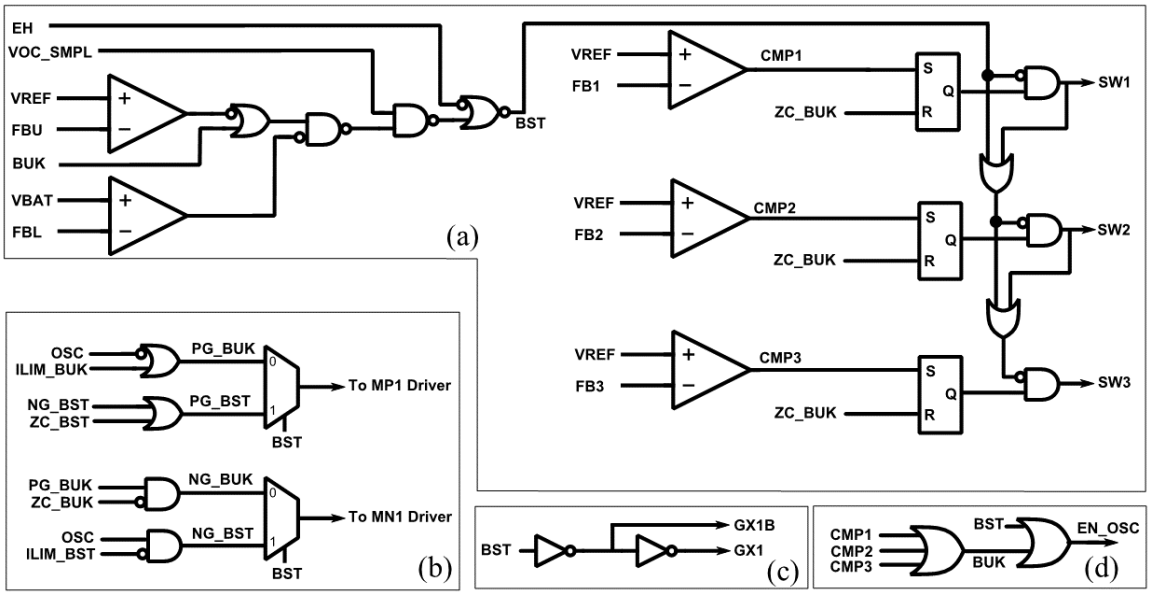


Figure 77: Signal generation of the system (a) V_{OUT} SIMO switch controller, (b) power stage controller, (c) energy harvesting transmission gate controller and (d) oscillator controller.

8.4.2 Cross Regulation Management in SIMO

Cross regulation is a critical system drawback for SIMO regulator [78–83]. Because a single inductor is being multiplexed between different loads, a transient in one load affects other domains unexpectedly. This condition deteriorates when multiple domains demand power at the same time. In this design, we have prioritized the load domains to direct the effect of cross regulation to flow in a certain way. The three load domains are prioritized to provide opportunity to differentiate between critical circuit blocks over the non-critical blocks. In this design, V_{OUT1} has the highest priority while V_{OUT3} has the lowest. In the event of simultaneous power demand, higher priority output is be provided first. This ensures no cross regulation at the highest priority output while offering standard cross regulation performance at the lowest priority one. Accordingly, the effect of cross regulation only flows from high priority domain to the low priority domain, but prevents the opposite flow. Hence a load demand in the lower domain will not affect the regulation performance on the higher priority domain. Additionally to reduce the effect of residual inductor current, the mode transition happens only after a zero current event is detected. The zero current

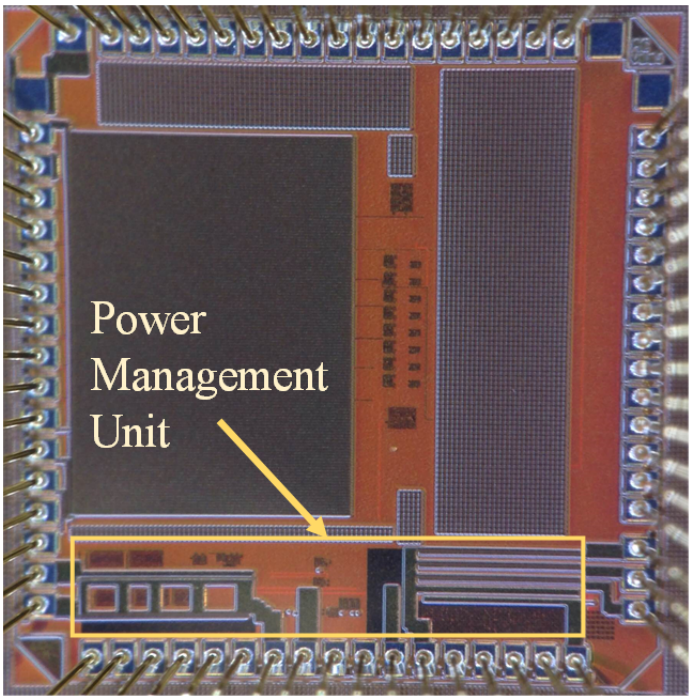


Figure 78: Die photo of the chip showing the power management unit (PMU). The die area is 2mmx2mm; PMU area is 0.6mm^2.

detection in buck mode is performed by measuring potential difference across NM1 using a comparator that generates ZC_{BUK} signal. Additionally, the current through the device MP1 is monitored and the signal $ILIM_{BUK}$ triggers when it goes above the designed limit. $ILIM_{BUK}$ is generated by the current limit circuit and truncates the MP1 pulse width forcing it turn off before the other maximum allowed time set by the oscillator.

8.5 Autonomous Mode Management (AMM)

The AMM controls the switching between forced load delivery and forced harvesting mode of the sensor (depending on load demand and energy availability) as well as transitions between the boost and buck mode of the regulators (depending on the priority of the load and battery voltage level). In applications with a dual purpose sensor (e.g., an energy harvesting and imaging sensor, see Chapter 9) and a target frame rate, an external frame rate control signal will cause EH to change from low (sensing, and load delivery) to high (harvesting). The AMM enforces (i) boost-only operation when battery voltage (V_{BAT}) is

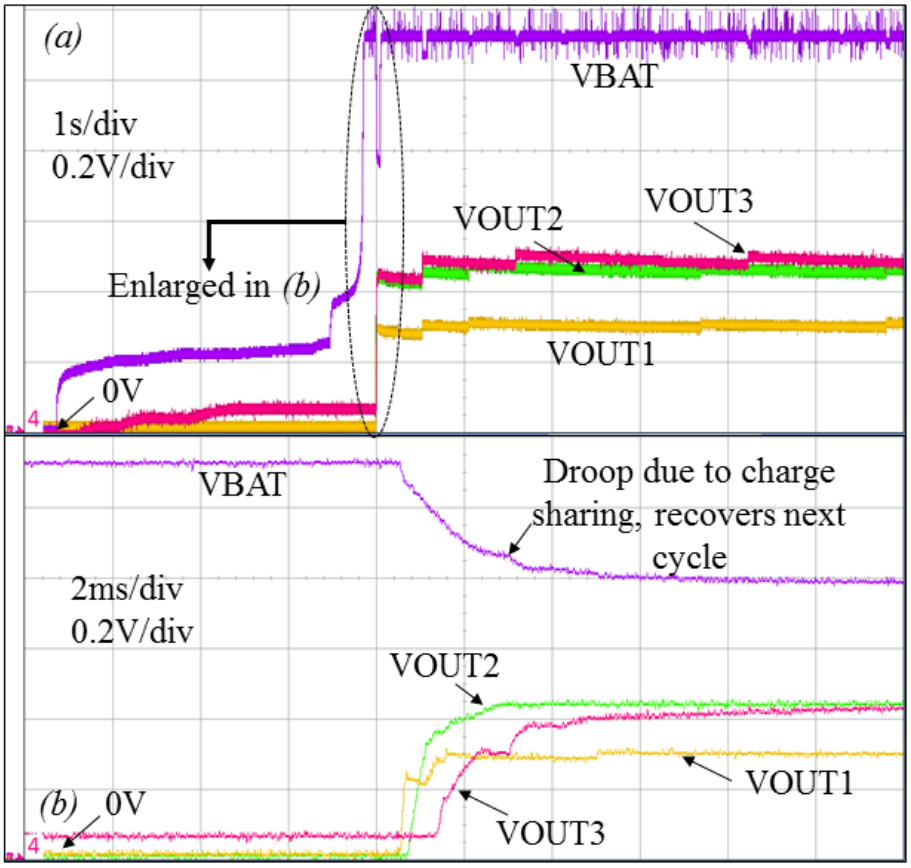


Figure 79: (a)PMU start-up and operation in cold start condition (battery-less start-up) from 0.37V, generating four domains and (b) shows the marked portion in enlarged view. The battery voltage experiences a droop when the output capacitors charges up. The droop recovers in subsequent boost phase. The output domains regulate independently. Here V_{OUT2} and V_{OUT3} are set at same level while V_{OUT1} is set at lower level.

less than a lower limit (LL) (deep discharge cut off point), (ii) buck-only operation if V_{BAT} is higher than a higher limit (HL) to prevent overcharging, and (iii) switching between buck and boost modes when: LL < V_{BAT} < HL. The algorithm is shown in Fig. 76 and the related schematics are shown in Fig. 77.

8.6 Measurement Results

A test-chip in 0.13μm CMOS demonstrates the proposed power management unit (PMU) with integrated CMOS image sensor (Fig. 78). The chip is wire bonded in open cavity LCC 64 package.

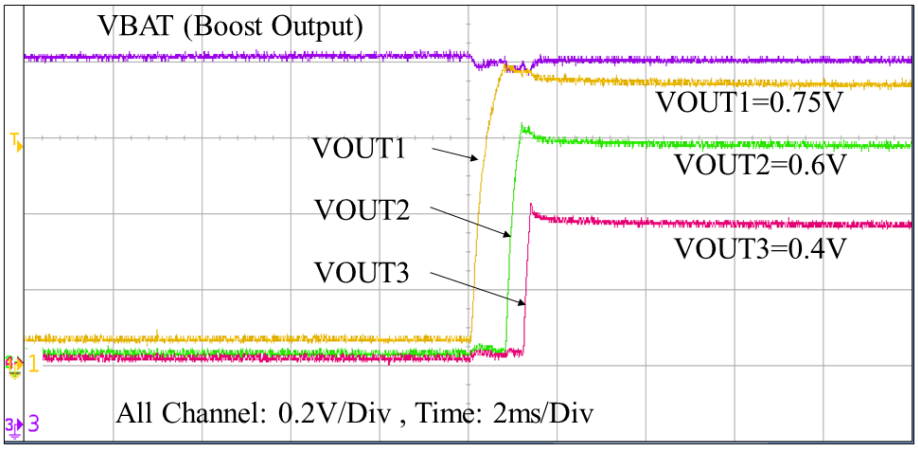


Figure 80: Startup sequence of different output levels. The sequence is dictated by the priority of different domains; here V_{OUT1} has the highest priority and V_{OUT3} has the lowest.

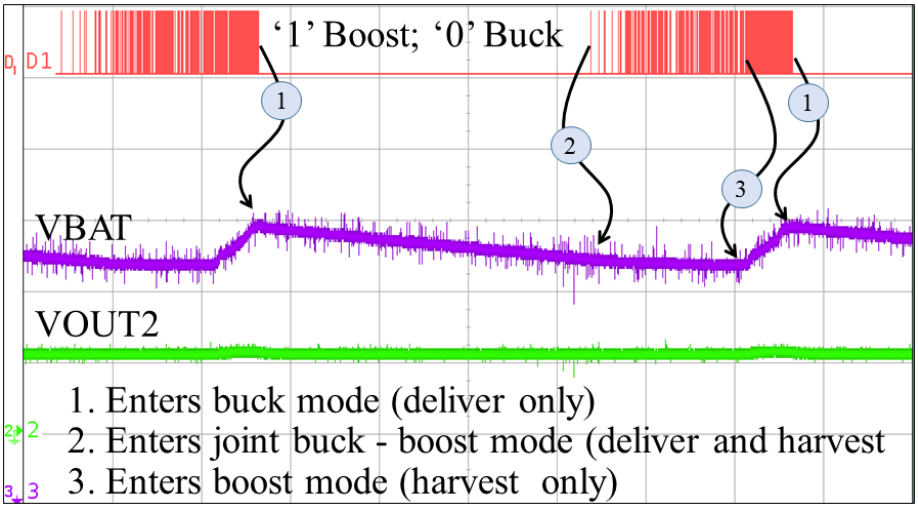


Figure 81: Different events of battery management.

Fig.79(a) shows cold start from 370mV at V_{EH} (230mV at V_{BAT}) and generation of four voltage domains including V_{BAT}. The battery node serves as the input to the SIMO buck stage which generate three regulated domains. When the three SIMO domains start up, the battery experiences a droop [Fig.79(b)] which is recovered at the next boost phase. The regulator is biased from V_{BAT} and typically at 1V biasing, it can harvest from 50mV or higher input while consuming 0.2μW of bias power.

Fig. 80 shows a close up view of the SIMO domains during start up. Since the domains are sequenced through priority assignment, they start up in consecutively which is

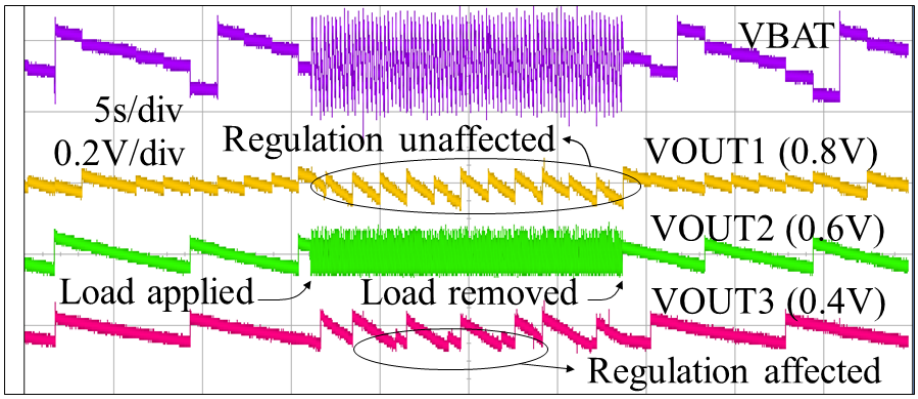


Figure 82: Load regulation and the effect of priority of cross regulation management.

clearly visible, V_{OUT1} highest and V_{OUT3} being lowest. The priority assignment also help to minimize cross regulation in higher priority domains.

Fig. 81 shows the different events of the battery management technique. As the battery level reaches higher threshold, the regulator enters buck only mode and starts discharging. When the discharged battery crosses a hysteresis window, it enters a mode when both buck and boost is allowed. That is, during this time the system supplies the load domains however, if there's an idle period in between, it goes back to harvesting mode. The SIMO domains are designed with higher priority over energy harvesting (boost mode) and among the SIMO domains, V_{OUT1} is designed with the highest priority. If the battery voltage keeps falling further, sensing a critically low level in the battery, the regulator invokes a boost-only mode to replenish the charge.

Fig. 82 shows the load regulation profile of the regulator. The load is applied to V_{OUT2} only. This applied load increased the activity factor of this domain, however the regulator is able to maintain the DC level of regulation. Note that the applied load at V_{OUT2} affects the V_{BAT} which eventually results in increases the activity factors for both V_{OUT1} and V_{OUT3}. The cross regulation minimization is visible from the way V_{OUT1} and V_{OUT3} are affected. During the high load period, the ripple pattern in V_{OUT1} remains periodic but V_{OUT3} suffers from aperiodic ripples. This phenomenon is expected due to the priority assignment. Since V_{OUT2} has higher priority than V_{OUT3}, with the load applied, V_{OUT2} is demanding more

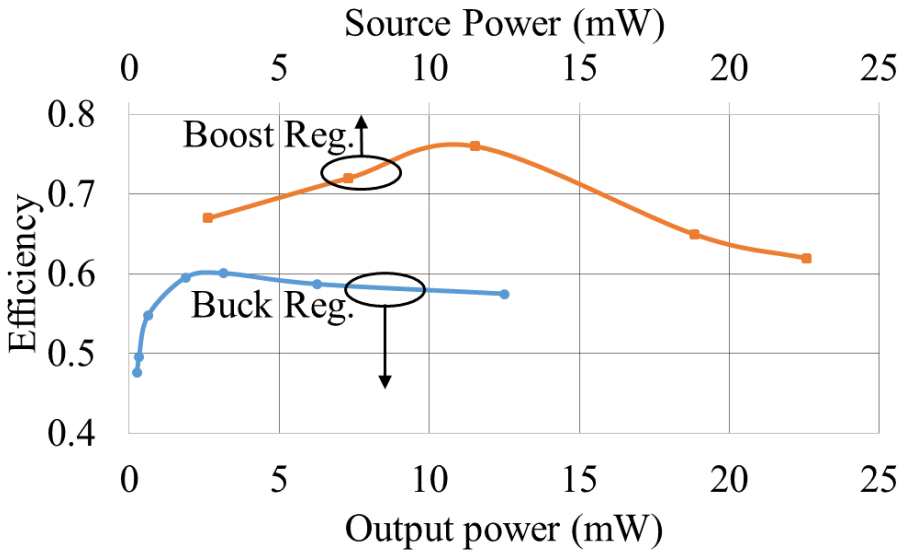


Figure 83: Efficiency profiles of the boost and buck regulators.

active time which overlaps with V_{OUT3} demand. Since the AMM gives priority to V_{OUT2} over V_{OUT3} during simultaneous demand, V_{OUT3} suffers from cross regulation. During the whole period, V_{OUT1} enjoys highest priority and is not affected directly by the V_{OUT2} load application. The priority based regulation hence offers a mechanism to push the cross-regulation towards the low priority domains while offering cross-regulation free operation at the higher priority domains.

Fig. 83 shows the efficiency profiles of the boost and buck regulator. The buck efficiency is lower due to the higher resistance of the SIMO switches; by optimizing the switch sizes, the efficiency is expected to improve.

Key performance characteristics of this power management unit are provided in Table 6 in comparison with other works. The integrated PMU generates four voltage domains using a single inductor and power stage. As compared with a prior PMU-only work [64], this PMU achieves lower cold-start voltage (370mV) and consumes lower bias power (0.2μW).

8.7 Summary

This chapter presents a highly integrated power management solution for energy harvesting and multiple domain power delivery. The demonstrated system harvests energy, stores

Table 6: Comparison with prior works (Regulator)

Item	ISSCC ' 14 [63]	VLSI '14 [64]	ISSCC '13 [65]	VLSI '15 [66]	**This work**
No. of domains	2	4	3	2	**4**
Cold Start	n/a	380mV	n/a	330mV	**370mV**
Max. V_{BAT}/V_{OUT} range	1.8V/0.8V	5V/1.2V-5V	3V/1V-3V	4.1V/1V	**3.3V/0.2V-1.2V**
Bias Power	n/a	1.2μW	0.4μW	3.2nW	**0.2μW**
Max. Eff. (Boost/Buck)	83%	92%/92%	83%	84%/ >80%	**76%/54%**
Max. Power	10mW	100mW	10mW	1μW	**10mW**
Area (mm^2)/Tech.	n/a/180nm	2.25/130nm	4.35/180nm	2.42/180nm	**0.6/130nm**
Battery Mgt.	No	Yes	No	Yes	**Yes**
Cross Regulation Mgt.	No	No	No	No	**Yes**

it in a battery and delivers three independently regulated voltage domains to power different types of circuitry. This system provides compact power management solutions for extremely reduced form-factor electronics in mobile and distributed applications.

CHAPTER 9

TOWARDS SELF-POWERED SENSORS: A BRIEF NOTE AND PRELIMINARY RESULTS

This chapter discusses some preliminary results on integrated self-powered sensors for pervasive IoT devices.

9.1 Introduction

Harvesting energy, being essential for increased lifetime of distributed sensors network electronics however, requires additional devices such as thermoelectric, piezoelectric, photovoltaic, etc., which increases system complexity and cost. An alternative approach to design a truly self-powered sensor node will be to use the existing sensor itself as an energy source. Consider the example of a wireless image sensor with on-chip CMOS pixel array, image processing, and communication (Fig. 84). Many wireless image sensing requires relatively low frame-rate, often limited by the channel bandwidth. Hence, the pixel array is used for sensing only for a limited fraction of time. The on-chip sensor can be configured to harvest energy during the idle time and store on-board in a battery or supercapacitor, providing potential of a truly self-powered system. Few recent works have shown the feasibility of using an image pixel array for harvesting (Table 7) [84–87] . However, an integrated system producing multiple regulated output voltage for powering a typical sensor node with on-chip imaging, processing, and communication has not been demonstrated yet.

Fig. 84 shows the architecture of the self-powered image sensor node that includes the dual-purpose CMOS sensor, image processing, communication, and power management. This chapter presents a some design concepts and preliminary results on harvesting energy from an on-chip dual purpose CMOS image sensor. It focuses on the design and

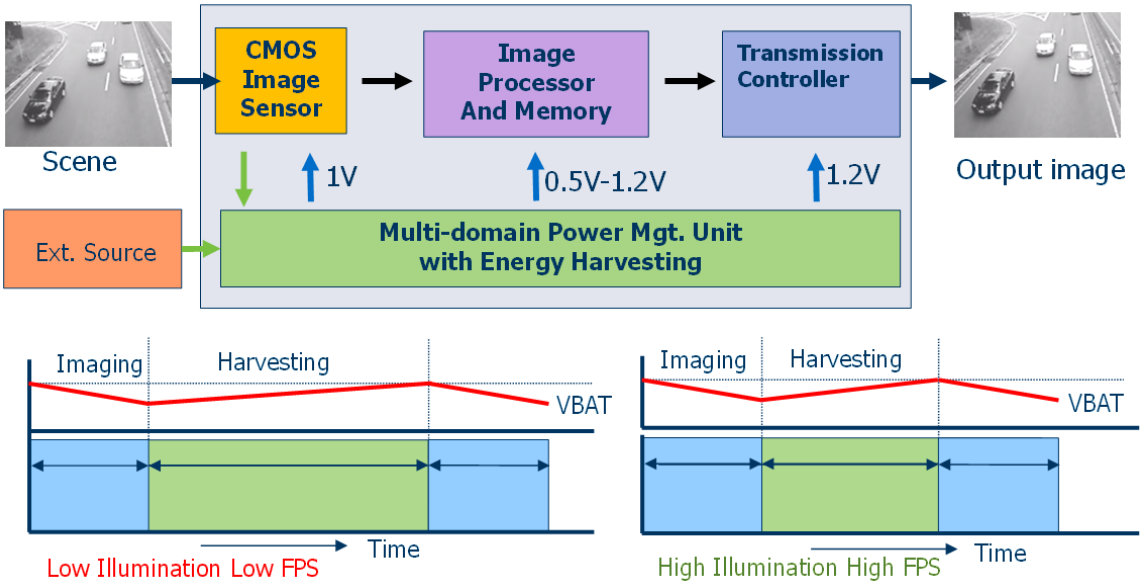


Figure 84: Energy autonomous imaging system architecture. This work focuses only on the energy harvesting aspect of the image sensor and the power management circuit discussion.

operation of the pixel design to support dual purposes (sensing and harvesting). Few results on the energy harvesting aspect of the sensor are also presented. The reconfigurable 128 x 96 CMOS Active Pixel Sensor (APS) array operates in photoconductive mode when imaging and photovoltaic mode when harvesting. The mode switching can be based on the frame rate, and/or autonomously managed based on available stored energy. A test-chip is designed in 0.13μm CMOS technology node. The measurement results demonstrate successful energy harvesting from the on-chip CMOS imager. An analysis shows the potential

Table 7: System level comparison with prior works on energy harvesting capable sensors

Item	Tech.	Sensor integration
Law'11 [84]	0.35μm	Sensor only
Wang'15 [85]	0.5μm	Sensor + switch only
Nayar'15 [86]	External sensor	Ext. Sensor + supercapacitor. Unregulated output
Chiou'15 [87]	0.18μm	Sensor + capacitor. Unregulated output
This work	**0.13μm**	**Sensor + full DC-DC regulator with 3 regulated output.**

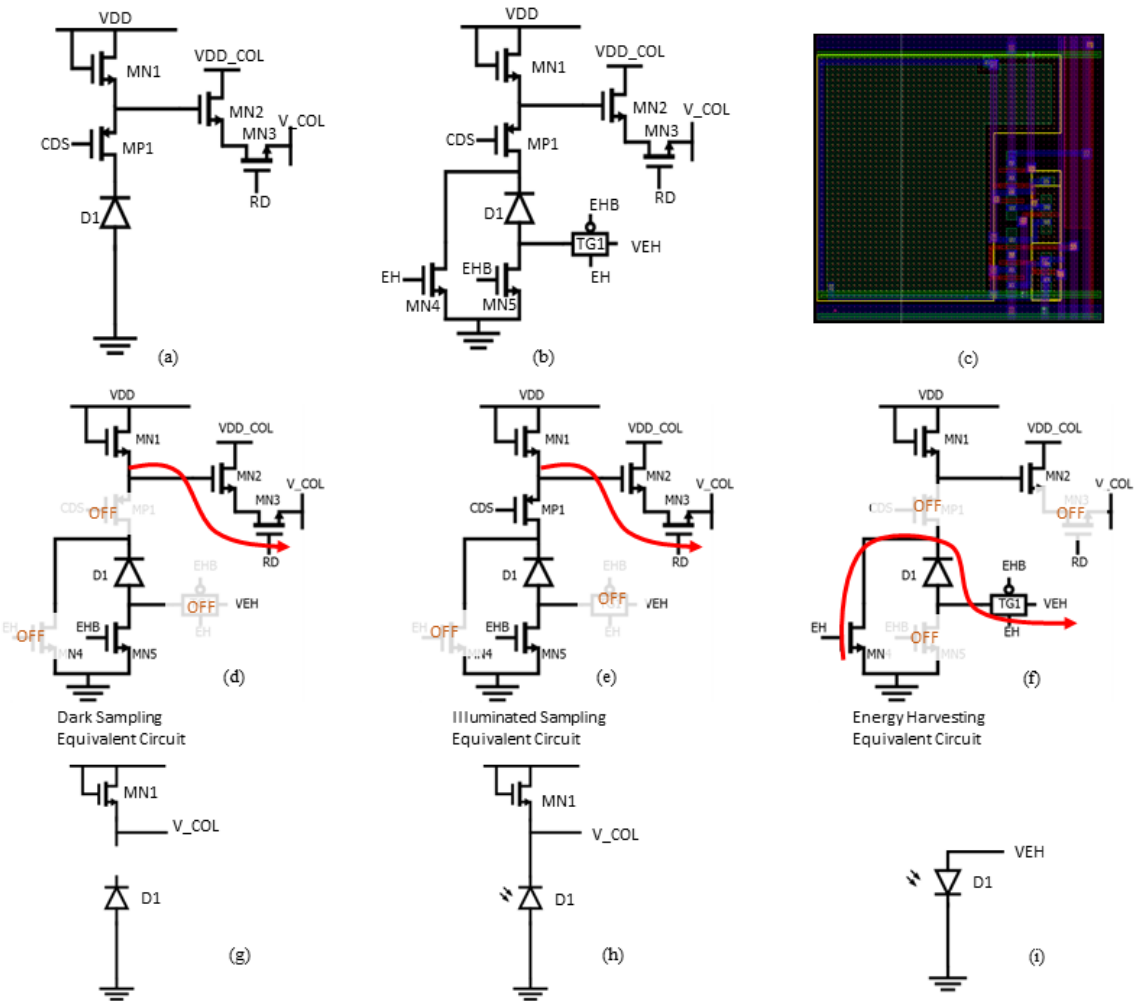


Figure 85: (a) Conventional logarithmic CMOS APS (b) Proposed APS with reconfigurable photodiode, (c) layout of the proposed APS (d) circuit configuration during dark sampling, (d) circuit configuration during illuminated sampling, (f) circuit configuration during photovoltaic operation (V_{EH} of all pixels are shorted in this mode to form a single cell from which energy is harvested) and (g-i) equivalent circuit of the pixel circuit during dark sampling, illuminated sampling and energy harvesting, respectively.

of self-powered operation of the system. The associated power management circuit for energy harvesting is integrated in the same die and is discussed in Chapter 8.

9.2 Design of the Energy Harvesting Image sensor

Fig.85(a) shows a conventional logarithmic Active Pixel Sensor (APS) which consists of the primary element, a photodiode (D1) and the control switches. Diode-connected device MN1 provides the logarithmic bias to photodiode while switch MP1 control the correlated

double sampling (CDS) which acts as electronic shutter to control the dark sampling and illuminated sampling time. Source follower amplifier MN2 charges VCOL through read control switch MN3. VCOL is then read by the column read ADC (not shown in the figure).

Fig.85(b) shows the proposed reconfigurable APS with 8-transistor and the photodiode D1. In addition to the switches such as in conventional APS, the proposed APS also has additional switches to provide the reconfigurability of the photodiode. Switches MN4 and MN5 operates in anti-phase to either connect the anode of the photodiode to ground (reverse biasing the diode in image sensing mode) or connect it to the energy harvesting transmission gate TG1(From where energy is extracted. The diode operates in forward bias condition in this phase.). Fig.85(c) shows the layout of the proposed unit pixel. Each pixel is 9μm x 9μm with fill factor of 44%. Without the energy harvesting capability the fill factor would be 54%. The unit pixel is used to create the 12288 pixel sensor array formed by 128 (H) x 96 (V) pixels. For image processing computational advantage, the pixels are grouped in 8x8 pixel arrays which is called pixel blocks. The whole sensor is segmented in 16 horizontal and 12 vertical blocks.

The image sensor operates in two phases for CDS. During first phase, the CDS switch MP1 is turned off [Fig.85(d)]; the only current flows through the diode is the leakage through the MP1. VCOL is read at the end of the dark sampling period. The illumination sampling beings immediately after the dark sampling when MP1 is turned on [Fig.85(e)]. The photodiode is now biased with the current set by MN1. The resulting voltage is sampled at the VCOL at the end of the illuminated sampling phase. The difference between these two values (dark and illuminated sampling voltages) is converted to digital bits by the ADCs. The details of the imaging working principle is discussed in other publications and is out of scope of this dissertation. During energy harvesting shown in Fig.85(f), the cathode of the diode is connected to ground through MN4 and energy is extracted at the V_{EH} node. The V_{EH} nodes of all pixels are shorted to form a single cell photovoltaic cell with approximately 0.44mm^2 effective charge generation area. In this mode, the charge

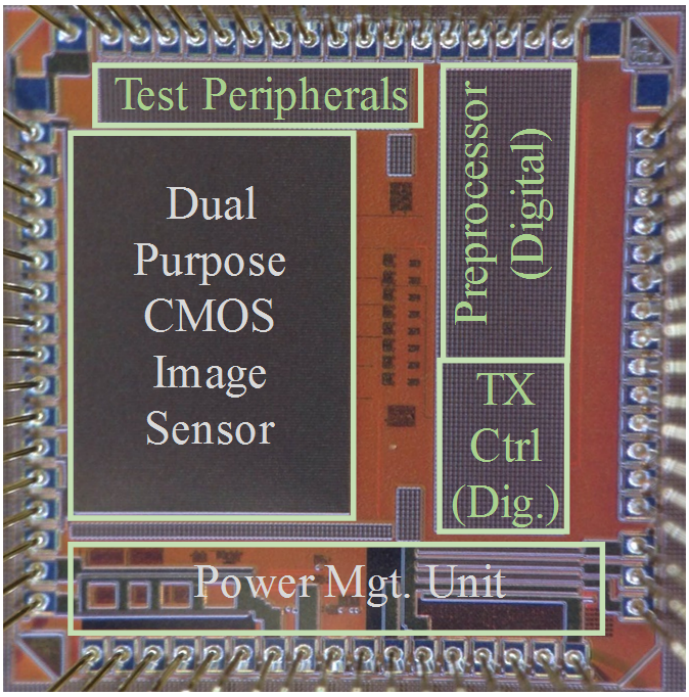


Figure 86: Die photo of the chip showing the sensor and power management unit. The die area is 2mmx2mm; sensor area is $1mm^2$. The PMU is discussed in Chapter 8.

flow in the parallel-configured pixels will be similar to any regular photovoltaic cell. As discussed in the next section, the V_{EH} node is the input of the energy harvesting and voltage regulation unit.

Fig.85(g-i) show the corresponding equivalent circuits of image sensor during dark sampling, illuminated sampling and energy harvesting; respectively.

9.3 Autonomous Mode Management (AMM) for Joint Sensing, Harvesting and Delivery

The AMM controls the switching between imaging and harvesting mode of the sensor (depending on frame rate and energy availability) as well as transitions between the boost and buck mode of the regulators (depending on the priority of the load and battery voltage level). In applications with a target frame rate, a frame rate control signal will cause EH to change from low (sensing) to high (harvesting). A low EH forces buck only operation to enable sensing, processing, and communication of a frame. The high EH on the other

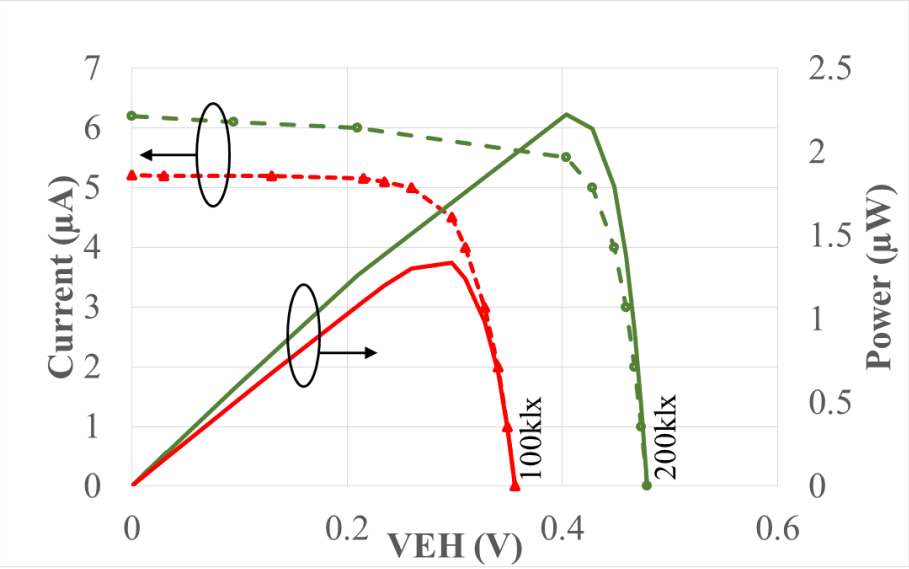


Figure 87: I-V characteristics of the CMOS image sensor.

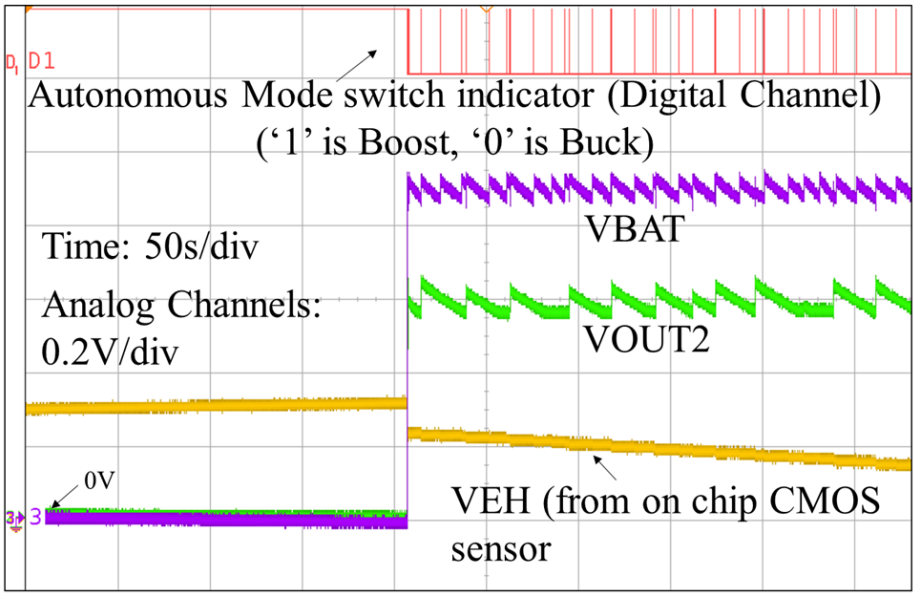


Figure 88: PMU start-up and operation from the voltage generated from the designed CMOS image sensor.

hand, enables both boost and buck operation between sensing two frames. The boost mode is necessary to harvest energy and replenish the energy storage. The buck operation remains necessary for some circuit blocks even between frames. For example, preserving the previous frame data is often required for compressing image with temporal redundancy, and hence, on-chip memory should be powered in between two frame capturing [88]. The

AMM function of the power management unit is discussed in Section 8.5.

In energy autonomous imaging mode, the EH is self-generated by the system. Such decision is made by sensing the voltage drop in the energy storage and assessing how much energy is required to process the next frame. If the energy level in the storage is below that minimum limit, the system decides to harvest before allowing next frame capturing. Thus, in the self-powered case, the frame rate becomes a system defined variable and varies depending on available energy. In practical operation, the demanded frame rate can push the system into sensing but if enough energy is not available, the AMM will stop sensing and will go to harvesting mode.

9.4 Measurement Results

A test-chip in 0.13μm CMOS demonstrates the proposed power management unit (PMU) with integrated CMOS image sensor (Fig. 86). The chip is wire bonded in open cavity LCC 64 package.

Fig. 87 shows the DC I-V profile of the CMOS pixel array during harvesting. It generates 2.1μW of peak power at 200klx luminance. A cool white (7000K) LED lamp 1000 lm is used for photo response measurement.

Fig. 88 shows the PMU harvesting from the image sensor, storing energy in battery and supplying a load domain. The V_{EH} which is connected to the sensor is seen to charge at the beginning, indicating the charging of the capacitor from the sensor current which is reconfigured as a photovoltaic cell for this measurement. As the battery voltage reaches certain threshold, the power management unit is connected to the battery and system starts harvesting. The battery voltage falls due to the charge transfer from the input to the output. The output domain is also starts regulating as soon as the battery voltage reaches the regulation level. It is worth noting that, since the load current is more than the current supplied by the sensor for this measurement, the V_{EH} is seen to fall monotonically. It is hence necessary to isolate the power management unit from the V_{EH} if it is required to replenish the input

Table 8: Comparison with prior arts (Energy harvesting from Sensors)

Item	Law'11 [84]	Wang'15 [85]	Nayar'15 [86]	**This work**
Array	32x32	32x32	30x40	**128x 96**
Pixel size	15x15μm^2	54x48μm^2	2.8x2.8 mm^2	**9x9μm^2**
Fill factor	21%	36%	N/A	**44%**
Generated power	35.6nW	2μW	0.77mW	**2.1μW**

capacitor (V_{EH} node).

Table 8 compares this work with other prior arts on different aspects of the sensor array. To the best of the author's knowledge, this work (in conjunction with the work mentioned in Chapter 8) presents the first ever single-chip demonstration of energy harvesting from a moderately sized CMOS pixel array with integrated power management unit having multiple output domains.

9.5 Summary

This chapter presents a brief discussion on reconfigurable dual-purpose image sensor that performs as imager as well as energy harvesting transducer. This preliminary demonstration opens up future research avenues towards fully energy autonomous, highly integrated sensors those are capable of harvesting in-situ energy and will operate for much longer period without the need of external energy supply.

CHAPTER 10

CONCLUSION

10.1 Dissertation Summary and Contribution

With emerging applications of low power pervasive IoT devices, the demand for efficient energy delivery is of critical importance. This research presents system and circuit level solutions for low power IoT devices. From system level, different performance aspects have been investigated. Topics include stand alone efficiency of an energy harvesting boost regulator, effect of cascading of multiple boost regulator stages on system efficiency, time division multiplexing of a single component between different types of regulator and to generate multiple supply domains in a certain regulator type. Additionally, effect of secondary node control along with primary output control is also explored. From circuit level, major challenges undertaken are design of high duty cycle analog oscillator to achieve high conversion ratio in a single stage regulator, design of bias gating to reduce regulator's self consumption and specific design technique of bias gated circuit blocks.

In Chapter 4 an analog oscillator with very high duty cycle is presented. The oscillator uses an internally generated current based oscillator whose duty cycle depends on the ratio to two similar circuit. Since all components used for the oscillator are internal to the chip, with proper layout matching the circuit achieves highly stable duty cycle which is temperature, bias and process invariant. The oscillator is implemented in a prototype boost regulator designed with PFM based asynchronous mode topology. The implemented boost regulator achieves high conversion ratio by dint of the merit of the oscillator circuit. The high conversion ratio helps the boost regulator to decrease the operating input of system. This is particularly important specially when applied to an energy harvesting application where the input voltage is often widely varying and is usually very low.

Chapter 5 presents a system level solution for improving regulator efficiency by minimizing the self-consumption of the regulator. The PFM mode regulator goes through active

and idle modes and many circuit blocks are not required to operate during idling. By utilizing the inherent operating principle of PFM mode regulator, a bias gating technique is implemented which, during idle mode, cuts off the bias current of selective analog circuit blocks, those are not in required during that time. The primary challenge addressed are the selection of the major blocks those provide significant saving through bias gating. Additionally, the synchronization of the shutting down of the circuit blocks and reviving those during the next active phase are the other challenges discussed in details. Transistor level circuit design of this blocks and how bias gating is implemented inside those blocks are also discussed along with silicon results.

In Chapter 6 a system with two cascaded boost regulator is presented. This system increases the conversion ratio by having two stages in cascaded which helps to reduce the operating input voltage even further. The system also exhibit a dependency of intermediate node control on the overall efficiency. Additionally, the system demonstrates that for very high conversion ratio, a cascaded system offers higher efficiency as opposed to a single stage regulator operating at same conversion ratio. This effect is arises from the inherent dependency of efficiency on conversion ratio for most regulators whose efficiency typically degrades with higher conversion ratio.

Chapter 7 presents an improvement of the design discussed in chapter 6. The cascaded system uses two inductor to achieve the high conversion ratio which burdens the system with higher cost, volume and weight. In the improved system, only one inductor is used. The cascaded system offers similar benefit as discussed in Chapter 6 but uses only one inductor by multiplexing it in between two stages. This solution helps to reduces system size, weight, volume and most like will be less costly.

In Chapter 8 a final system level solution is proposed which encompasses the learnings for previous chapters. This system embeds a boost regulator and a multiple output buck regulator in a compact design. The system explores very high degree of integration both from silicon transistor and external component multiplexing. The system uses only one inductor

and one power stage to perform both the boost and multi-domain buck operation. The system is capable of harvesting from very low input voltage by using the oscillator presented earlier and it incorporates the bias gating technique to minimize the self-consumption. Additionally it uses the inductor multiplexing technique and implements a single inductor multiple output (SIMO) buck regulator design. The multiple output domain enables this system to be used as integrated power management unit for complex IoT devices which houses different types on internal circuit with different output level and power demand. This solution offers an integrated solution for application in a compact form.

Finally, in Chapter 9, a brief discussion on design and demonstration of a dual purpose CMOS APS is presented. In conjunction with the PMU presented in Chapter 8, this discussion lays out initial steps towards self-powered sensors for prolonged operational lifetime.

In conclusion, this research focuses on different aspects of energy delivery and power management for low power applications. Many low power applications run intermittently and have a long idle time in between two consecutive active periods. By combining the PFM mode architecture boost regulator which exhibits similar characteristics, this research explores different challenges such as, improving efficiency, increasing conversion ratio, lowering the operating input voltage and reducing the external component count. Several circuits are proposed along with some system level solutions. A number of prototypes are implemented in 130nm CMOS to demonstrate proposed circuit and system solutions. The outcome of this research is expected to improve the overall understanding of the challenges of efficient energy delivery for very low power applications.

10.2 Future Research Opportunities

Most of the outcome of this work can be implemented immediately to practical applications. Additionally, the findings from this research can be extended in several potential future research.

Chapter 6 offers an insight to the control of intermediate node voltage in a cascaded

regulator and its impact on efficiency. However a circuit level solution is not presented. A possible implementation may include an integrated control circuit discussed briefly in 6.6.5. An advantage of such an implementation is that it offers an autonomous tracking of the most efficient operating point and will probably help to extend the operating time of the load without the battery or the storage being replenished.

An improvement over the system proposed in Chapter 7 is the optimization of the switch sizes used for transmission gates. Since the transmission gates in series with the inductor current, the resistance affects the efficiency. The optimization should be performed based on the load range the regulator is expected to delivery. For each load range the optimization may lead to a different switch size. An integrated control scheme can be developed to control the switch size dynamically that can shade both the switch size and the driver size to improve the efficiency.

The concept of bias gating introduced in Chapter 5 can be extended further by implementing a load dependent, adaptive bias gating controller. An adaptive controller will help to reduce bias current even further by including more critical circuit blocks into bias gating. A major challenge to overcome is to adjust the response time of the regulator as a function of the load. Typically a faster response time is required for higher load range but response time can be relaxed at lower load. As the load changes increases, the controller can release the critical circuit blocks to improve the response time. On the other hand when the load decreases, the critical block can be bias gated; this will increase the response time of the regulator but will offer further bias saving during low load operation and thus improve overall system efficiency.

In broader perspective, the understanding of this research can be extended to analyze systems with multiple output domain and wider load range. In many cases, the individual load domains are optimized for the specific domain. An analytical study for global optimization of multi-domain regulator will lead to a much needed solution for todays low power IoT devices. Additionally, the power management understanding can be coupled

with different features of of specific load and activity pattern to attain high degree of energy autonomy. As an example, the system described in Chapter 8 and Chapter 9 can be extended for autonomous imaging system with variable frame rate which harvests the required energy and depending on the available energy can adjust the frame rate and image quality. Such level of energy autonomy will lead to more efficient, pervasive and wide spread deployment of environmental and remote sensors.

APPENDIX A

PUBLICATION LIST

Journal:

- **K. Z. Ahmed**, and S. Mukhopadhyay, "A 190nA Bias Current 10mV Input Multi-Stage Boost Regulator with Intermediate Node Control to Supply RF Blocks in Self-powered Wireless Sensors," *IEEE Transactions on Power Electronics*, vol.31, no.2, pp.1322-1333, Feb. 2016.

- **K. Z. Ahmed**, and S. Mukhopadhyay, "A wide conversion ratio, extended input 3.5A Boost Regulator with 82% Efficiency for Low Voltage Energy Harvesting," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4776-4786, Sep. 2014.

Conference:

- **K. Z. Ahmed**, and S. Mukhopadhyay, "A Single-Inductor-Cascaded-Stage Topology for High Conversion Ratio Boost Regulator," in *The 34th IEEE International Conference on Computer Design (ICCD)*, Oct. 2016.

- **K. Z. Ahmed**, M. F. Amir, J. H. Ko , and S. Mukhopadhyay, "Reconfigurable 96x128 Active Pixel Sensor with 2.1μW/mm^2 Power Generation and Regulated Multi-domain Power Delivery for Self-Powered Imaging," in *2016 European Solid-State Circuits Conference (ESSCIRC)*, Sept. 2016.

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