MODELING AND SIMULATION OF SILICON INTERPOSERS FOR 3-D INTEGRATED SYSTEMS

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MODELING AND SIMULATION OF SILICON INTERPOSER FOR 3-D INTEGRATED SYSTEMS

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To my family

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CHAPTER 1

INTRODUCTION

1.1 Background

Three-dimensional (3-D) system integration is believed to be a promising technology and has gained tremendous momentum in the semiconductor industry recently. The concept of 3-D integrated circuits is shown in Figure 1. In 3-D ICs, multiple dies are stacked, and vertical interconnections between dies are realized by through-silicon vias (TSVs). These TSVs are the core technology that replace long interconnects in 2-D ICs with short vertical interconnects. The shortened wire can result in low wire delay, less parasitic effects and higher clock frequency [1-3] than 2-D ICs, thereby improving the overall system performance. In addition, it is possible with 3-D heterogeneous integration to stack different functional modules, including memory, MEMS, antenna, RF, analog/digital blocks into a package. Among all the components in the 3-D system as shown in Figure 1, the silicon interposer with TSVs and redistribution layer (RDL) traces is a key enabler and thus needs to be carefully designed to achieve optimal system performance [4]. As a result, the fast and reliable simulation of the interconnections in the silicon interposer is a necessity to speed up the design cycle time, while maintaining accuracy of the results.

1.2 Motivation

The silicon interposer is expected to have high input/output counts, fine wiring lines and many TSVs. Modeling and design of the silicon interposer can be challenging due to the following reasons: (1) Silicon substrate is not an ideal medium for signal transmission since the interconnections and TSVs are exposed to additional losses due to leakage. (2) TSVs are multi-scale structures with oxide thickness less than one micron and aspect

ratio of 1:20 or higher. (3) Hundreds of interconnects routed with fine pitch on silicon substrates will cause enhanced coupling between signal lines, which can introduce distortion. (4) The insulating oxide layer around TSVs and below the RDL traces also influence the characteristics of interconnections, causing frequency-dependent parasitic effects. (5) The resistance and conductance of TSVs is temperature dependent because of the temperature-dependent conductivity [5]. Moreover, TSVs connected to multiple long RDL transmission lines will lead to frequent signal-via transitions in the silicon interposer, which results in combined signal and power integrity issues. As a result, modeling the interconnect response of high-density signal paths with TSVs in the silicon interposer is becoming a critical task.

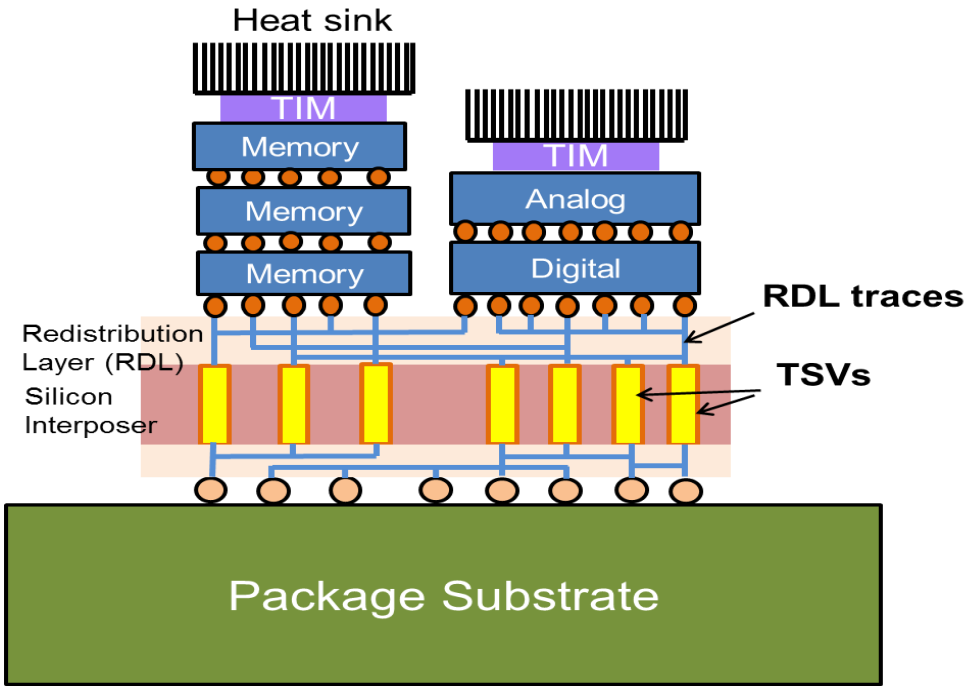


Figure 1. Silicon interposer with TSVs and RDL traces in 3-D systems.

1.3 Contributions

This dissertation mainly focuses on developing an efficient modeling approach for silicon interposers in 3-D systems. The contributions of the research are listed as follows:

1. The investigation of the coupling effects in large TSV arrays. The importance of coupling between TSVs for low resistivity silicon substrates is quantified both in frequency and time domains. This has been compared with high resistivity silicon substrates. The comparison between the two indicates the importance of jitter and voltage analysis in TSV arrays for low resistivity silicon substrates due to enhanced coupling.

2. The development of an electromagnetic modeling approach for non-uniform TSVs. To model the complex TSV structures, an approach for modeling conical TSVs is proposed first. Later a hybrid modeling method which combines the conical TSV modeling method and cylindrical modeling method is proposed to model the non-uniform TSV structures.

3. The development of a hybrid modeling approach for power delivery networks (PDN) with through-silicon vias (TSVs). The proposed approach extends multi-layer finite difference method (M-FDM) to include TSVs by extracting their parasitic behavior using an integral equation based solver. Using the proposed modeling technique the power/signal integrity of the PDN with TSVs/through-glass vias (TGVs) in lossy silicon interposers and low loss glass interposers is investigated and compared.

4. The development of an efficient approach for modeling signal paths with TSVs in silicon interposers. The proposed method utilizes the 3-D finite-difference frequency-domain (FDFD) method to model the redistribution layer (RDL) transmission lines. A new formulation on incorporating multiport networks into the 3-D FDFD formulation is presented to include the parasitic effects of TSV arrays in the system matrix.

5. The development of a 3-D FDFD non-conformal domain decomposition method (DDM). The proposed method allows modeling individual domains independently using the FDFD method with non-matching meshing grids at interfaces. This non-conformal DDM is used to model interconnections in silicon interposers.

1.4 Organization of the Dissertation

This dissertation consists of nine chapters. In Chapter 1, the background and motivation, contributions, and the organization of this dissertation are introduced. In Chapter 2, the research problem to be addressed and prior arts that have been developed are investigated. In Chapter 3, the coupling effects in large TSV arrays are investigated, and the coupling effects in low resistivity and high resistivity silicon substrates are compared. In Chapter 4, a modeling approach for non-uniform TSVs is proposed. In Chapter 5, a modeling approach for the power delivery network with TSVs is proposed and the simultaneous switching noise (SSN) in silicon and glass interposers are analyzed. In Chapter 6, an efficient approach for modeling the signal paths with TSVs in silicon interposers is presented, this approach uses finite-difference frequency domain (FDFD) technique coupled with an integral equation based method where the latter is applied to TSVs. In Chapter 7, the 3-D FDFD non-conformal domain decomposition method is proposed and used to model the interconnections in silicon interposers. Chapter 8 presents the possible future work. Finally, the conclusion and summary of the research work in this dissertation are presented in Chapter 9.

CHAPTER 2

ORIGIN AND HISTORY OF THE PROBLEM

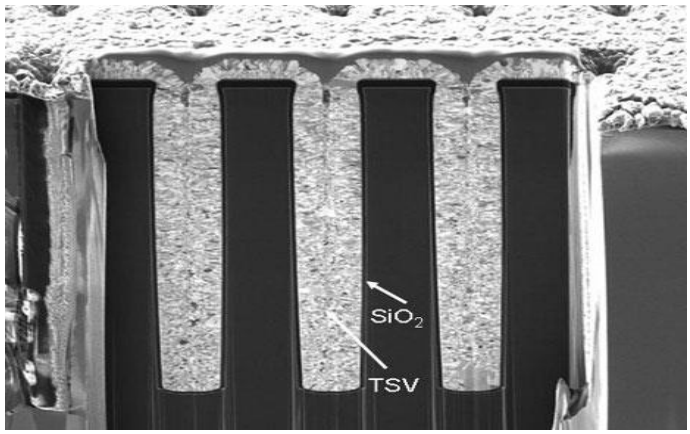
2.1 Introduction

To design high-speed signal paths with TSVs in silicon interposers and perform signal/power integrity analysis for 3-D systems, the electrical model of TSVs must be obtained using design parameters such as material and geometric information. Then, this electrical model can be used to obtain overall system performance. Therefore, many approaches have been proposed for modeling and analysis of TSVs. In this chapter, the prior research for electrical modeling of TSVs is introduced.

2.2 Lumped Element based TSV Modeling

Figure 2 shows a typical structure of TSVs [6]. The conductor core of TSV usually is made of copper or tungsten. A thin oxide liner layer is deposited around the conductor. For the lumped element based TSV modeling, an equivalent circuit model can be constructed from physical intuition using an $RLCG$ element [7]. The model contains series resistance and inductance of copper conductors, shunt oxide capacitance, and shunt silicon admittance. The value of each component is found by tuning the circuit element to fit its frequency response with measurement data using the parameter optimization method. Since this model is not tied to the geometrical and physical parameters of TSVs, several approaches are presented to obtain the closed-form formulae for the $RLCG$ elements in the equivalent circuit model [7-11]. The π-type equivalent circuit is shown in Figure 3, where R and L denote the per-unit-length (p.u.l.) resistance and inductance of the TSV, C_{ox} denotes the p.u.l. capacitance due to the oxide liner, and C_{si} and G_{si} denote the p.u.l. capacitance and conductance of the silicon substrate. However, these resistance-inductance models were not rigorously derived and did not consider the non-

uniform current distribution in TSV conductor caused by adjacent TSVs, therefore it can not capture all the semiconductor effects. This equivalent circuit model was again investigated in [12], where rigorous closed-form formulae for the resistance and inductance of TSVs are derived from the magneto-quasi-static theory with a Fourier-Bessel expansion approach. This equivalent-circuit model can capture the important parasitic effects of TSVs, including skin effect, proximity effect and lossy silicon effects. It can generate accurate results comparable to 3-D full-wave solvers. The equivalent circuit model is extended in [13] to consider all the parasitic components of the TSV, where a scalable electrical model of TSVs including bump and RDL traces was proposed. Although lumped element modeling can provide reasonable good results for the insertion loss, it becomes difficult to extend this method to model large TSV arrays since the current distribution in one TSV conductor will be affected by all the other adjacent TSVs and becomes non-uniform in high-density TSV arrays, it is difficult to use analytical equations to accurately account for the complex current distribution in TSVs and capture all the coupling effects between TSVs. Hence a full wave analysis method is required that is scalable to multiple TSVs as in arrays. Because of the multi-scale dimensions of TSVs (oxide thickness and aspect ratio), this becomes a very challenging task and is a major bottleneck for commercially available EM solvers where large arrays of TSVs must be modeled.



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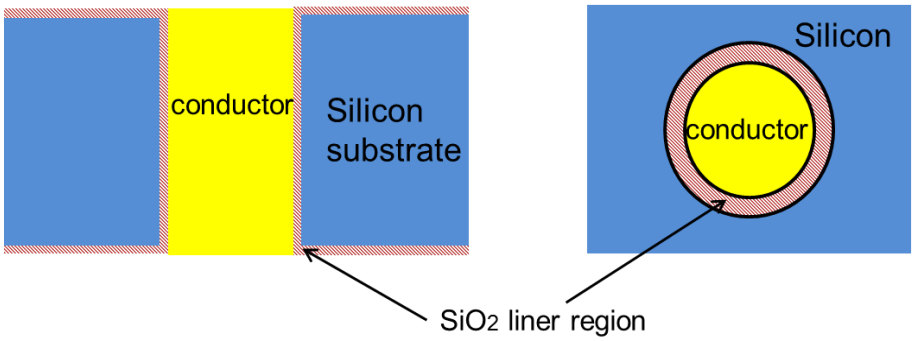
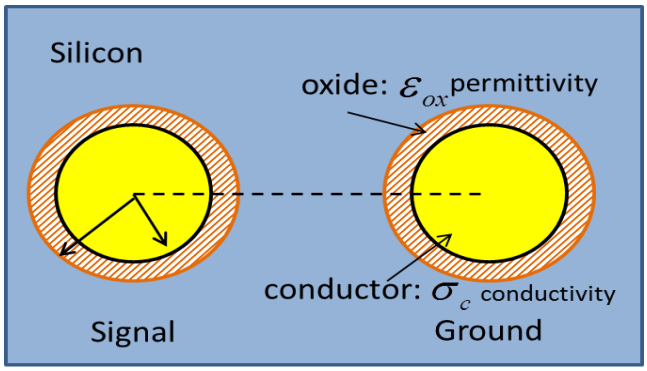


(b)

Figure 2. Typical TSV structure (a) Cross-section SEM image of TSVs (b) cross-section and top view of a single TSV.



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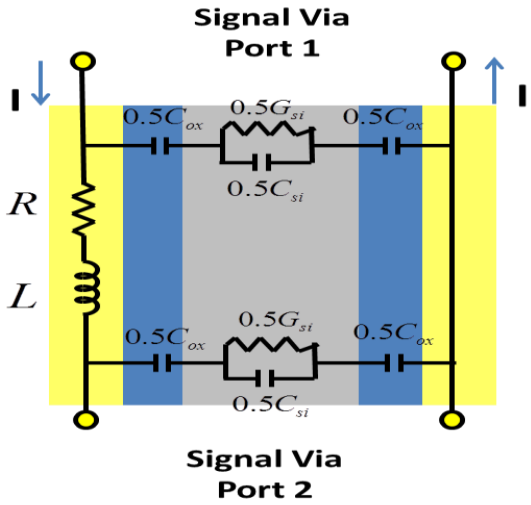


(b)

Figure 3. A signal-ground TSV pair (a) Cross-section view (b) $\pi-$type equivalent circuit model

2.3 Electromagnetic Modeling of TSVs

To address the problem of modeling large TSV arrays, a modeling method based on solving Maxwell's equations in integral form is proposed in [14-16]. In this approach, specialized basis functions which approximate the current and charge in the TSVs are derived. Using these basis functions, the electrical response of the structure can be extracted by solving Maxwell's equations. The modeling flow is shown in Figure 4. This proposed method can generate equivalent $RLCG$ parameters of TSVs that represent the following parasitic elements.

(1) Conductor series resistance and inductance: This represents the loss and inductive coupling in copper conductors, which are due to the volume current density distribution. The conductor series impedance can be extracted by solving the electric field integral equation (EFIE) with cylindrical conduction mode basis functions (CMBFs) [14].

(2) Substrate parallel conductance and capacitance: This represents the loss and capacitive coupling between conductor and insulator surfaces, which is produced by the surface charge density distribution on the conductor and dielectric surfaces. The parallel admittance can be extracted by solving the scalar potential integral equation (SPIE) with cylindrical accumulation mode basis functions (AMBFs). The conductance terms can be computed by using the complex permittivity for silicon defined as in equation (1) [17]:

$$\varepsilon_{si} = \varepsilon_0 \varepsilon_{si,i}(1 - j\tan\delta - j\frac{\sigma_{si}}{\omega\varepsilon_0\varepsilon_{si,i}}) \tag{1}$$

where ε_{si} is the dielectric constant, σ_{si} is the conductivity of silicon and $\tan\delta$ is the intrinsic loss tangent.

(3) Excess capacitance in oxide liner: This represents the effect of the insulator between conductor and silicon substrate, which originates from polarization current in the insulator. The new basis functions, called polarization mode basis functions (PMBFs),

[15] are proposed to capture the polarization current density distribution. The excess capacitance is extracted by solving EFIE with PMBFs.

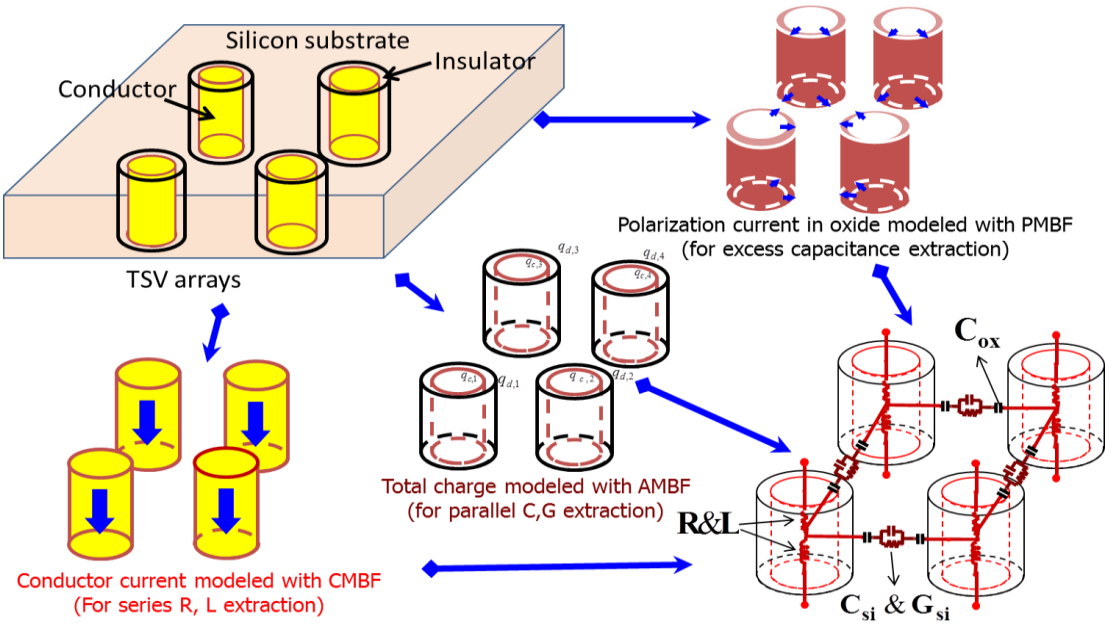


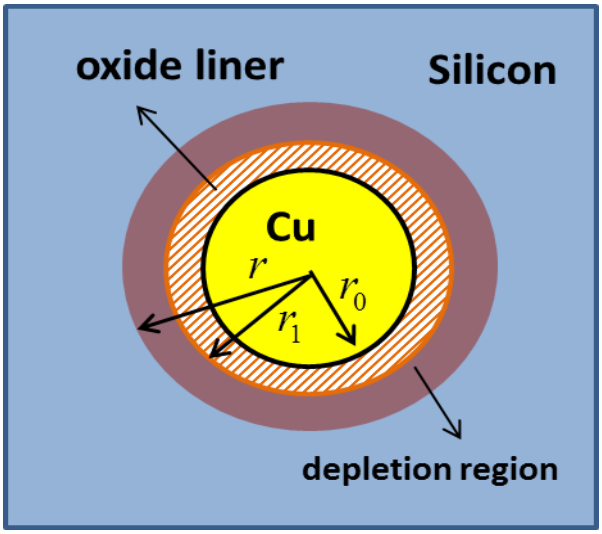
Figure 4. Modeling procedure for 2×2 TSV arrays [16].

All of these elements can capture the non-uniform effect of charge and current distribution in the TSVs, which depends on the proximity of the neighboring TSV interconnections. As illustrated in Figure 4, the extracted individual elements are combined to generate the complete equivalent circuit model of the entire TSV structure. A major challenge in modeling TSVs arises from the multi-scale dimensions of TSV structure due to the thin oxide thickness, aspect ratio and the need for modeling multiple TSVs. Using the specialized basis functions described above eliminates the need for meshing the structure and therefore is computationally less expensive and memory efficient.

2.4 MOS Capacitance in TSVs

To obtain a rigorous model of TSVs, the voltage-dependent MOS capacitance of TSVs should be considered. The TSV shown in Figure 5(a) consists of a cylindrical conductor surrounded by an oxide liner embedded in a silicon substrate, which is a cylindrical

metal-oxide-semiconductor (MOS) structure. Such a TSV under bias condition exhibits a capacitance behavior similar to a planar MOS capacitor [18]. Figure 5(b) shows a typical capacitance (C_g) plot with change in the gate voltage (V_g) for a planar MOS capacitor. As shown in Figure 5(b), at high gate voltage the MOS capacitance has three possibilities: deep depletion, high frequency, and low frequency.



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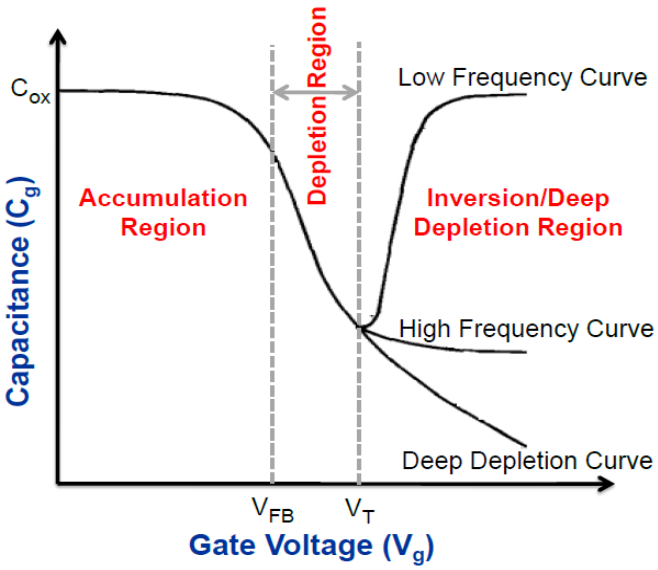


(b)

Figure 5. (a) Schematic cross section of a TSV biased in the depletion region (b) Capacitance-voltage plot for a planar MOS capacitor.

The first analytical model of the MOS capacitance effect is proposed in [19]. This analysis is performed by analytically solving Poisson's equation assuming full depletion approximation (FDA). The FDA simplifies the analysis by assuming that the depletion region (formed in the semiconductor) is fully depleted (i.e. there are no mobile charge carriers in the depletion region).

The full depletion approximation enables a simple analysis but it does not provide the most accurate result. A more accurate electrical model of a TSV is presented in [20]. This method performs exact analysis by solving Poisson's equation numerically in cylindrical coordinate using the Runge-Kutta method [21].

2.5 Modeling of RDL traces on silicon interposer

In the silicon interposer, signal paths often consist of TSVs and RDL transmission lines. When designing the signal paths with TSVs in a silicon interposer, the RDL is an essential component that should be considered with the TSV. Therefore, modeling and analysis of RDLs is also important for 3D system design. An analytical model for a RDL is proposed in [13]. In this approach, RDL traces are modeled using analytical equations. A RDL structure on a dielectric layer with structure parameters is shown in Figure 6 and the proposed equivalent circuit model is shown in Figure 7. An electrical model of the signal paths in the silicon interposer can be obtained by combing this analytical model of RDLs with the analytical model of TSVs discussed in the previous section. However, this model is mostly analytical and limited to a few interconnects. Efficient approaches for modeling a large number of RDLs and TSVs therefore need to be investigated.

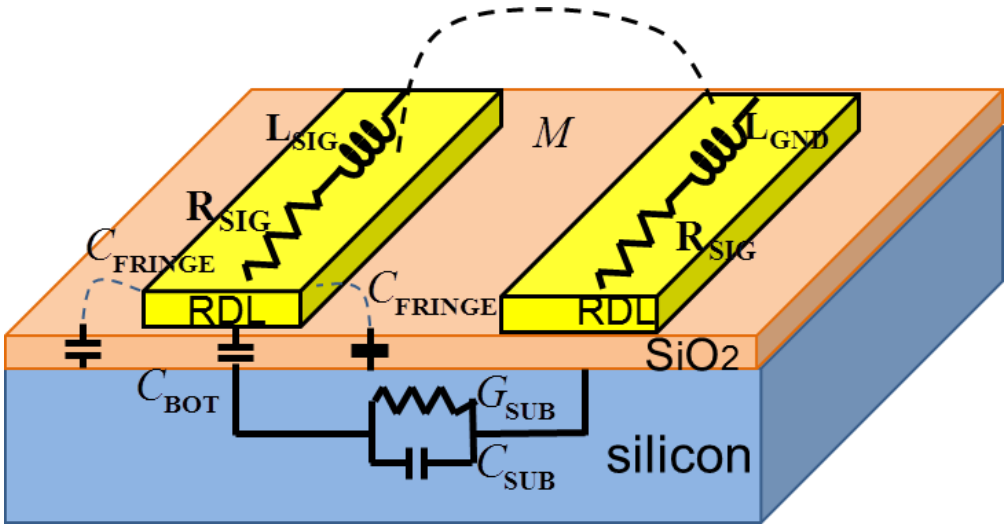


Figure 6. RDL structure on dielectric layer with its structure parameters

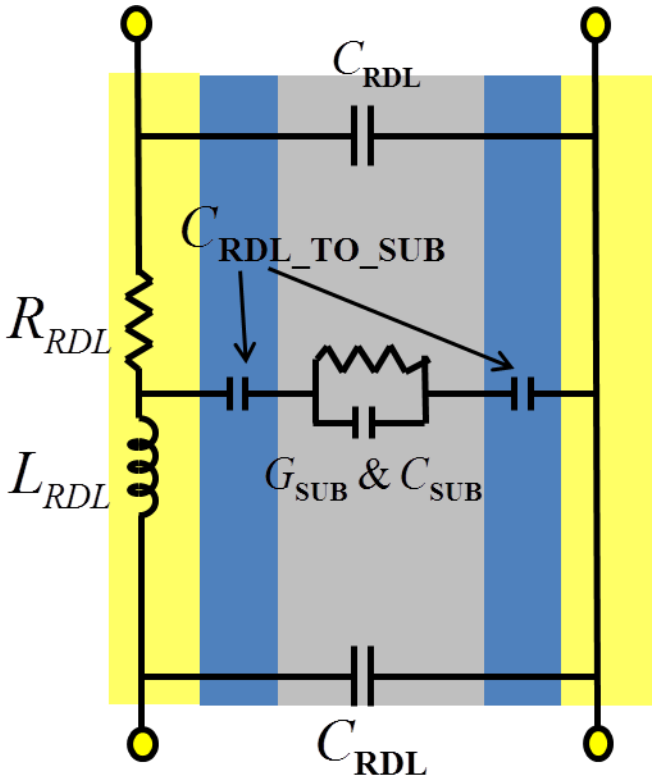


Figure 7. The equivalent circuit model of the RDL traces.

2.6 Technical Focus of This Dissertation

The investigation of the prior arts for TSV modeling provides the understanding of the advantages and limitations of existing modeling techniques. With the evolution of 3-D integration, efficient modeling tools are needed to facilitate 3-D IC designs. The technical focus of this dissertation is summarized as follows:

1. The investigation of the coupling effects in large TSV arrays. The importance of coupling in large TSV arrays is quantified in both time domain and frequency domain.

2. The development of a modeling approach for non-uniform TSVs

3. The development of a hybrid modeling approach for a power delivery network with TSVs.

4. The development of an efficient approach for modeling signal paths with TSVs in silicon interposers.

5. The development of the 3-D FDFD non-conformal domain decomposition method and its application for modeling interconnections in silicon interposers.

2.7 Summary

This chapter introduces the origin and history of the research. It reviews previous modeling approaches for the interconnections in silicon interposer. Several lumped TSV/RDL modeling approaches are briefly introduced and later an electromagnetic modeling approach for TSVs arrays is investigated. The advantages and limitations of these previous modeling approaches are also provided. The limitations of existing modeling approaches for the interconnections in silicon interposer motivate the technique research in this dissertation.

CHAPTER 3

COUPLING ANALYSIS OF LARGE TSV ARRAYS USING SPECIALIZED BASIS FUNCTIONS

3.1 Introduction

A TSV pair with dimensions is shown in Figure 8. Unlike vias in packages and PCBs, TSVs are embedded in a lossy silicon substrate and surrounded by a thin oxide liner. Therefore, the TSV-to-TSV coupling path will include the TSV conductor, oxide liner, and silicon substrate, which is more complicated and significant than traditional wire coupling [22]. The coupling of the TSV pair shown in Figure 8 is examined and Figure 10(a) shows the coupling S-parameter of this TSV pair. We use this TSV pair to perform transient simulation and obtain the coupled noise at the victim TSV. The configuration of the transient simulation is shown in Figure 9 and the simulation results show that the coupled noise can reach up to 150mV, which can not be neglected, as shown in Figure 10(b).

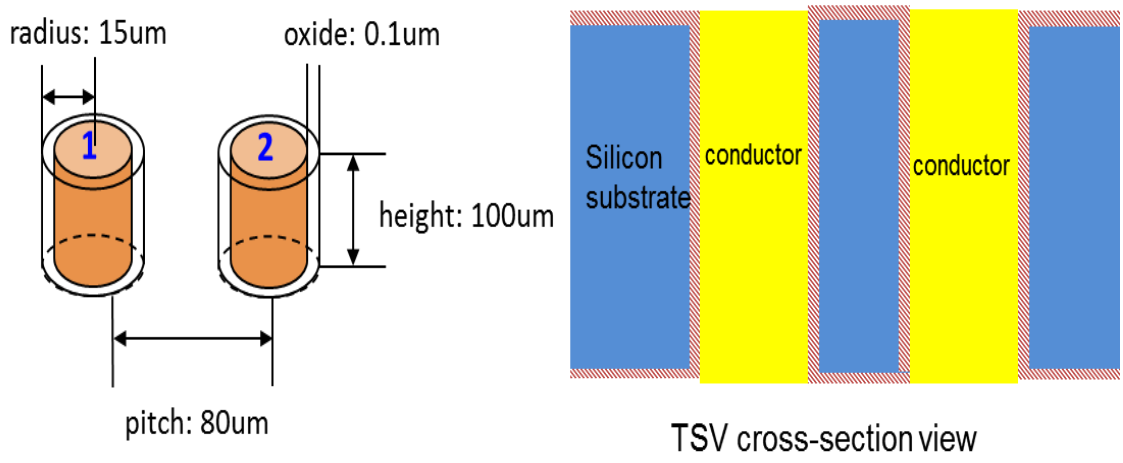


Figure 8. TSV pair with dimensions

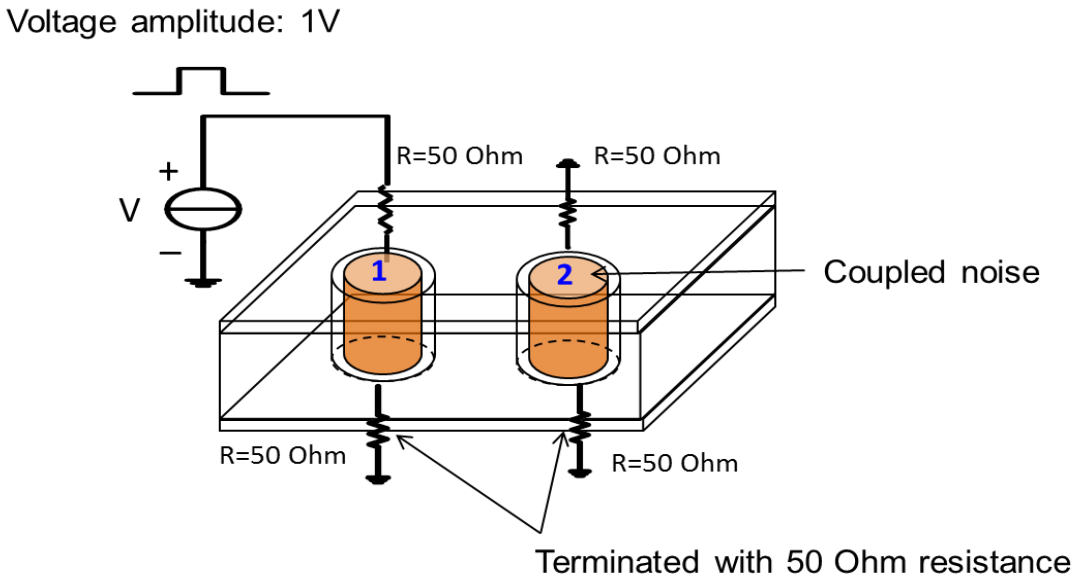
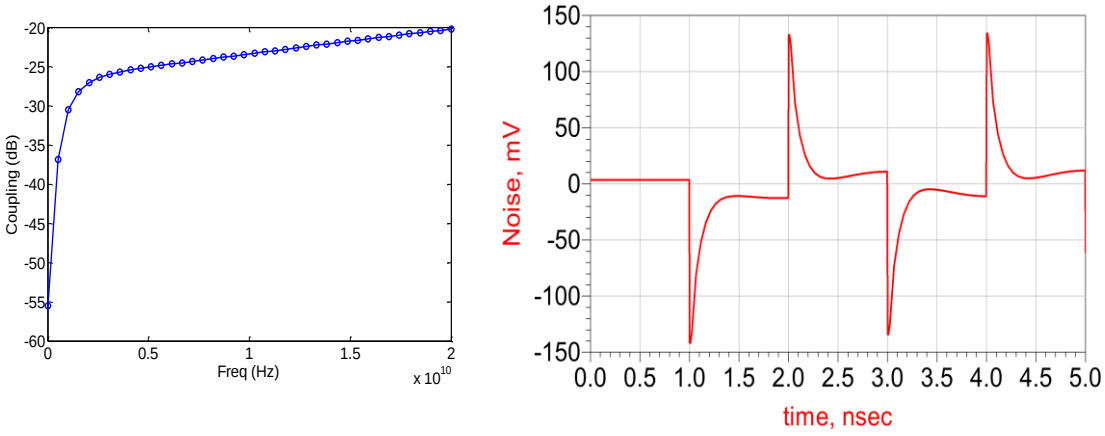


Figure 9. Transient simulation setup for TSV pair.



(a) (b)

Figure 10. (a) Coupling for TSV pair, (b) Coupled noise obtained at TSV-2.

Because of the high integration density of interconnections in 3D stacked ICs, a large number of TSVs need to be used in the silicon interposer package. The coupling between TSVs in TSV arrays become more complicated since one victim TSV is surrounded by many aggressor TSVs, therefore, it is very difficult to estimate the coupling in large TSV arrays. This chapter focuses on analyzing TSV arrays and provides details on the coupling effects in large TSV arrays [23, 24].

3.2 TSV Modeling With Cylindrical Modal Basis Functions

This section describes the TSV modeling method used in TSV array coupling analysis. This method can generate equivalent *RLCG* parameters of TSVs by classifying TSV structures into the following three parts: (1) Conductor series resistance and inductance: this represents the resistive loss and inductive coupling of the copper conductor, which can be extracted by using the electric field integral equation (EFIE) [3] with cylindrical conduction mode basis functions (CMBFs) [4], (2) Substrate parallel conductance and capacitance: this represents the resistive loss and capacitive coupling in the substrate, which can be extracted by using the scalar potential integral equation (SPIE) with cylindrical accumulation mode basis functions (AMBFs) [5], (3) Oxide liner excess capacitance, this represents the capacitive coupling between the conductor and substrate, which can be extracted by using the EFIE with new basis functions called polarization mode basis functions (PMBFs).

Since the details of the modeling are discussed in previous work [2], we briefly describe the three parts of the extraction procedure using different basis functions.

3.2.1 Conductor Series Resistance and Inductance Extraction

The EFIE equation used in the inductance and resistance extraction is given by [5]

$$\frac{\vec{J}(\vec{r},w)}{\sigma} + j\frac{\omega u}{4\pi}\int_{V'} G(\vec{r},\vec{r'})\vec{J}(\vec{r'},\omega)dV' = -\nabla\Phi(\vec{r},\omega) \tag{2}$$

The current density of a conductor segment j can be approximated using the following equation

$$\vec{J}_j(\vec{r},\omega) \cong \sum_{n,q} I_{jnq}\vec{w}_{jnq}(\vec{r},\omega) \tag{3}$$

where $\vec{w}_{jnq}(\vec{r},\omega)$ is the basis function in conductor segment *j* with order *n* and orientation *q*.

After inserting the approximation (3) into the current density term in (2) and applying the inner product (4) based on Galerkin's method,

$$\left\langle \vec{w}_{imd}(\vec{r},\omega), \vec{x} \right\rangle = \int_V \vec{w}^*_{imd}(\vec{r},\omega)\cdot\vec{x}dV \tag{4}$$

the following equivalent voltage equation (5) can be obtained.

$$\sum_{n,q} I_{jnq}R_{imd,jnq} + j\omega\sum_{n,q} I_{jnq}L_{imd,jnq} = \Delta V^j_{imd} \tag{5}$$

where $R_{imd,jnq} = \frac{1}{\sigma}\int_{V_i} \vec{w}^*_{imd}(\vec{r}_i,\omega)\cdot\vec{w}_{jnq}(\vec{r}_j,\omega)$,

$$L_{imd,jnq} = \frac{\mu}{4\pi}\int_{V_j}\int_{V_i} \vec{w}^*_{imd}(\vec{r}_i,\omega)\cdot\vec{w}_{jnq}(\vec{r}_j,\omega)\frac{1}{\left|\vec{r_i}-\vec{r_j}\right|}dV_j dV_i$$

and

$$\Delta V^j_{imd} = -\frac{1}{\sigma}\int_{S_i}\Phi_j(\vec{r}_i)\vec{w}^*_{imd}(\vec{r}_i,\omega)\cdot d\vec{S_i}$$

In the above equations, *i*, *m*, *d* represent the index of the inductive cell, the order of CMBF and the orientation of CMBF, respectively. $\vec{w}_{imd}(r_i,\omega)$ is the cylindrical CMBF with the *(i, m, d)-th* order.

3.2.2 Substrate Parallel Conductance and Capacitance Calculation

The SPIE equation used for substrate parallel conductance and capacitance calculation is expressed as:

$$\frac{1}{4\pi\varepsilon_0}\int_{V'} G(\vec{r},\vec{r'})q(\vec{r'},\omega)dV' = \Phi(\vec{r},\omega) \tag{6}$$

By inserting the charge density distribution function $q = \sum_{n=0} Q_{knq} v_{knq}$ and applying the inner product

$$\left\langle \vec{v}_{lmd}(\vec{r},\omega), \vec{x} \right\rangle = \int_S v_{lmd}(\vec{r},\omega) x dS \tag{7}$$

the following equation (8) can be deduced from the SPIE (6).

$$\sum_{lnq} P^{C,D}_{kmd,lnq,} Q_{lnq} = \Phi^{C,D}_{kmd} \tag{8}$$

where $P^{C,D}_{kmd,\ln q} = \frac{1}{4\pi\varepsilon_{si}} \int_{S_l} \int_{S_k} v_{kmd}(\vec{r_k}) v_{\ln q}(\vec{r_l}) \frac{1}{\left|\vec{r_i} - \vec{r_j}\right|}$.

Here, k, m, d represent the index of the conductor number, modal order and orientation, respectively. $P^{C,D}_{kmd,\ln q}$ is the partial potential coefficient between the (k,m,d)-th and (l,n,q)-th order modes. The superscripts *C* and *D* represent the conductor surface and insulator surface of the TSV, respectively.

3.2.3 Oxide Liner Excess Capacitance Extraction

The EFIE equation used for the extraction of the excess capacitance in oxide liner is given by

$$\frac{\overrightarrow{J^P}(\vec{r},\omega)}{j\omega\varepsilon_0(\varepsilon_{ox}-\varepsilon_{si})}+j\omega\frac{u}{4\pi}\int_{V'}G(\vec{r},\vec{r'})\overrightarrow{J^P}(\vec{r'},\omega)dV'=-\nabla\Phi(\vec{r},\omega) \tag{9}$$

Using a similar process as for inductance and resistance extraction, the following equation (10) can be deduced from (9), expressed as

$$\sum_{l,n,q}I_{\ln q}\frac{1}{j\omega C^{ex}_{kmd,\ln q}}+\sum_{l,n,q}j\omega L_{kmd,\ln q}I_{\ln q}=\int_{V_k}\vec{u}_{kmd}\cdot(-\nabla\Phi)dV_k \tag{10}$$

where $C^{ex}_{kmd,\ln q}=\dfrac{\varepsilon_0(\varepsilon_{ox}-\varepsilon_{si})}{\int\vec{u}_{kmd}\cdot\vec{u}_{\ln q}dV_k}$

and

$$L_{kmd,\ln q}=\frac{\mu}{4\pi}\int_{V_k}\int_{V_l}G(\vec{r_k},\vec{r_l})\vec{u}_{kmd}(\vec{r}_k)\cdot\vec{u}_{\ln q}(\vec{r}_l)\frac{1}{\left|\vec{r_i}-\vec{r_j}\right|}dV_ldV_k$$

Here, k,m,d also represent the index of conductor number, modal order and orientation respectively.

Equations (5), (8), and (10) can be combined into a large matrix equation, which relates the terminal currents and nodal voltages to the modal circuit elements consisting of the conductor *R-L* elements, the parallel conductance and capacitance in the substrate, and the excess capacitance in the oxide liner. Since this TSV modeling method uses a small number of global modal basis functions, it is more efficient than the full wave commercial EM solvers available and has been correlated with other results in [16]. Moreover, since this method is scalable, it can be easily extended to arrays of TSVs. In the following section, the TSV modeling method described is used to obtain the model for a large TSV array, which has then been used for coupling analysis in this chapter.

3.3 Characteristics of Coupled Waveform in TSV Array

The flow of the proposed transient coupling analysis approach is shown in Figure 11. This method starts by obtaining a TSV array frequency domain model. Once the model is obtained, it is converted to a Spice sub-circuit model which can be used for time domain simulation in Hpsice. This is done using Idem [25] which enables the development of a macromodel by preserving passivity and causality. After generating the Spice sub-circuit model, the effects of waveform coupling in the TSV array can be obtained by performing time domain simulation. All transient simulations are performed using Hspice.

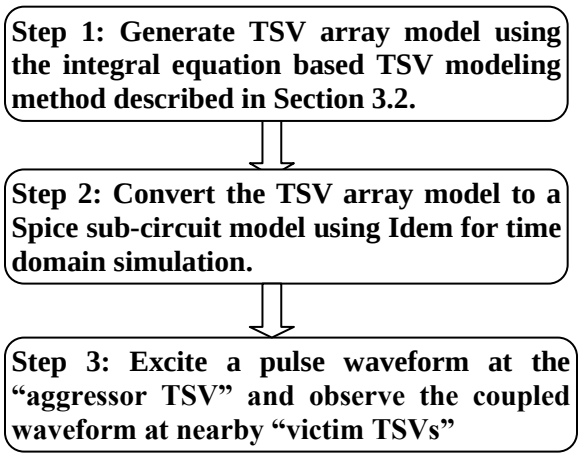


Figure 11. Modeling flow for coupled TSV analysis.

The structure for TSV coupling analysis is shown in Figure 12. To perform coupling analysis, a TSV array model is first generated using the integral equation based TSV modeling method described in Section 3.2 [16]. In this example, we generate a 5×5 TSV array model of the structure shown in Figure 12. The dielectric constants of silicon and silicon dioxide used were 11.9 and 3.9, respectively. The copper conductivity used is $\sigma = 5.8\times10^{7}\,S/m$. The TSV diameter, substrate thickness and oxide thickness are $20\,\mu$m, $200\,\mu$m and $0.1\,\mu$m, respectively. Before performing the transient analysis, the S-parameter model of the TSV arrays obtained using the modeling approach is examined.

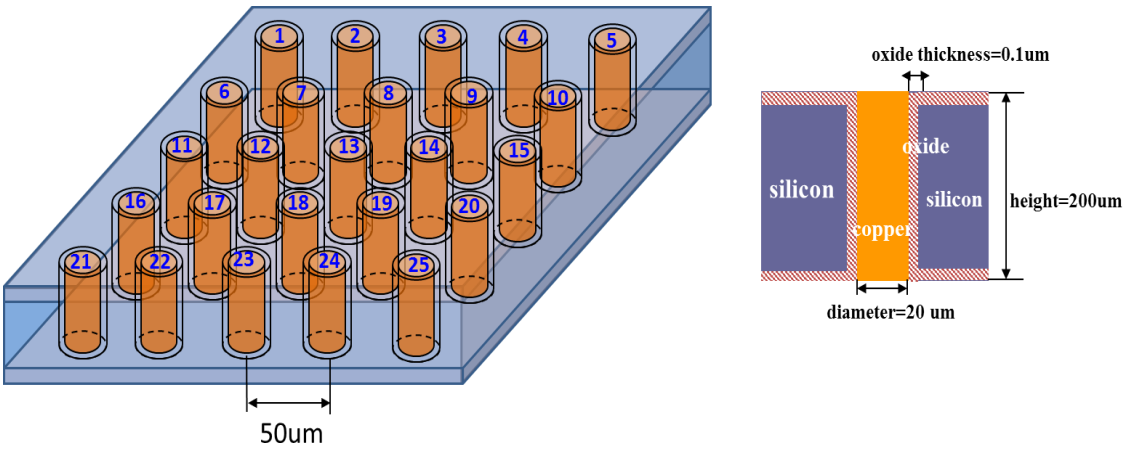


Figure 12. 5×5 **TSV array structure**.

The coupling between TSV-1 and other TSVs (TSV-2, TSV-3, TSV-5, TSV-25) is shown in Figure 13. The frequency range is from 1000 Hz to 10 GHz. It can be seen that the isolation is high and the coupling has a sharp slope at low frequency. As frequency further increases, it shows a positive ramp, indicating that the coupling increases with frequency.

The insertion loss of TSV-1 is shown in Figure 14. It illustrates that there is significant signal loss and the insertion loss increases rapidly to 1.1 dB at 1 GHz. The sharp slope of the insertion loss at low frequency is due to the small oxide liner thickness resulting in a larger oxide capacitance, which provides a leakage path to the silicon substrate [26]. As frequency increases, the insertion loss shows a negative slope, indicating the signal loss increases with frequency.

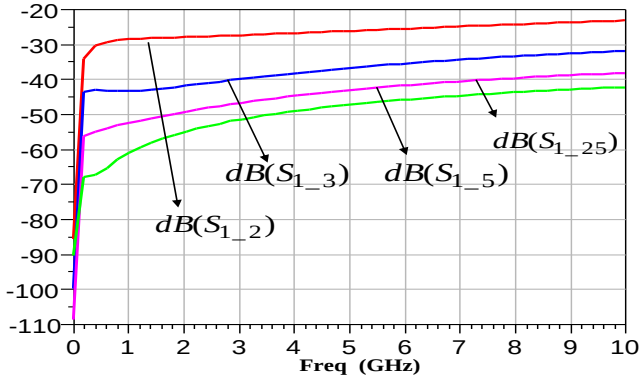
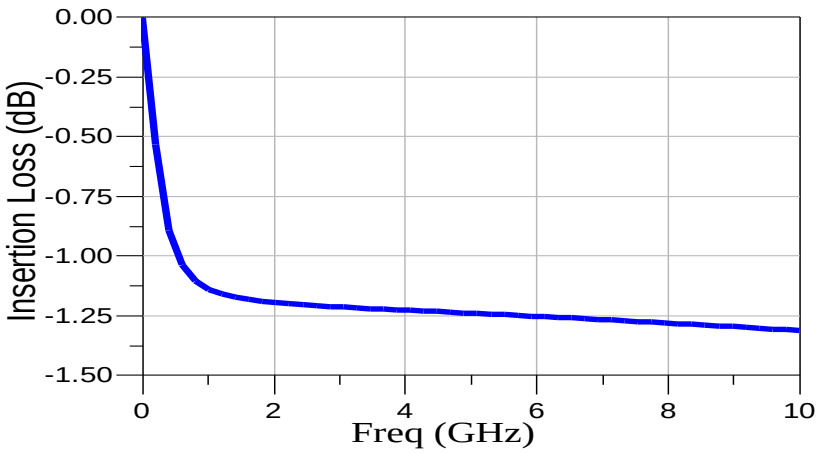


Figure 13. Coupling between different TSV pairs.



(b)

Figure 14. Insertion loss of TSV-1.

The structure for TSV coupling analysis is the same as shown in Figure 12. The configuration of TSVs in the coupling analysis is shown in Figure 15. In the TSV array, TSV-1 is defined as "aggressor TSV", which is excited with one pulse with 2 V magnitude and 10 ns width. The pulse rise and fall times are both 0.1 ns. All the other TSVs other than ground TSVs in the array are defined as "victim TSVs", which are terminated with 50 Ohm resistors on both sides, as shown in Figure 15.

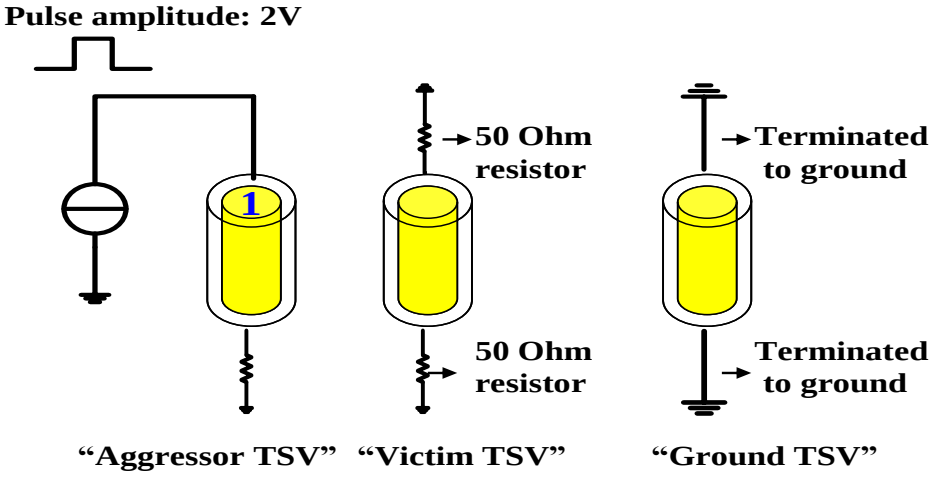


Figure 15. Configuration of TSVs in coupling analysis.

Three different test cases are simulated and compared: (a) silicon substrate conductivity is 10 S/m and no ground TSV is used; (b) silicon substrate conductivity is changed to

0.01 S/m and no ground TSV is used; (c) silicon substrate conductivity is 10 S/m and ground TSVs are used, as shown in Figure 16.

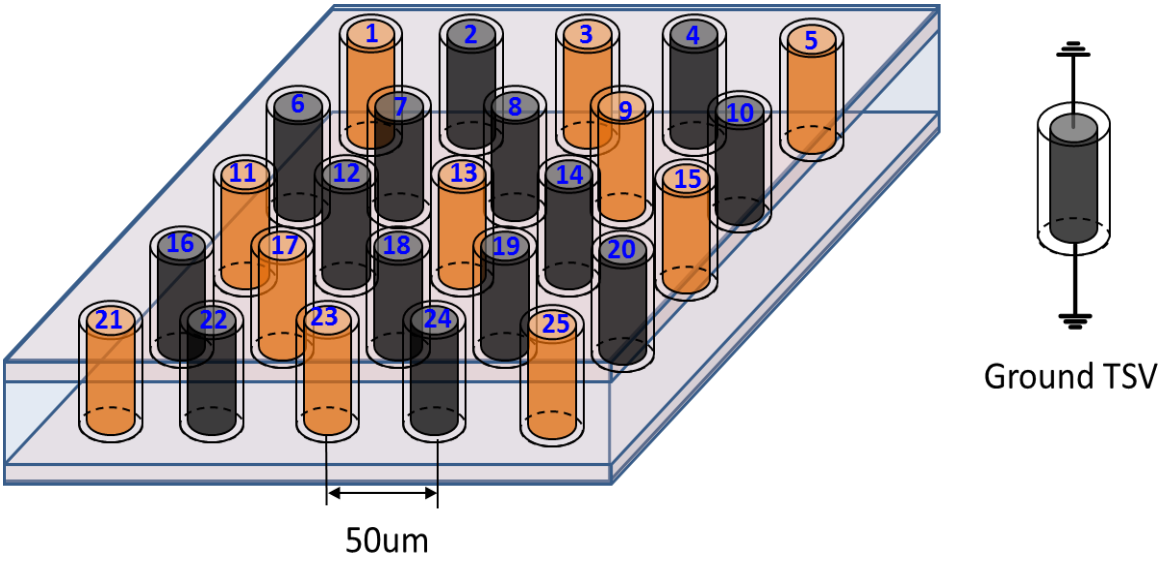


Figure 16. Positions of the ground TSVs in Case (c).

In Case (a), TSV-2, TSV-7 and TSV-25 are selected to observe the coupled waveform from aggressor TSV-1. The coupled waveform results are shown in Figure 17. As can be observed from Figure 17, with substrate conductivity of 10 S/m, the peak amplitudes of the coupled waveform at TSV-2, TSV-7 and TSV-25 are 95 mV, 35 mV and 7 mV, respectively. The coupling is more obvious at the adjacent TSVs (TSV-2 and TSV-7) of the aggressor TSV-1 due to shorter distance. Most importantly, it is observed that all these coupled waveforms have a very long tail, and the farther the TSV from the aggressor TSV-1, the longer is the tail. Hence, the time constant of the coupled waveform increases with the distance to the "aggressor TSV" which is due to the conductive and capacitive nature of silicon. The long tail of the coupled waveforms can have a detrimental effect on the signal integrity of the silicon interposer, since the effect of coupled noise is present on the coupled TSV for an extended period of time. Such an effect will never be seen in low loss dielectrics such as in organic/ceramic packages or printed circuit boards.

Case (b) is simulated to observe the coupling effects of TSVs in high resistivity substrate. As is well known, a high resistivity silicon substrate behaves like a low loss dielectric. The coupled waveforms at TSV-2, TSV-7 and TSV-25 are shown in Figure 18. As can be seen from Figure 18, the long tail of the coupled waveform disappears and the amplitude of the waveform is also smaller as compared to Case (a) when silicon conductivity was 10 S/m. The comparison of the peak amplitude of the coupled waveforms is shown in Table 1. From our preliminary simulation results, we can see that the high resistivity substrate is better for reducing the coupling between TSVs in the TSV array structure. This conclusion is validated in Section 3.4. However, a low resistivity silicon substrate is preferred from a manufacturing standpoint due to existing manufacturing infrastructure and lower cost. Hence, methods to reduce this coupling are required.

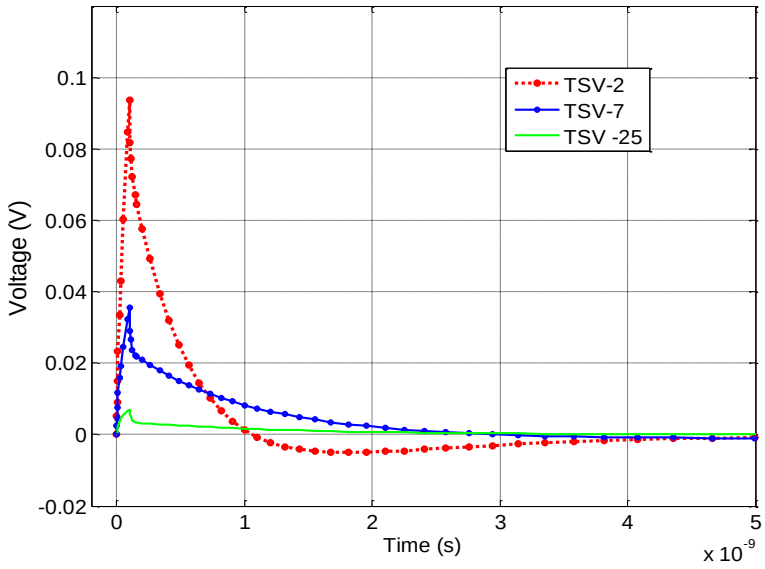


Figure 17. Coupling waveform with substrate conductivity of 10S/m

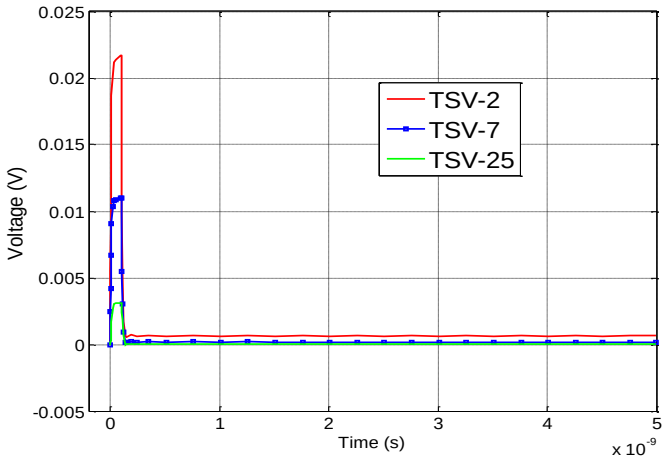


Figure 18. Coupling waveforms with substrate conductivity of 0.01 S/m.

Table 1: Comparison of peak amplitude of "victim TSVs" waveform with different silicon substrate

Silicon substrate	TSV-2	TSV-7	TSV-25
Conductivity: 10 S/m	94 mV	35 mV	7 mV
Conductivity: 0.01 S/m	22 mV	11 mV	3 mV

In Case (c), ground TSVs, as shown in Figure 16, are included and the silicon conductivity is set to be 10 S/m. It is simulated to observe the effects of ground TSVs on the coupled waveform. Figure 19 shows the comparison of the coupled waveform at TSV-13 with and without ground TSVs. It shows that when there is no ground TSV in the TSV array, the coupled waveform at TSV-13 has a spike, which can distort the signal when the signal is switching. However, with ground TSVs used, the spike disappears and the crosstalk becomes a smoother waveform, as shown in Figure 19. This is due to the ground TSVs providing shielding that can reduce the coupling between TSVs, as shown in Figure 20. However, even with shielding a long residual waveform in the time domain exist on TSV-13 which has considerable amplitude. This effect is unique to TSV arrays due to the presence of the silicon substrate, which is caused by the slow wave mode, resulting in a magnetic field that penetrates the silicon substrate through the shielding conductor. It has been concluded in the past that three modes exist for a microstrip line on Si-SiO2 double-layer system [27] as shown in Figure 21. Three modes are separated

based on the frequency, thickness of SiO2 layer and Si substrate and silicon conductivity. 1) When the product of the frequency and resistivity of the Si-substrate is large enough to produce a small dielectric loss angle, the silicon substrate act as a dielectric, which is quasi-TEM mode. 2) When the product of the frequency and substrate conductivity is large enough to yield a small depth of penetration into silicon, the silicon substrate act as a conductor wall, which is skin effect mode. 3) When the frequency is not so high and the resistivity is moderate, the slow wave mode occurs. TSVs have a similar structure to Si-SiO2 system and these three modes also exist in TSV structure [28]. A TSV pair is simulated in CST Microwave Studio [29] to investigate the three modes in TSVs. The conductivity of the silicon substrate is first set at $\sigma = 0.01S/m$ and the electric field and magnetic field distribution at 0.5 GHz in silicon substrate are obtained as shown in Figure 22. Both electric field and magnetic field penetrates the silicon substrate indicates the TSV pair in the quasi-TEM mode. The conductivity of the silicon substrate is then set at $\sigma = 5.8e7S/m$. There is almost no electric field and magnetic field in the silicon substrate as shown in Figure 23, which indicate that the TSV pair in the skin effect mode. Later, the conductivity of the silicon substrate is set at $\sigma = 10S/m$. The electric field and magnetic field at 0.5GHz in silicon substrate are obtained as shown in Figure 24. Intrinsic impedance is calculated using the simulated electric and magnetic field values. The low intrinsic impedance of $\eta = \frac{|E|}{|H|} = 58.2\Omega$ indicates the electrical field partially penetrates the silicon substrate and verifies that the slow wave mode exists in the TSV pair.

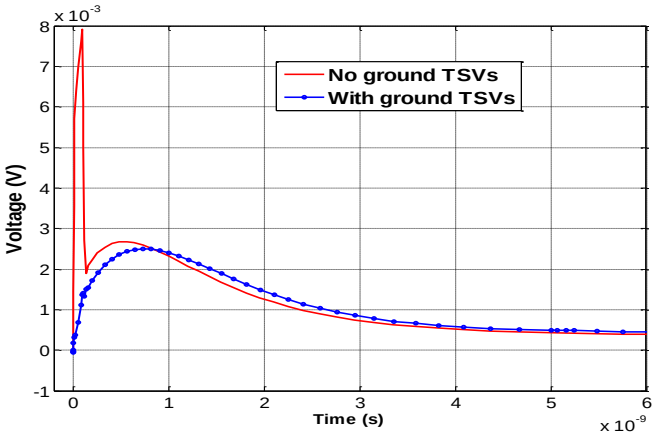


Figure 19. Coupling waveform with substrate conductivity of 10 S/m and ground TSVs.

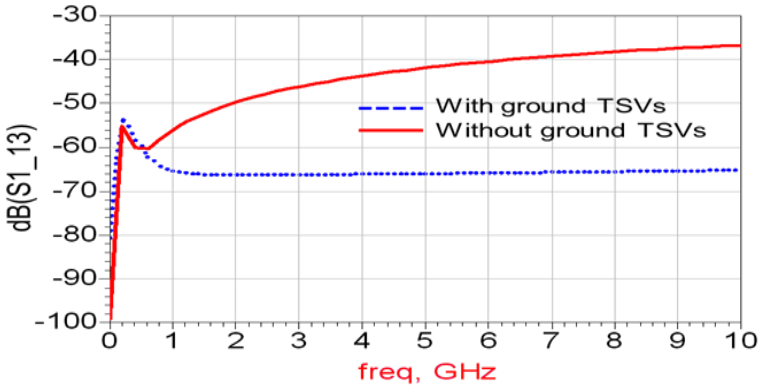


Figure 20. Coupling S-parameter between TSV-1 and TSV-13 with and without ground TSVs.

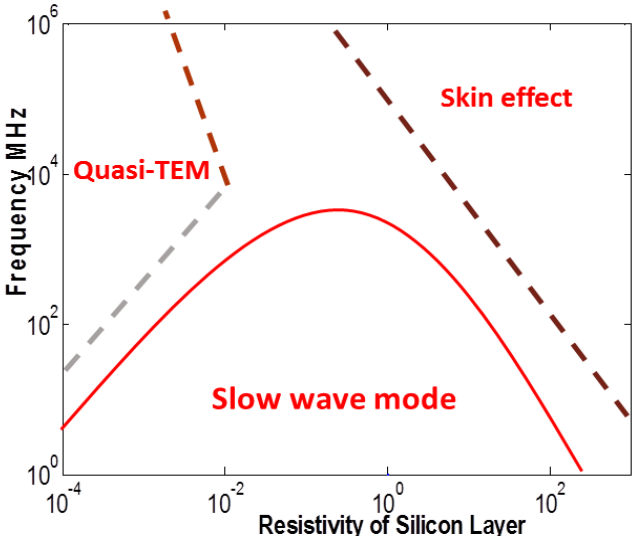


Figure 21. Three modes exist in Si-SiO2 system

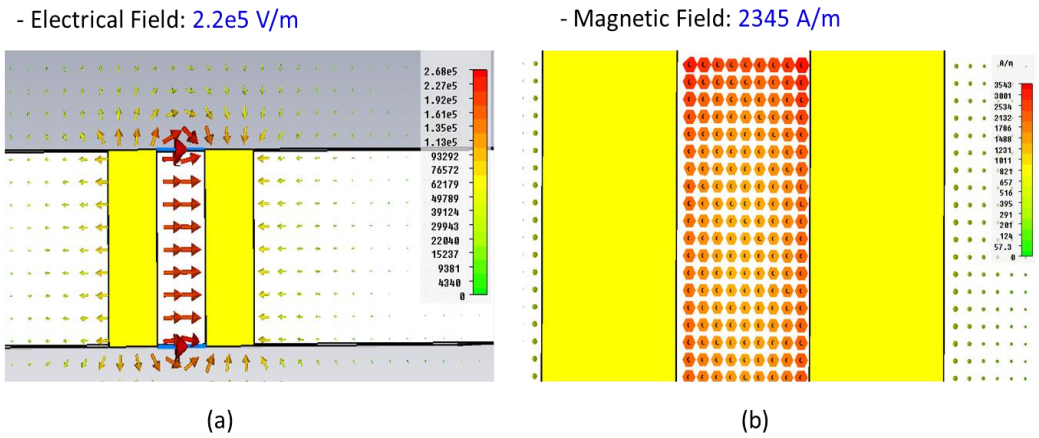


Figure 22. Quasi-TEM mode (a) Electric field distribution, (b) Magnetic field distribution.

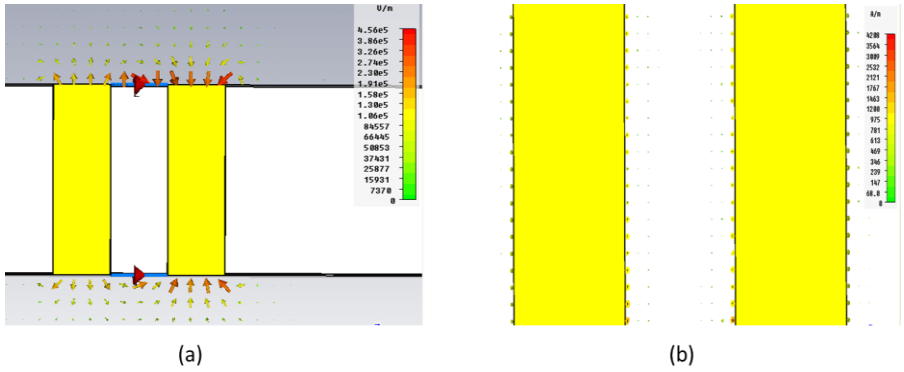


Figure 23. Skin effect mode (a) Electric field distribution (b) Magnetic field distribution.

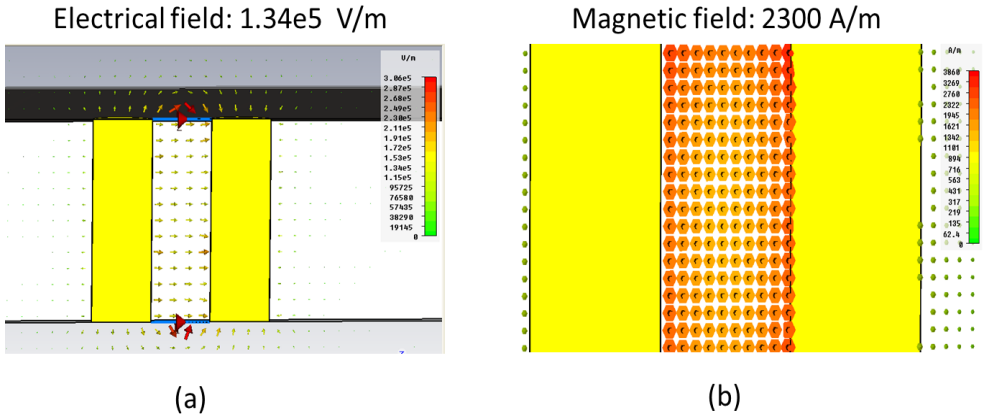


Figure 24. Slow wave mode (a) Electric field distribution, (b) Magnetic field distribution.

3.4 Eye Diagram Analysis of TSV Arrays

In this section, the eye diagram analysis of the TSV array structure is simulated. The TSV array structure used to obtain the eye diagrams is the same as in Figure 12. The same three test cases (a) (b) (c) as in Section 3.3 are used for simulation. In the eye diagram analysis, all the TSVs other than ground TSVs are defined as "signal TSVs". As shown in Figure 25, each signal TSV is connected with a 50 Ohm resistor and random bit generator. The random bit generators transmit different random bit sequences to the input of different signal TSVs. The bit rate of the random bit generator is set to be 5Gb/s.

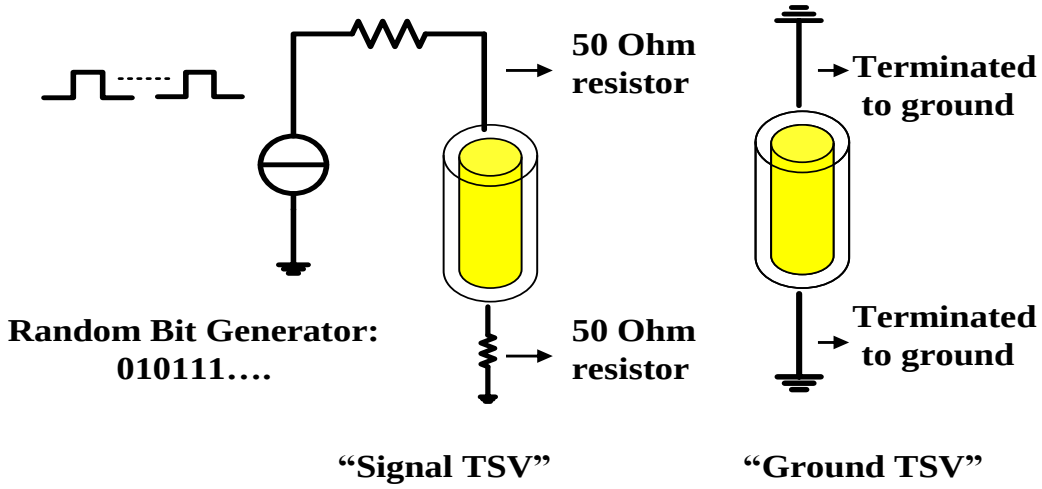


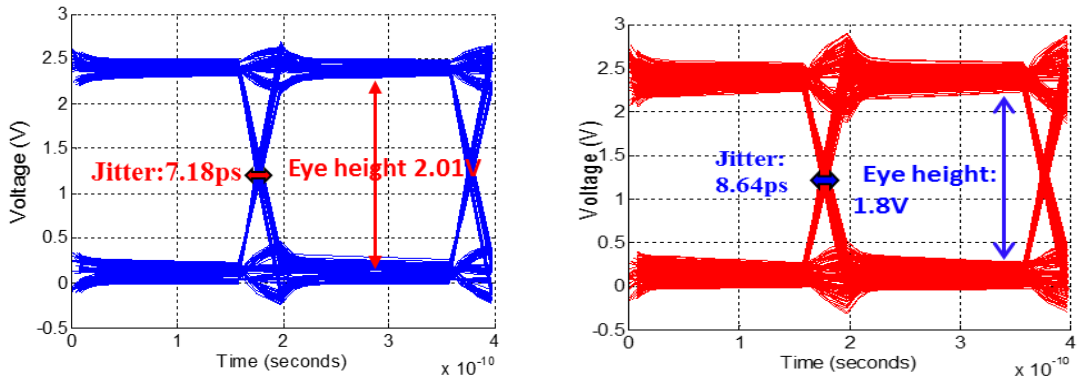
Figure 25. Configuration of "Signal TSV" and "Ground TSV" in the TSV array for eye diagram analysis.

The simulated eye diagrams of TSV-1 and TSV-13 for case (a), (b) and (c) are shown in Figure 26, Figure 27, and Figure 28, respectively. The eye height and jitter of TSV-1 and TSV-13 for three cases are also simulated and summarized in Table 2.

Table 2. Eye height and jitter in case (a), (b) and (c)

Cases		Eye height (V)	Jitter (ps)
Case (a)	TSV-1	2.01	7.18
	TSV-13	1.8	8.64
Case (b)	TSV-1	2.49	7.17
	TSV-13	2.49	7.93
Case (c)	TSV-1	2.01	3.55
	TSV-13	1.85	3.85

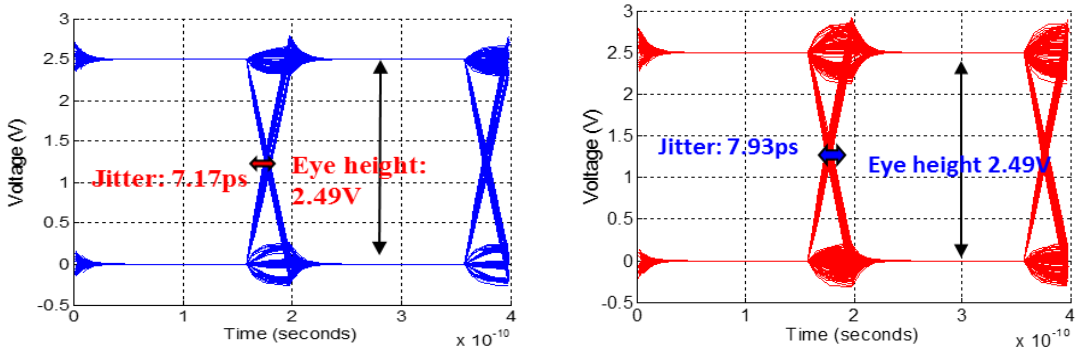
Case a: Since the low resistivity substrate is used, the increased coupling and long tail of the coupled noise (Figure 17) will deteriorate the signal transmitted, which change the rise/fall times and amplitude of the signals, similar to pulse deterioration due to inter symbol interference (ISI). Therefore the coupling and long tail of the coupled noise causes variability in the eye height and increases jitter for TSV-1 and 13, as shown in Figure 26.



(a) (b)

Figure 26. Eye diagram of (a) TSV-1 (b) TSV-13 (substrate conductivity: 10 S/m).

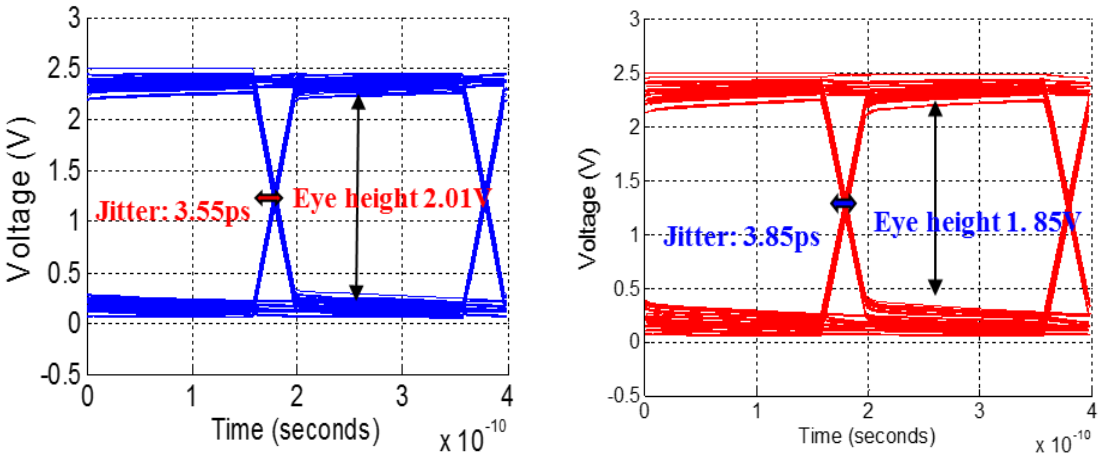
Case b: As shown in Figure 27, for high resistivity substrates, since the coupled noise has narrow width with low peak amplitude, the coupled noise has less effect on rise/fall times and amplitude of the signals transmitted. Therefore there is no variability in the eye height between TSV-1 and 13.



(a) (b)

Figure 27. Eye diagram of (a) TSV-1 (b) TSV-13 (substrate conductivity: 0.01 S/m).

Case c: The ground TSVs are used in the TSV array. The number of signal channels is reduced to 11 as a result of surrounding the signal TSVs with ground connections. There is no spike exists in the coupled waveform when multiple ground TSVs are included as shown in Figure 23, therefore the coupled waveform in case (c) has little impact on the rise/fall times of the signals. As a result, the jitter is reduced by 4ps compared to case (a) and (b) as shown in Figure 26. With shielding using ground TSVs, though the jitter can be reduced, as shown in Figure 28, there is still a long tail of the coupled waveform which will affect the amplitudes of the signals. Therefore the variability still exists in the eye height between TSV-1 and 13.



(a) (b)

Figure 28. Eye diagram of (a) TSV-1 (b) TSV-13 (substrate conductivity: 10 S/m).

As can be seen from the results comparison in Figure 26-Figure 28, without using ground TSVs, there is overshoot in the eye diagrams for case (a) and (b), which is caused by the spike in the coupled waveform.

3.5 Summary

The TSV modeling approach using global cylindrical modal basis functions is briefly described in this chapter. This modeling approach classifies the multi-scale TSV structure

into three parts: (a) Resistance and inductance extraction. (b) Substrate capacitance and conductance extraction, (c) Oxide capacitance extraction. Since only a small number of global basis functions are used, it can model large TSV arrays. The CPU time comparison using this approach and the commercial full-wave solver CST Microwave Studio [29] are compared in [16] and shown in Table 3.

Table 3. CPU time Comparison of the CST and proposed method

	CST (sec.)	Proposed method (sec.)	Number of freq. point
Three TSVs	8608	773	50
Four TSVs	10694	1227.24	50
5×5 TSV arrays	N/A	16555.77	40

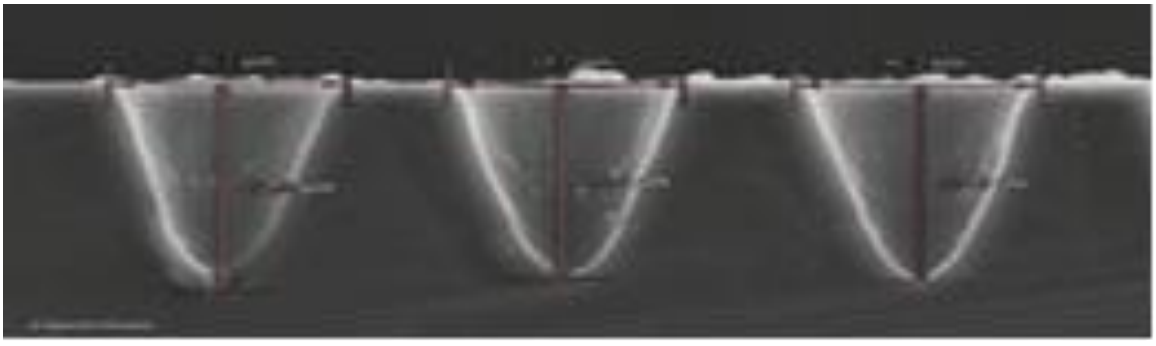
The modeling approach is later used to investigate the details on the coupling between TSVs in large TSV arrays and determine their effect on signal integrity. Coupling for low resistivity substrates induces variability in signal integrity across the silicon interposer which can be a major problem. Depending on the signal to ground ratio, the jitter can increase as well. Though this issue can be solved by using a silicon substrate with high resistivity, it is not a practical solution from a manufacturing stand-point due to the cost and infrastructure. Hence, alternate methods are required to address the variability issue to address signal integrity in silicon interposers with low resistivity.

CHAPTER 4

MODELING OF NON-UNIFORM THROUGH-SILICON VIA USING SPECIALIZED BASIS FUNCTIONS

4.1 Introduction

TSVs are treated as cylindrical structures in the modeling method described in CHAPTER 3. However, in reality, the fabricated TSVs sometimes end up with a non-uniform structure as shown in Figure 29. The tapered TSVs have different reflection noise, signal loss and parasitic effects compared to cylindrical TSVs. In this chapter, a hybrid approach for electromagnetic modeling of non-uniform through-silicon vias (TSVs) in three dimensional integrated circuits (3D ICs) is proposed. For non-uniform TSV structures, TSVs are divided vertically into conical and cylindrical sections. The modeling of the conical TSV is extended from [16] and uses conical modal basis functions to extract electrical parasitic elements of conical TSVs. By using the conical TSV modeling method combined with cylindrical TSV modeling method, complex TSV structures can be modeled efficiently [30]. The accuracy of this hybrid method is validated by comparison with 3-D full-wave simulations.



(a)

(b) (c)

Figure 29. Cross-sectional image of real TSV structure, (a) SEM cross-section view of laser drilled blind vias in silicon[31], (b) SEM cross-section of TSV after integration [32], (c) cross-section of 3D-WLP TSV [33].

4.2 Conical TSV Modeling

The structure of conical TSVs is similar to cylindrical TSVs except the conical contour. Therefore, the conical TSV modeling procedure can be divided into three parts similar as [16]: (1) Resistance and inductance extraction, which represents the loss and inductive coupling in conductors. (2) Substrate parallel conductance and capacitance extraction, which represents the loss and capacitive coupling between conductor and insulator surfaces. (3) Excess capacitance extraction, which represents the effect of the insulator between conductor and silicon substrate. The modeling flow for a conical TSV pair is shown in Figure 30.

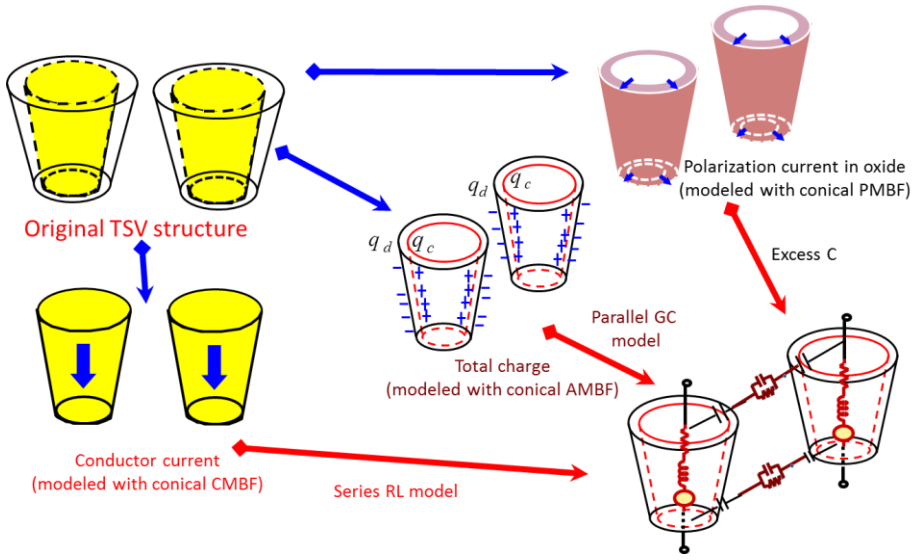


Figure 30. Modeling flow for a conical TSV pair.

4.2.1 Conical Conductor Series Resistance and Inductance Extraction

The electrical field integral equation (EFIE) [34] used to extract resistance and inductance of the conical conductor is the same as in [14], but V' in equation (11) is extended to the conical volume of the conductor.

$$\frac{\vec{J}(\vec{r},\omega)}{\sigma}+\frac{j\omega\mu}{4\pi}\int_{V'}G(\vec{r},\vec{r}')\vec{J}(\vec{r}',\omega)dV'=-\nabla\Phi(\vec{r},\omega) \tag{11}$$

After inserting the approximation of the current density in equation (12) and applying Galerkin's method, equation (13) can be obtained.

$$\vec{J}_j(\vec{r},\omega)\cong\sum_{n,q}I_{jnq}\vec{w}_{jnq}(\vec{r},\omega) \tag{12}$$

$$\sum_{n,q}I_{jnq}R_{imd,jnq}+j\omega\sum_{n,q}I_{jnq}L_{imd,jnq}=\Delta V^{j}_{imd} \tag{13}$$

where $R_{imd,jnq}=\frac{1}{\sigma}\int_{V_i}\vec{w}^{*}_{imd}(\vec{r}_i,\omega)\cdot\vec{w}_{jnq}(\vec{r}_j,\omega)$, $L_{imd,jnq}=\frac{\mu}{4\pi}\int_{V_j}\int_{V_i}\vec{w}^{*}_{imd}(\vec{r}_i,\omega)\cdot\vec{w}_{jnq}(\vec{r}_j,\omega)\frac{1}{|\vec{r}_i-\vec{r}_j|}dV_jdV_i$

$\vec{w}_{jnq}(\vec{r}_i,w)$ is the normalized jnq th order conical conduction modal basis functions (CMBF), and j,n,q represent the index of the cell, modal order and orientation of conical CMBF, respectively. V_i,V_j in equation (13) are conical volumes. Partial resistance and partial inductance can be obtained by numerically integrating in the conical volume V_i,V_j shown in Figure 31. The conical CMBFs are obtained by modifying the normalization factor of cylindrical CMBFs [14]. The normalization factor of conical CMBFs is a function of the conical cross-sectional radius, described in equation (14). The skin effect (SE) and proximity effect (PE) mode of conical CMBFs at different cross-section of the conical structure are plotted in Figure 32. As can be seen from Figure 32,

the radius of the conical CMBFs is changing according to the radius of the conical structure.

To calculate the integral in equation (13), the coordinates are defined as shown in Figure 31. Therefore, after substituting the basis function $\frac{1}{A_{in}} J_n(\alpha\rho)\cos(n\varphi_i - \varphi_d)$ [14], the original equation to calculate partial resistance and inductance can be expanded as equation 0 and equation (16), respectively.

$$A_{in} = \begin{cases} \dfrac{2\pi\rho}{\alpha} J_1(\alpha\rho) & n = 0 \\ \dfrac{2^{2-n}\alpha^n \rho^{2+n}}{(2+n)n!} F_2\left(1+\frac{n}{2};\{2+\frac{n}{2},1+n\};-\frac{1}{4}\alpha^2\rho^2\right) & n > 0 \end{cases} \tag{14}$$

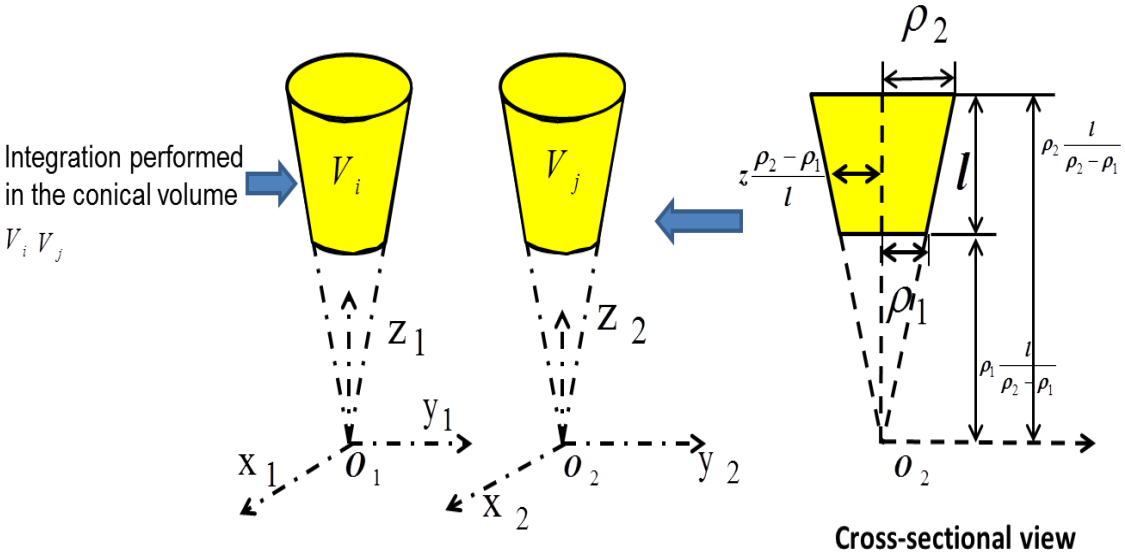


Figure 31. Definition of coordinate used to calculate numerical integral.

$$R_{imd,jnq} = \frac{1}{\sigma}\int_0^{2\pi}\cos(m\varphi_i - \varphi_d)\cos(n\varphi_j - \varphi_q)d\varphi \int_{\rho_1\frac{l}{\rho_2-\rho_1}}^{\rho_2\frac{l}{\rho_2-\rho_1}} \frac{1}{A_{in}A_{jm}^*} dz \int_0^{z\frac{\rho_2-\rho_1}{l}} \rho J_m(\alpha^*\rho) J_n(\alpha\rho) d\rho \tag{15}$$

$$L_{imd,jnq} = \frac{\mu}{8\pi} \int_{\rho_1 \frac{l}{\rho_2-\rho_1}}^{\rho_2 \frac{l}{\rho_2-\rho_1}} \int_{\rho_1 \frac{l}{\rho_2-\rho_1}}^{\rho_2 \frac{l}{\rho_2-\rho_1}} \frac{1}{A_{im}^* A_{jn}} \frac{1}{|\vec{r}_i - \vec{r}_j|} dz \int_{z\frac{\rho_2-\rho_1}{l}}^{z\frac{\rho_2-\rho_1}{l}} \int_0^l \rho J_m(\alpha^* \rho_i) J_n(\alpha \rho_j) I_\varphi d\rho_i d\rho_j \quad (16)$$

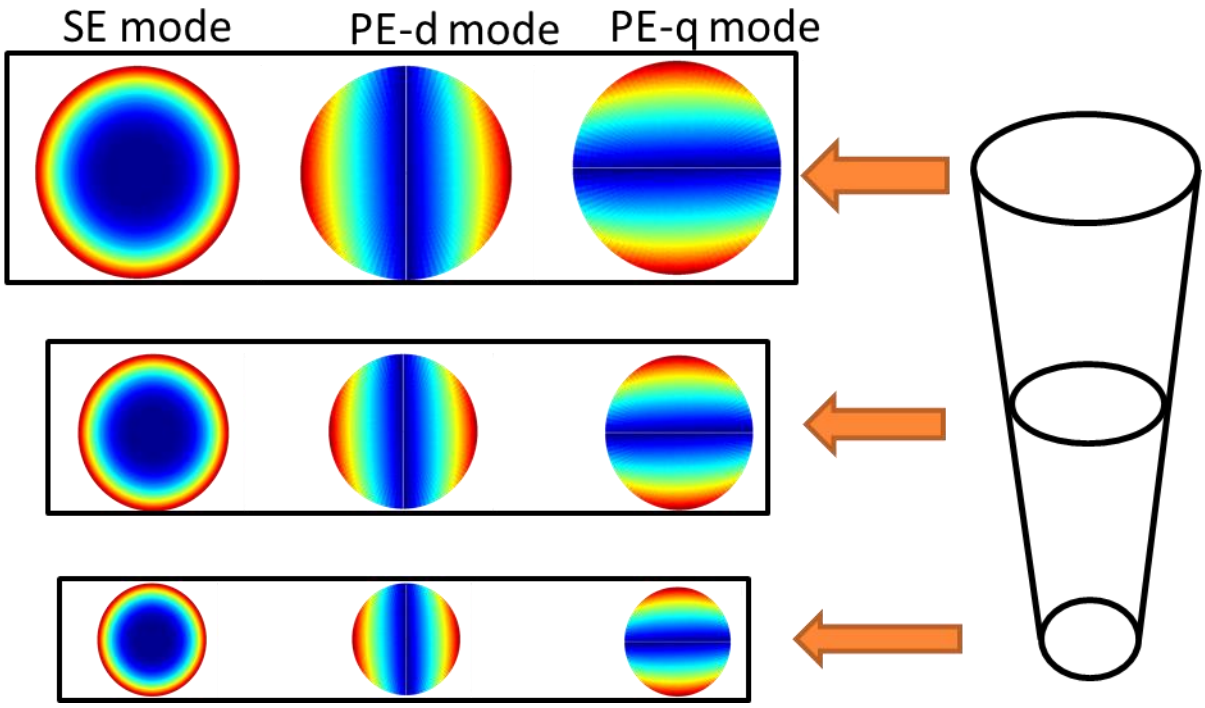


Figure 32. Conical CMBFs at different cross-section of the conical structure at 0.1 GHz.

4.2.2 Substrate Conductance and Capacitance Extraction of Conical TSVs

The Scalar Potential Integral Equation (SPIE) equation [35] combined with conical accumulation mode basis functions (AMBFs) can be used to extract substrate parallel conductance and capacitance. The conical AMBFs are obtained by modifying the normalization factor of cylindrical AMBFs [35]. The extraction procedure of conductance and capacitance is extended from [35] by changing the cylindrical TSV surfaces to conical TSV surfaces. The resultant equivalent circuit equation is expressed as:

$$\sum_{n,q} Q_{knq} P^{C,D}_{lmd,knq} = V^{k}_{lmd} \tag{17}$$

where $P^{C,D}_{lmd,knq} = \frac{1}{4\pi\varepsilon_0} \int_{S_l}\int_{S_k} v_{lmd}(\vec{r_l}) v_{knq}(\vec{r_k}) \frac{1}{|\vec{r_l} - \vec{r_k}|} dS_k dS_l$

$v_{lmd}(\vec{r_l})$ is the normalized lmd th order conical AMBF. l, m, d represent the index of the cell, order and orientation of conical AMBF, respectively. S_l, S_k are the lateral conical surfaces. Partial potential coefficients $P^{C,D}_{lmd,knq}$ can be obtained by calculating the integral over the conical surfaces S_l, S_k.

The normalization factor of a conical AMBF is obtained by equating the integration of the basis function over the lateral conical surface to unity, which is expressed as in equation (18).

$$A_{lm} = \begin{cases} \pi(\rho_1 + \rho_2)\sqrt{l^2 + (\rho_2 - \rho_1)^2} & m = 0 \\ 2(\rho_1 + \rho_2)\sqrt{l^2 + (\rho_2 - \rho_1)^2} & m > 0 \end{cases} \tag{18}$$

In order to calculate the surface integral in equation (17), we first transform the Cartesian coordinates to circular conical coordinates. Then equation (17) can be expanded as shown in equation (19), which is used to calculate the potential coefficients.

$$P_{lmd,kmq} = \frac{1}{4\pi\varepsilon_0} \int_{\rho_1 \frac{l}{\rho_2-\rho_1}}^{\rho_2 \frac{l}{\rho_2-\rho_1}} \int_{\frac{l}{\rho_2-\rho_1}}^{\frac{l}{\rho_2-\rho_1}} dz dz' \int_0^{2\pi}\int_0^{2\pi} v_{lmd}(\vec{r_l}) v_{knq}(\vec{r_k}) \frac{1}{|\vec{r_l} - \vec{r_k}|} \left\| \frac{\partial \Phi}{\partial \varphi}(\varphi, z) \times \frac{\partial \Phi}{\partial t}(\varphi, z) \right\| \cdot \left\| \frac{\partial \Phi'}{\partial \varphi}(\varphi, z) \times \frac{\partial \Phi'}{\partial \varphi}(\varphi, z) \right\| d\varphi d\varphi \tag{19}$$

where $\left\| \frac{\partial \Phi}{\partial \varphi}(\varphi, z) \times \frac{\partial \Phi}{\partial \varphi}(\varphi, z) \right\| = z\left(\frac{\rho_2 - \rho_1}{l}\right)\sqrt{1 + \left(\frac{\rho_2 - \rho_1}{l}\right)^2}$ $\left\| \frac{\partial \Phi'}{\partial \varphi}(\varphi, z) \times \frac{\partial \Phi'}{\partial \varphi}(\varphi, z) \right\| = z\left(\frac{\rho_2' - \rho_1'}{l}\right)\sqrt{1 + \left(\frac{\rho_2' - \rho_1'}{l}\right)^2}$

4.2.3 Oxide Liner Excess Capacitance Extraction of Conical TSV

To calculate the oxide liner excess capacitance, the EFIE equation combined with conical polarization mode basis functions (PMBFs) can be used. The conical PMBFs are obtained by modifying the normalization factor of the cylindrical PMBFs [16] which are

deduced from solving the Laplace's equation in the insulator region. The oxide capacitance extraction procedure is extended from [16] by changing the integral volume to a conical annulus. The resultant oxide capacitance calculation formula is given as the following equation (20):

$$C^{ex}_{kmd,\ln q} = \frac{\varepsilon_0(\varepsilon_{ox} - \varepsilon_{si})}{\int_{V_k} \vec{u}_{kmd} \cdot \vec{u}_{lnq} dV_k} \tag{20}$$

where $\vec{u}_{kmd}$ is the conical PMBF. k, m, d represent the index of the cell, order and orientation of conical PMBF, respectively. V_k in equation (20) is the conical oxide region as shown in Figure 33.

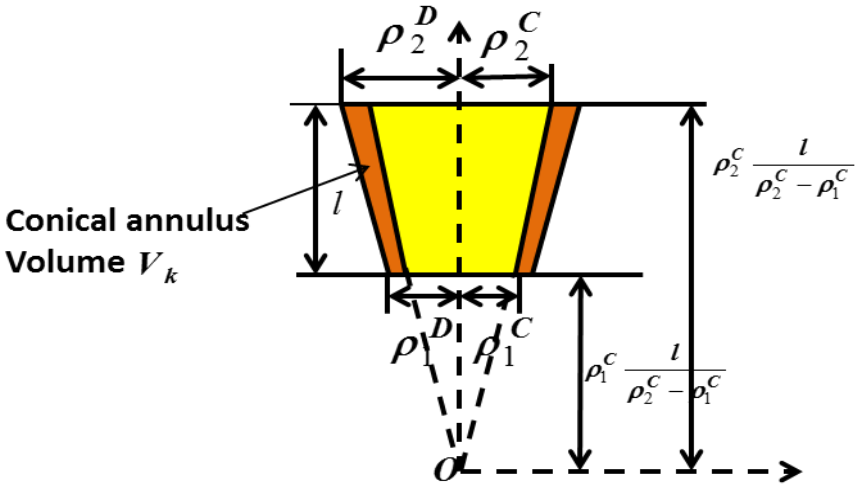


Figure 33. Parameters used to calculate oxide capacitance.

The normalization factor of the conical PMBFs is obtained by equating the integration of the basis function over the lateral surface to unity. Given the parameters of conical TSVs defined as shown in Figure 33, the normalization factor of conical PMBFs can be expressed as equation (21). Given the coordinate system defined as in Figure 32, the oxide capacitance calculation formula (20) can be expressed as equation (22).

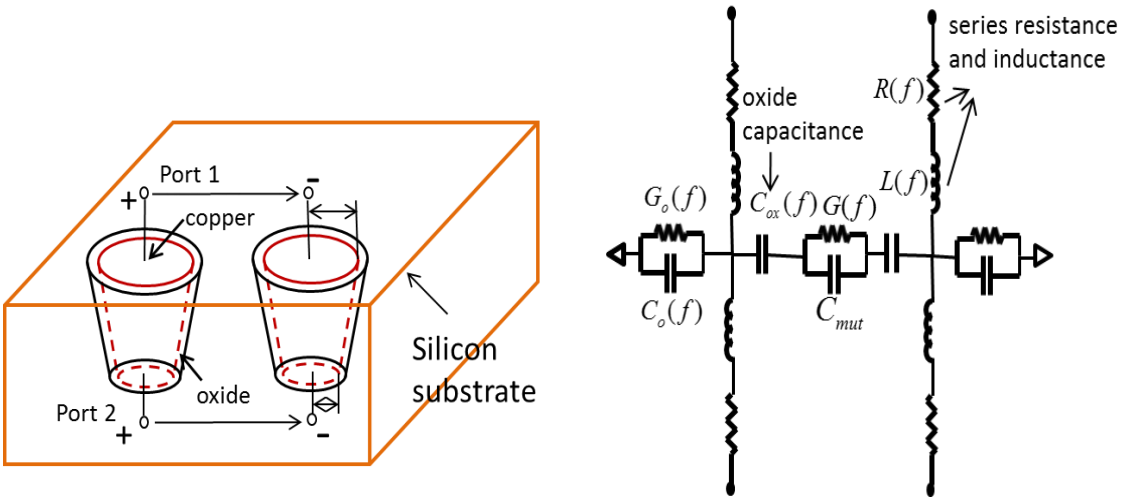
$$A_{km}=\begin{cases}2\pi\sqrt{l^2+(\rho_2^D-\rho_1^D)} & m=0\\ 4\sqrt{l^2+(\rho_2^D-\rho_1^D)}\{\dfrac{(\rho_2^D-\rho_1^D)^m}{(\rho_2^C-\rho_1^C)^m}+\dfrac{(\rho_2^D-\rho_1^D)^{-m}}{(\rho_2^C-\rho_1^C)^{-m}}\} & m>0\end{cases} \tag{21}$$

$$C_{kmd,\ln q}^{ex}=\frac{\varepsilon_0(\varepsilon_{ox}-\varepsilon_{si})}{\int_{\rho_1^C\frac{l}{\rho_2^C-\rho_1^C}}^{\rho_2^C\frac{l}{\rho_2^C-\rho_1^C}}dz\int_{z\frac{\rho_2^C-\rho_1^C}{l}}^{z\frac{\rho_2^C-\rho_1^C}{l}+\rho_2^D-\rho_2^C}\vec{u}_{kmd}\cdot\vec{u}_{lnq}d\rho\int_0^{2\pi}d\varphi} \tag{22}$$

4.3 Simulation Results of Conical TSVs

The proposed modeling method is applied to model two conical TSV interconnections. The ports setup of the conical TSV pair is shown in Figure 34(a). The length, pitch, oxide thickness, top radius, and bottom radius are 200um, 50um, 0.1um, 10um, and 5um, respectively. The conductivity of the silicon substrate is set as 10 S/m. The dielectric constants of silicon dioxide and silicon are set to be 3.9 and 11.9, respectively. For comparison, two cases of cylindrical TSV pairs are simulated using the modeling method [16]. The radii of the cylindrical TSVs in these two cases are fixed at 10um and 5um, respectively. All other parameters are the same as the conical TSV pair.

The equivalent circuit of the two conical TSVs is shown in Figure 34(b). This equivalent circuit is obtained by combining the conductor $R-L$ elements, insulator excess capacitance and potential coefficient elements into a single matrix equation. The frequency-dependent values of $RLCG$ parameters of the conical TSVs obtained using the proposed method are shown in Figure 35 and Figure 36. The capacitance plotted in Figure 36(a) is the equivalent capacitance C_0+2C, where C_0 is the self-capacitance and C is the sum of oxide capacitance and mutual capacitance ($C=C_{ox}+C_{mut}$). As can be seen from Figure 35 and Figure 36, the $RLCG$ values of conical TSVs show a similar frequency-dependent trend as cylindrical TSVs, and the $RLCG$ values of conical TSVs are between the two cylindrical TSV pairs.



(a) (b)

Figure 34. (a) Geometry, ports setup of two conical TSVs (b) Equivalent circuit of two conical TSVs.

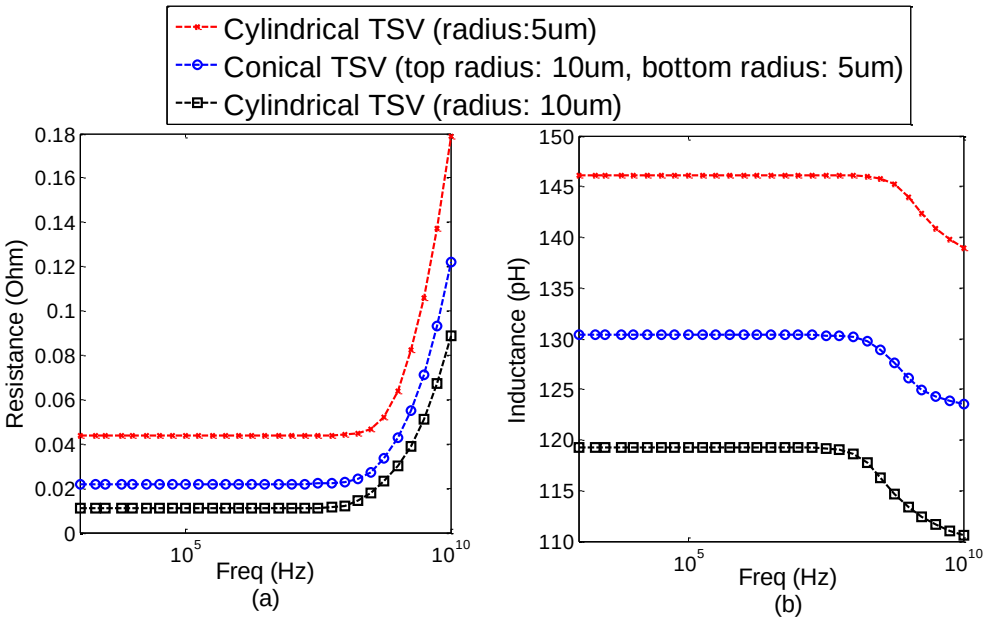


Figure 35. Equivalent parasitic elements of conical TSVs with 10um top radius and 5um bottom radius, cylindrical TSVs with 5um radius, cylindrical TSVs with 10um radius, (a) Series resistance of the conductor, (b) Self-inductance of the conductor.

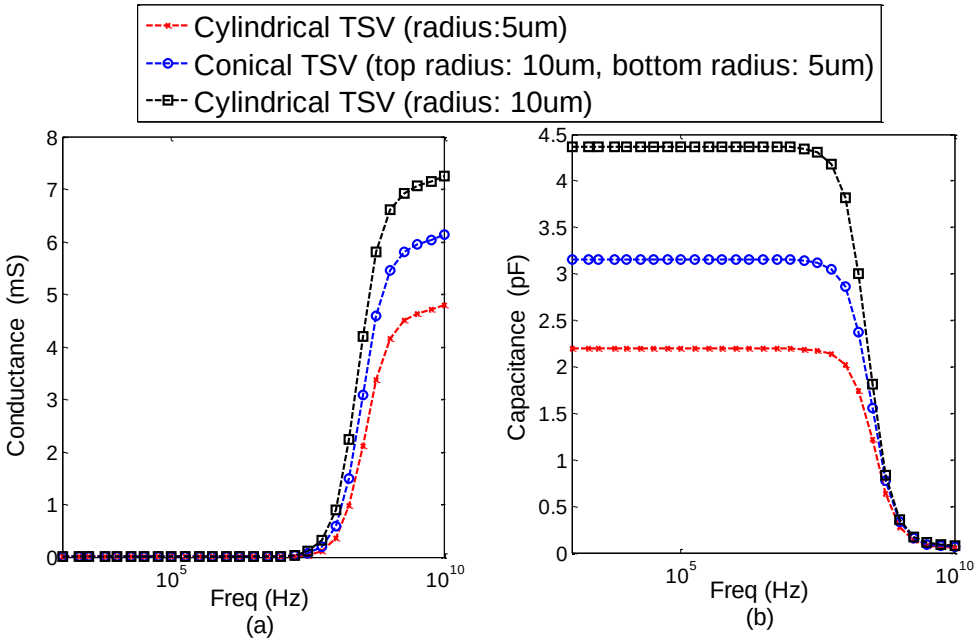


Figure 36. Equivalent parasitic elements of conical TSVs with 10um top radius and 5um bottom radius, cylindrical TSVs with 5um radius, cylindrical TSVs with 10um radius, (a) Equivalence conductance $G_0 + 2G$, (b) Equivalence capacitance $C_0 + 2C$.

The insertion losses of the conical TSVs using the proposed modeling approach and CST Microwave Studio [29] are shown in Figure 37. As can be seen from Figure 37, the insertion loss obtained using the proposed method shows good correlation with simulation result from CST up 10 GHz.

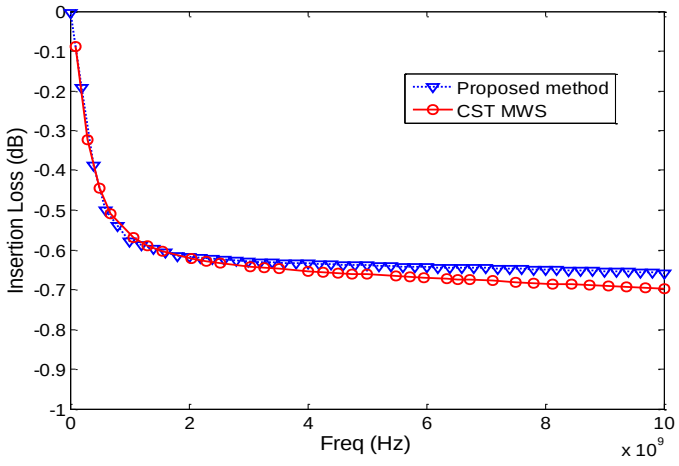


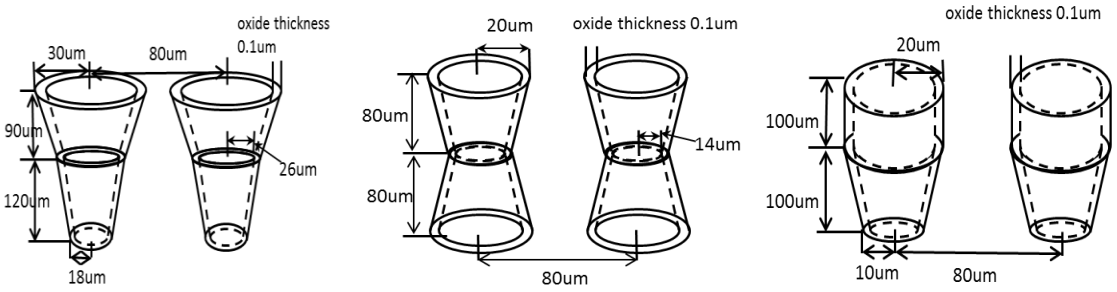
Figure 37. Insertion loss for two conical TSVs.

4.4 Modeling of Complex TSV Structures

In this section, a hybrid modeling method is proposed to model complex TSV structures. This modeling method can be divided into two steps. In the first step, the tapered TSVs are segmented into conical or cylindrical segments. Each segment can be modeled using the cylindrical TSV modeling method or the conical TSV modeling method based on the shape of the segment. In the second step, under the assumption that the maximum size of the problem space is much smaller than the wavelength of the maximum modeling frequency, the S-parameters of the segments are cascaded to obtain the insertion loss of the tapered TSV pair.

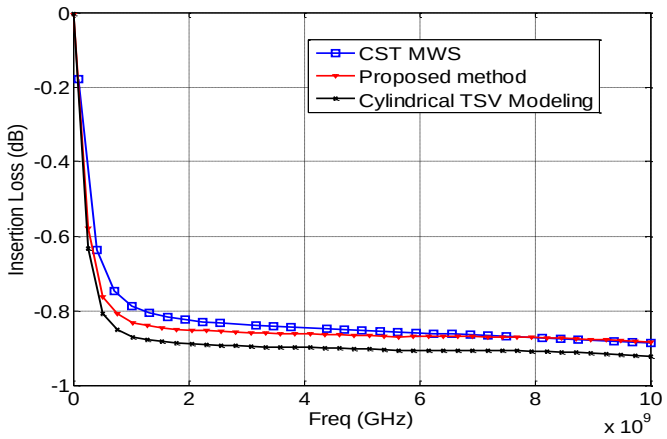
The proposed hybrid modeling method is applied to model three different complex tapered TSV pairs. The geometry of the three cases such as the length, oxide thickness, pitch, and radius is defined as in Figure 38. The conductivity of the silicon substrate is set at 10 S/m. The dielectric constants of silicon dioxide and silicon are set to be 3.9 and 11.9, respectively. To simulate the complex TSV structure, the proposed method consumes only about 30MB memory, which is 33× less than CST [29] which consumes about 1GB memory. The insertion losses of the three tapered TSV pairs using the hybrid modeling method and CST [29] are compared in Figure 39. For comparison, the three cases are also modeled using only one cylindrical segment, with the radius of the cylindrical segment set at 20um, 14um and 30um, respectively. As can be seen from Figure 39, the insertion losses obtained using the hybrid method and CST [29] show good correlation over a bandwidth of 10GHz. However, the insertion losses show larger deviation for the three cases using only cylindrical TSV modeling method. Although the difference of the insertion loss obtained using the proposed method and cylindrical TSV modeling is about 0.1dB-0.2dB, it is 10%-20% of the overall insertion loss. The 10%-20% difference of insertion loss is an important factor to consider when designing TSV

interconnections for 3-D systems, which indicates that cylindrical TSV modeling method can not accurately model non-uniform TSVs.

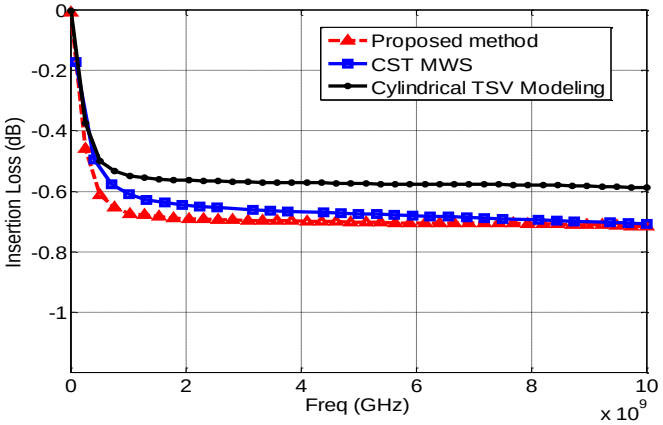


(a) (b) (c)

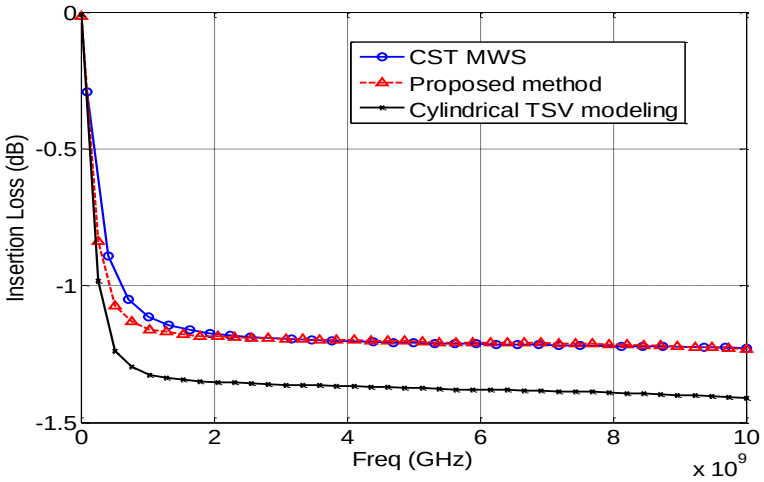
Figure 38. Complex TSV structures.



(a)



(b)



(c)

Figure 39. Insertion loss for three different complex TSV structures.

4.5 Summary

In this chapter, a conical TSV modeling approach is presented first. This approach is extended from the cylindrical TSV modeling approach described in CHAPTER 3 and uses conical modal basis functions to extract *RLCG* parasitic effects. It has been found that the conical TSVs have different parasitic effects compared to cylindrical TSVs, which indicates the importance of modeling non-uniform TSVs. Later, a hybrid modeling method for non-uniform TSV structures is presented. This method combines conical TSV and cylindrical TSV modeling method and can model non-uniform TSV structures with different profiles. The proposed method shows good correlation with full-wave simulations for non-uniform TSV pairs.

CHAPTER 5

MODELING AND ANALYSIS OF SILICON AND GLASS INTERPOSERS USING M-FDM AND MODAL DECOMPOSITION

5.1 Introduction

With increasing clock speed and an increase in the number of I/O pins in 3D systems, supplying clean power is becoming a major challenge. The large number of I/Os also leads to frequent signal via transitions between power and ground planes. This results in combined signal and power integrity issues. The PDN becomes more complicated when TSVs, which are the essential interconnections in 3D ICs, are included as shown in Figure 40. Therefore, modeling and analysis of the PDN including TSVs in 3D systems becomes necessary. Since TSVs are small and represent a multi-scale structure (due to insulator liner thickness and aspect ratio), a large mesh density is required by commercial full-wave EM solvers to co-simulate PDN with TSVs. Therefore, analysis consumes a large amount of memory and quickly leads to large computational time.

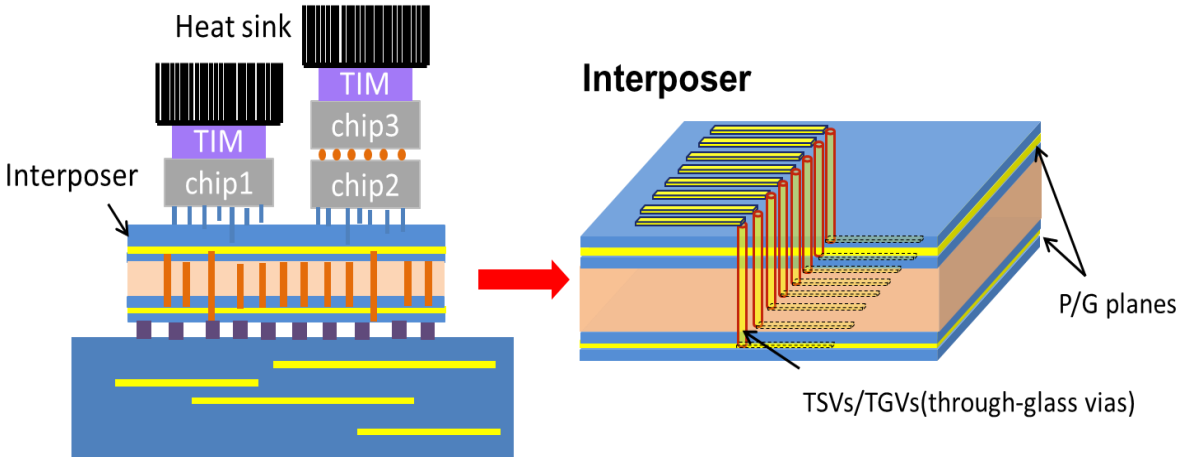


Figure 40. Power/ground planes in silicon interposer with TSVs.

In this chapter, an efficient hybrid modeling approach for power delivery networks (PDNs) with through-silicon vias (TSVs) for 3D systems is proposed [36]. The proposed

approach extends the multi-layer finite difference method (M-FDM) [37] to include TSVs by extracting their parasitic behavior using an integral equation based solver [16]. The proposed modeling technique is applied to model lossy silicon interposers and low loss glass interposers, which are two major types of interposers to achieve 3-D integration. Silicon interposers can achieve fine wiring and high I/O density [38], but it faces several challenges, such as high cost due to limited wafer size (200-300mm) from which to yield large number of interposers and signal losses in silicon interposer are usually large because of the lossy silicon [39]. Glass interposers have excellent surface flatness, high electrical resistivity and large panel liquid crystal display (LCD) glass substrate are widely used, therefore glass interposers can be manufactured at low cost [39, 40]. Using the proposed modeling technique, the power/signal integrity of silicon interposers and glass interposers are investigated and compared. The comparison indicates the benefits of using silicon interposers for high speed signaling.

5.2 Modeling of PDN Containing TSVs/Through-Glass-Vias

An accurate and computationally fast modeling approach for PDN with multiple TSVs is needed to support efficient analysis of signal/power integrity for 3D systems. This section describes a hybrid modeling approach that combines M-FDM, which can be used to model multiple P/G planes, and an integral equation based solver for TSVs. The details of this modeling approach are discussed in the following sections.

5.2.1 Modeling of Planes in Silicon Interposers

The Helmholtz equation is the underlying elliptic differential equation for modeling of P/G planes [41] given by:

$$(\nabla_T^2 + k^2)u = -jw\mu dJ_Z \tag{23}$$

where ∇_T^2 is the transverse Laplace operator parallel to the planar structure, k is the wavenumber, u is the voltage, w is the angular frequency, μ is the permeability, d is the distance between the planes and J_Z is the current density injected normal to the planes. The problem definition is completed by assuming a magnetic wall or an open boundary at the plane periphery. The Helmholtz equation is solved using the finite difference scheme. The 2-dimensional Laplace operator can be approximated as

$$\nabla_T^2 u = \frac{u_{i,j+1} + u_{i+1,j} + u_{i,j-1} + u_{i-1,j} - 4u_{i,j}}{h^2} \tag{24}$$

where h is the mesh length and $u_{i,j}$ is the voltage node (i,j) for the cell-centered discretization shown in Figure 41.

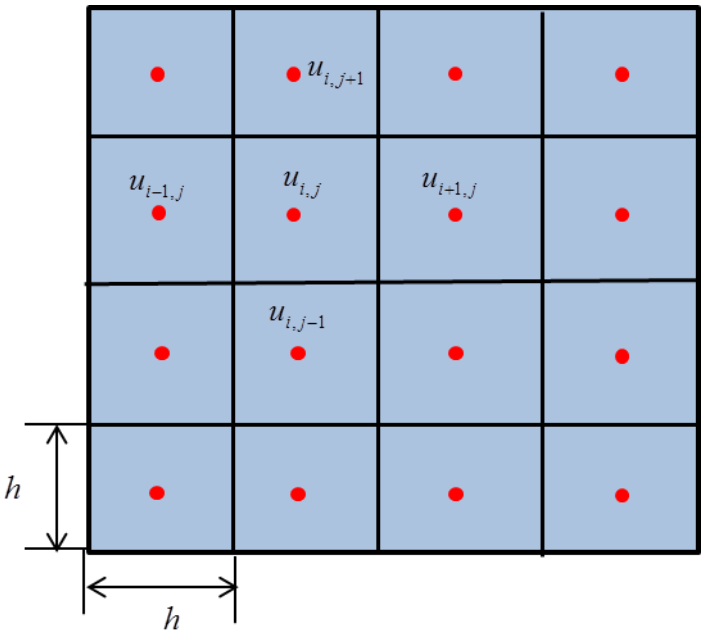


Figure 41. Discretization of the Laplace operator.

This discretization results in a bedspring unit cell model for plane pairs as shown in Figure 42. This plane pair consists of inductors between neighboring node and capacitors from each node to ground. The $RLCG$ parameters can be expressed in equation (25)-(28)

$$C = \varepsilon \frac{h^2}{d} \tag{25}$$

$$L = ud \tag{26}$$

$$R = \frac{2}{\sigma t} + 2\sqrt{\frac{j\omega u}{\sigma}} \tag{27}$$

$$G = \omega C \tan\delta \tag{28}$$

where ε is the permittivity, μ is the permeability, σ is the conductivity, and $\tan\delta$ is the loss tangent.

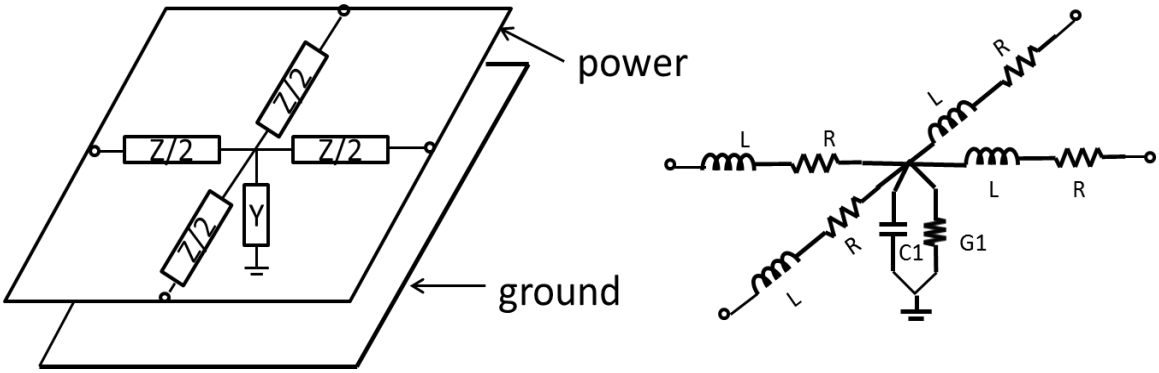


Figure 42. Unit Cell model for power/ground planes

This method is extended to model the inhomogeneous dielectric materials between power and ground planes by modifying the unit cell model [42]. The total admittance of the unit cell can be obtained by superposition of series admittance of all the dielectric layers. In the case of a double sided silicon interposer, the unit cell is found as shown in Figure 43. As shown in Figure 43, G_1 and G_{si} are the polymer and silicon conductance, G'_{si} is an additional term that accounts for the losses due to the finite conductivity of silicon and can be expressed in equation (29), and R_s represents the losses due to longitudinal current in conductive silicon and can be expressed in equation (30).

$$G'_{Si} = \frac{C_{Si}\sigma_{Si}}{\varepsilon_{Si}} \tag{29}$$

$$R_s = 2\sqrt{\frac{j\omega\mu}{\sigma_{Si}}} \tag{30}$$

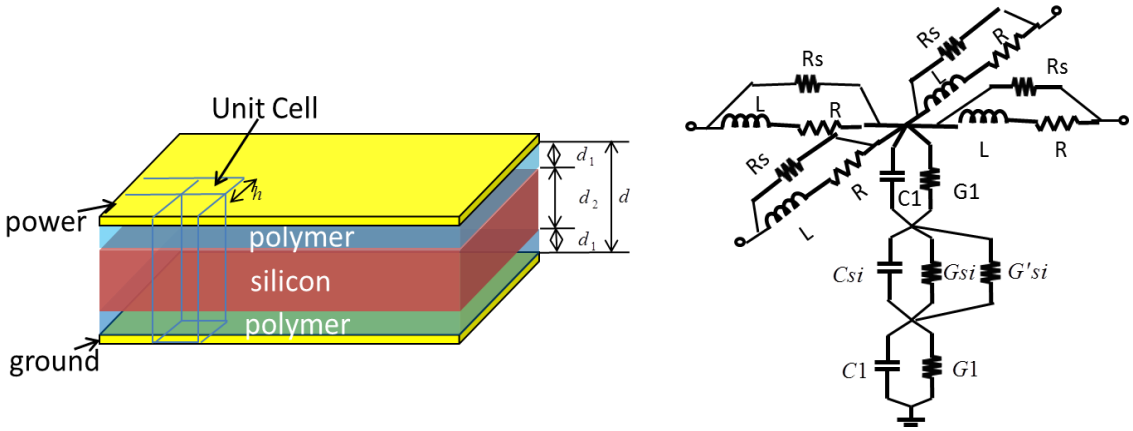


Figure 43. Geometry of P/G planes with unit cell and unit cell model for a double sided silicon interposer with P/G planes.

The transmission lines can be integrated into P/G planes using modal decomposition [43]. For a three conductor system consisting of two parallel plates (power/ground) and a signal conductor, there are two possible (quasi) TEM modes. One is the parallel-plate mode. The other is the mode that wave propagating along the signal line and there is no voltage difference between planes. The modal decomposition technique used to incorporate transmission-line models into power/ground plane models are described in Figure 44. Z^c_{par} and Z^c_{sig} represent the characteristic impedance of the parallel-plate and signal line modes. The subscripts p and s represent the line parameters of the top plane and the signal line, respectively. The subscripts par and sig represent the modal parameter of the top plane and the signal line. k is the coupling coefficient and defined as $\frac{L_{sp}}{L_{pp}}$, where L_{pp} and L_{sp} represent the pul self-inductance of the upper plane and the pul mutual inductance between the upper plane and the signal conductor. It can also be

expressed in terms of an admittance matrix as in equation (31), where Y_p and Y_s are the Y matrices of P/G planes and transmission lines (considering ideal reference) [44].

$$\begin{bmatrix} \boldsymbol{I}_p^i \\ \boldsymbol{I}_p^o \\ \boldsymbol{I}_m^i \\ \boldsymbol{I}_m^o \end{bmatrix} = \begin{bmatrix} k^2\boldsymbol{Y}_s + \boldsymbol{Y}_p & k\boldsymbol{Y}_s \\ k\boldsymbol{Y}_s & \boldsymbol{Y}_s \end{bmatrix} \begin{bmatrix} \boldsymbol{V}_p^i \\ \boldsymbol{V}_p^o \\ \boldsymbol{V}_m^i \\ \boldsymbol{V}_m^o \end{bmatrix} \tag{31}$$

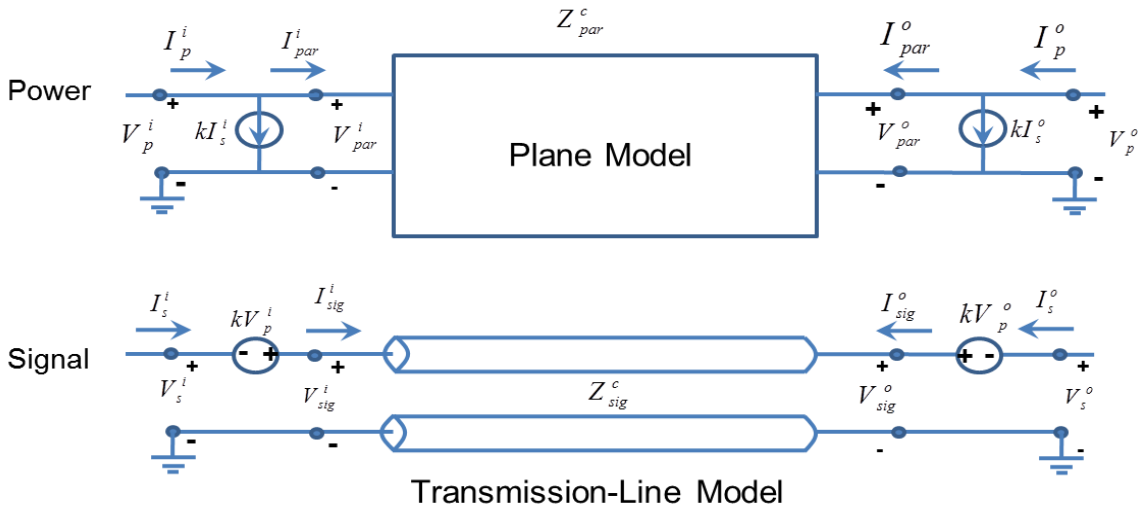


Figure 44. Incorporating transmission line model into plane mode using modal decomposition.

5.2.2 Integration of TSVs/TGVs and P/G planes

The responses of TSVs and power and ground planes need to be combined together to perform accurate system level analysis. This integration can be performed using the admittance matrix of the two modules along with the stamp rule. This process involves conversion of the TSV response into its equivalent model which is then stamped into the system admittance matrix. The coupling between TSVs and the power/ground planes are not considered in this integration process, since the coupling between transmission lines and the coupling between TSVs dominate.

For example in a two bit microstrip-via-microstrip transition structure as shown in Figure 46, the system response matrix of the planes and microstrip lines can be obtained by using M-FDM. This integration of TSVs and plane responses is based on the element stamping of modified nodal analysis (MNA) [45]. Figure 45 shows the element stamping procedure for stamping one element with Y-parameters in the modified nodal analysis, where m and n are the node numbers in the original system matrix before the element are stamped. Similarly, the TSV pair with Y-parameters can be stamped into the system matrix of power and ground planes as given by equation (32).

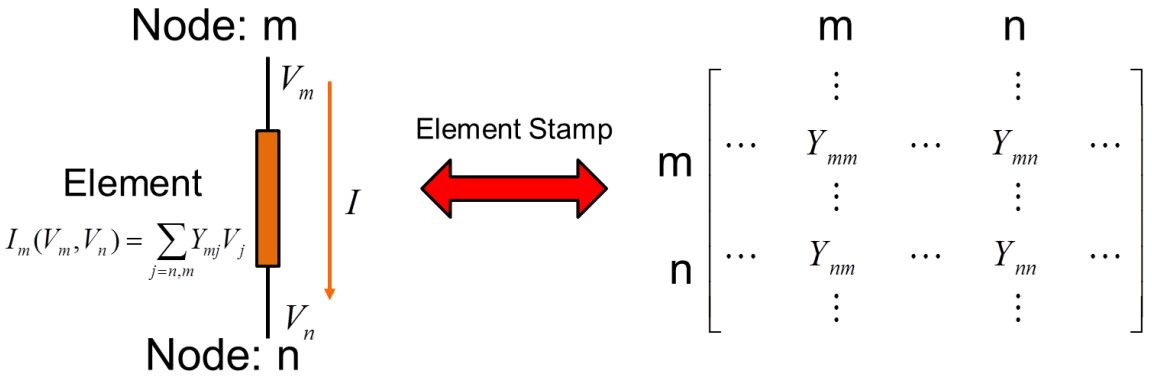


Figure 45. Element stamping of modified nodal analysis [45].

$$\begin{bmatrix} \vdots \\ I_1 \\ \vdots \\ I_2 \\ \vdots \\ I_3 \\ \vdots \\ I_4 \\ \vdots \end{bmatrix} = \begin{bmatrix} \vdots & \vdots & \vdots & \vdots \\ Y_{1,1}^{PDN}+Y_{1,1}^{TSV} & Y_{1,2}^{PDN}+Y_{1,2}^{TSV} & Y_{1,3}^{PDN}+Y_{1,3}^{TSV} & Y_{1,4}^{PDN}+Y_{1,4}^{TSV} \\ \vdots & \vdots & \vdots & \vdots \\ Y_{2,1}^{PDN}+Y_{2,1}^{TSV} & Y_{2,2}^{PDN}+Y_{2,2}^{TSV} & Y_{2,3}^{PDN}+Y_{2,3}^{TSV} & Y_{2,4}^{PDN}+Y_{2,4}^{TSV} \\ \vdots & \vdots & \vdots & \vdots \\ Y_{3,1}^{PDN}+Y_{3,1}^{TSV} & Y_{2,2}^{PDN}+Y_{3,2}^{TSV} & Y_{3,3}^{PDN}+Y_{3,3}^{TSV} & Y_{4,4}^{PDN}+Y_{3,4}^{TSV} \\ \vdots & \vdots & \vdots & \vdots \\ Y_{4,1}^{PDN}+Y_{4,1}^{TSV} & Y_{4,2}^{PDN}+Y_{4,2}^{TSV} & Y_{4,3}^{PDN}+Y_{4,3}^{TSV} & Y_{4,4}^{PDN}+Y_{4,4}^{TSV} \\ \vdots & \vdots & \vdots & \vdots \end{bmatrix} \begin{bmatrix} \vdots \\ V_1 \\ \vdots \\ V_2 \\ \vdots \\ V_3 \\ \vdots \\ V_4 \\ \vdots \end{bmatrix} \quad (32)$$

where $Y_{i,j}^{PDN}$ is the element in the Y matrix of power and ground planes including microstrip lines and $Y_{i,j}^{TSV}$ is the element in the Y matrix for the TSV response. A similar procedure can be applied to glass vias as well.

The proposed hybrid modeling approach is applied here to model a two bit microstrip-TSV transition structure as shown in Figure 46 with dimensions described. Two 20um thick polymer (with $\varepsilon_r = 2.51$ and $\tan\delta = 0.004$) layers are on both sides of the silicon (with 10 S/m conductivity and $\varepsilon_r = 11.9$) interposer. The length, pitch, radius, insulator liner thickness of the two TSVs are 200um, 100um, 20um, and 0.1um respectively. The length, width, thickness, spacing of the microstrip lines are 10mm, 40um, 10um and 80um, respectively. The insertion loss, far end and near end coupling obtained using the proposed method and CST Microwave Studio are shown in Figure 47. As can be seen from Figure 47, the S-parameters obtained using the proposed method show good correlation with simulation results from CST. To simulate this structure the proposed method takes ~10mins compared to CST which takes > 10 hours on a 2.4 GHz dual core computer.

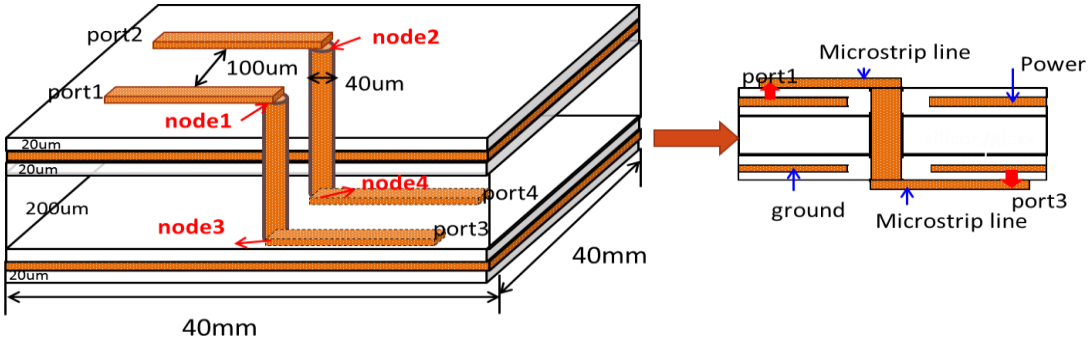
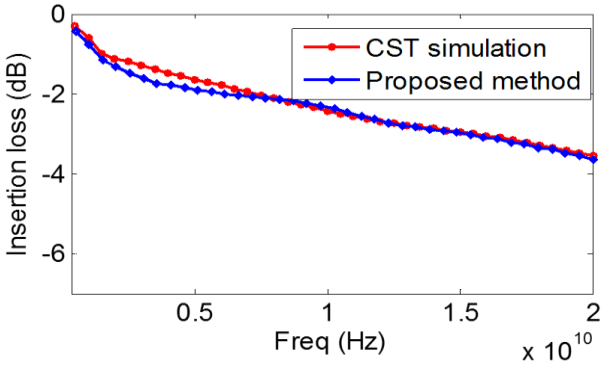
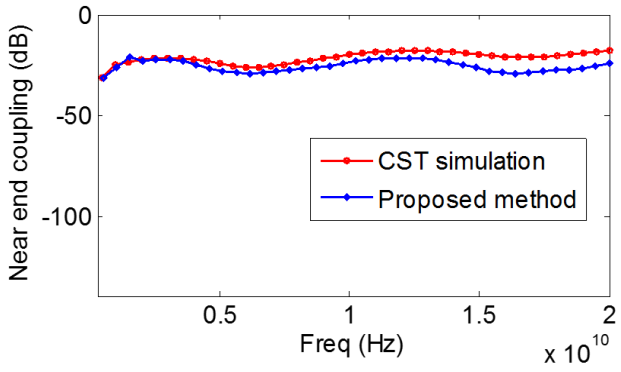


Figure 46. Two bit microstrip-via-microstrip transition structure.



(a)



(b)

Figure 47. S-parameters of the two bit microstrip-TSV transition structure, (a) insertion loss, (b) near end coupling.

5.3 Via Coupling Effects

5.3.1 TSVs and TGVs Coupling Effects

The proposed hybrid modeling method is used in the power/signal integrity analysis of a PDN with TSVs/TGVs. The coupling effects of only TSVs/TGVs in a silicon/glass interposer without P/G planes are first examined with 8×1 TSVs/TGVs array model. The geometry of the 8×1TSVs/TGVs array model and 16 ports definition are shown in Figure 48. The response of an 8×1 TSVs array model is obtained using the TSV modeling method mentioned in section II. The response of an 8×1TGV array model in a glass interposer is obtained using the method described in [14]. The near end and far end coupling between TSV-1/TGV-1 and TSV-2/TGV-2 in the TSV and TGV array are compared in Figure 49. As can be seen from Figure 49(a) (b), the coupling in a TSV array is larger than a TGV array, which is because the high conductivity silicon substrate introduces loss and coupling through the substrate. The insertion losses of TSVs/TGVs are also compared in Figure 49(c), where the sharp slope of the insertion loss of TSVs is caused by the small insulator liner thickness resulting in a larger capacitance [16].

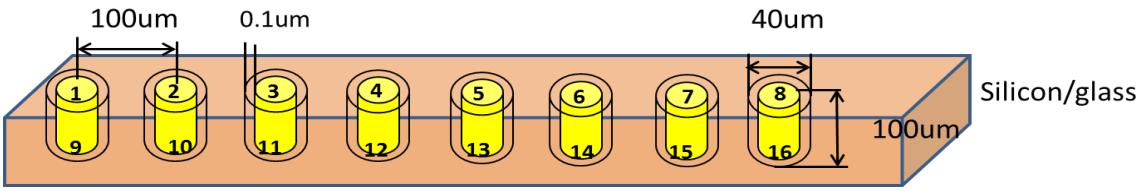
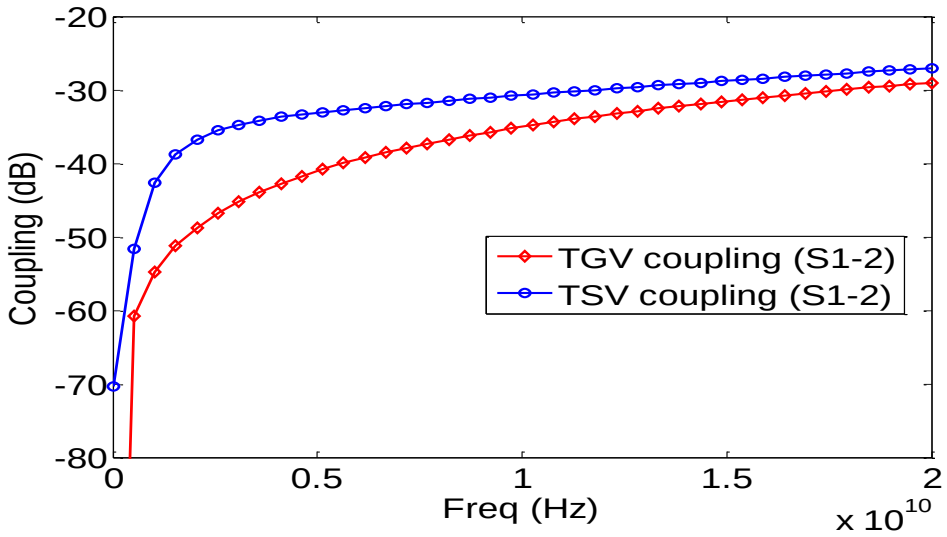
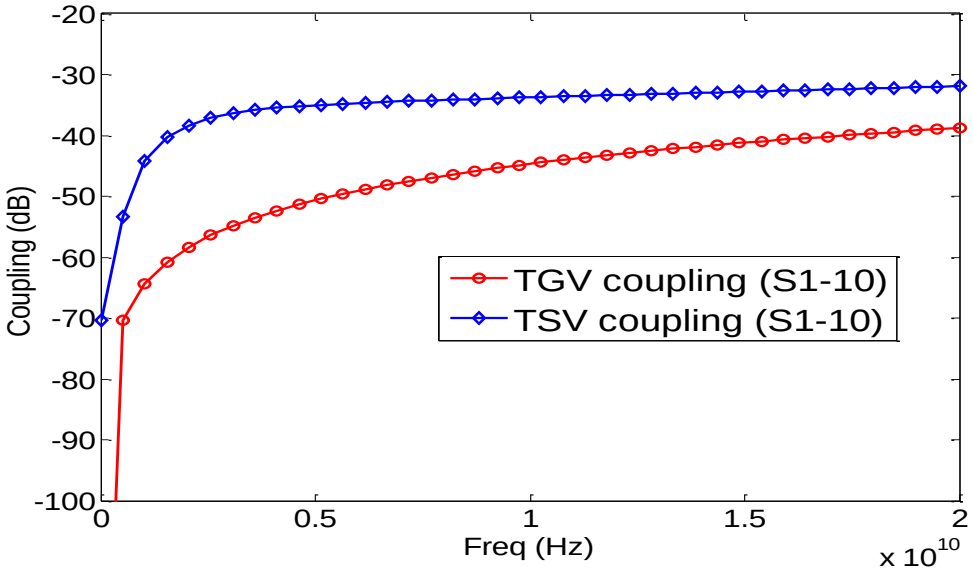


Figure 48. 8×1**TSVs/TGVs array model**



(a)



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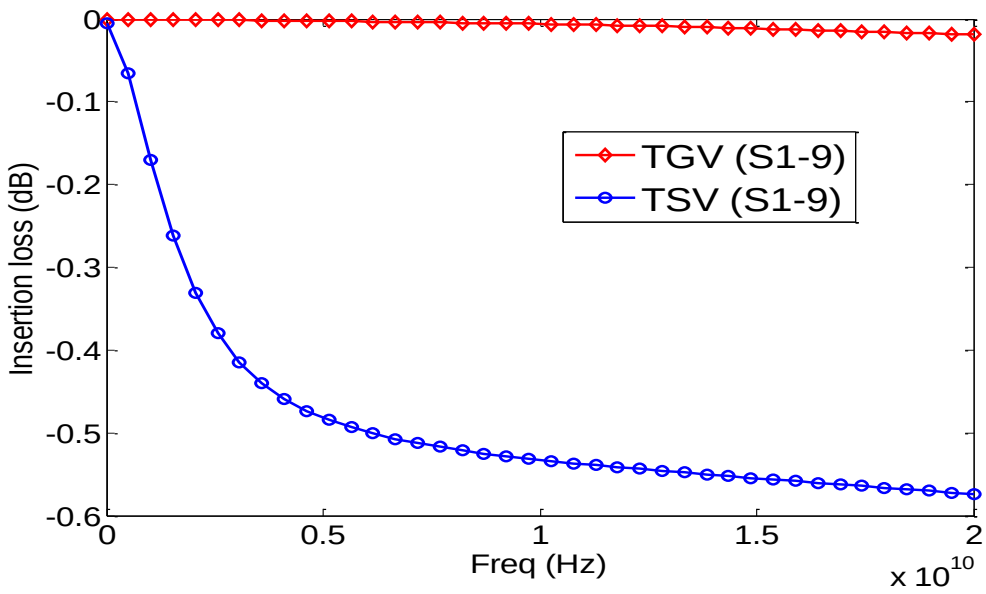


(c)

Figure 49. S-parameters of TSVs/THVs array, (a) insertion loss, (b) near end coupling, (c) far end coupling.

5.3.2 TSVs/TGVs Coupling Effects with P/G Planes Included

Consider an 8bit microstrip-via-microstrip transition structure as shown in Figure 50 with dimensions and port definition, where the test vehicle consists of four metal layers with microstrip lines (length=10mm, width=40um, thickness=10um, spacing=80um) on the top and bottom layer and P/G planes on second and third layer, respectively. Silicon (with 10 S/m conductivity and $\varepsilon_r = 11.9$) and glass (with $\varepsilon_r = 6.7$ and $\tan\delta = 0.006$) interposers are used in the test vehicle to investigate TSVs/TGVs coupling effects in different interposers between P/G planes.

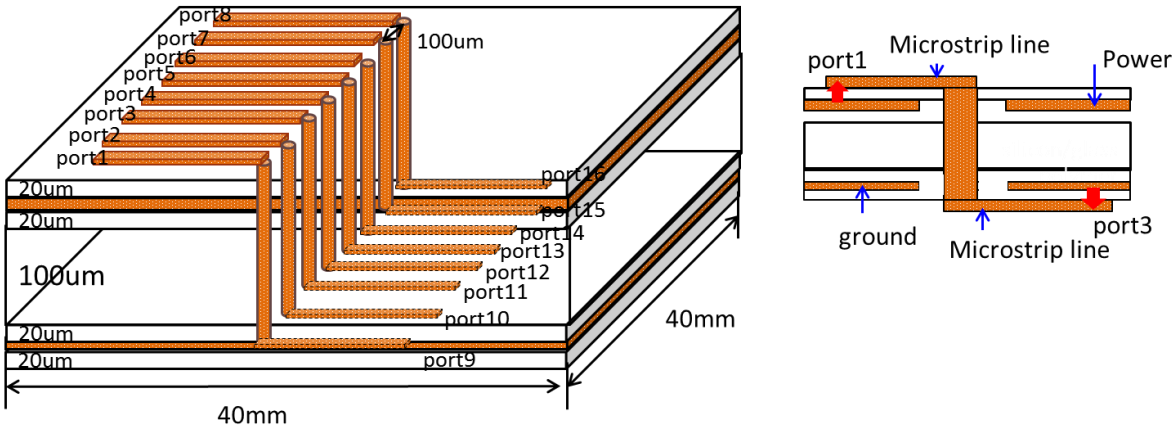
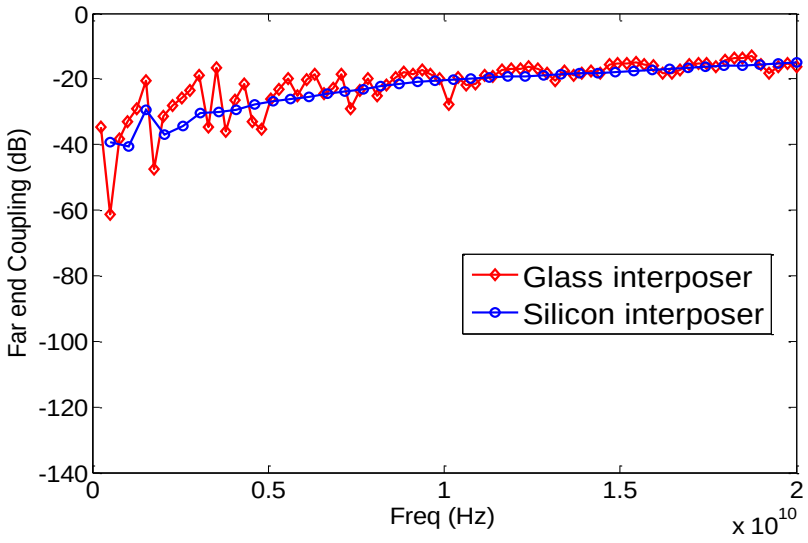
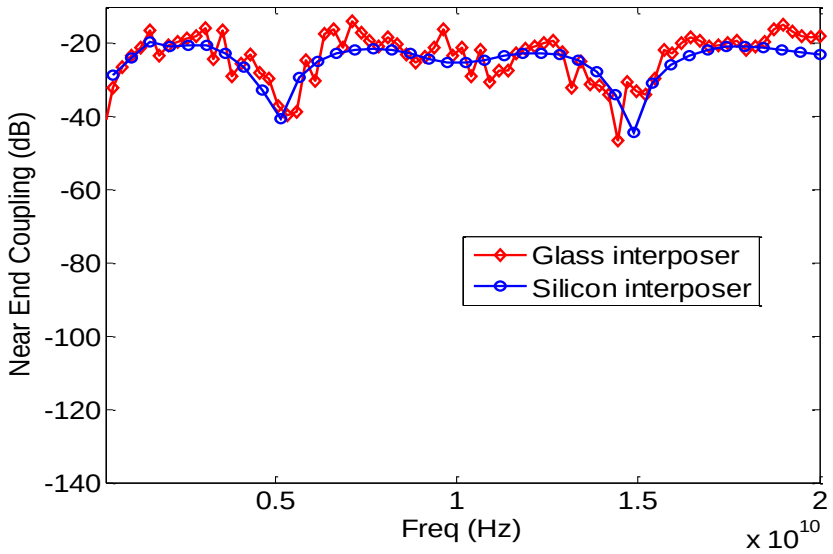


Figure 50. 8 bit microstrip-via-microstrip transition structure.

The 8 bit microstrip-via-microstrip transition structure shown in Figure 50 is co-simulated using the proposed hybrid modeling approach. The far end and near end coupling of the structure in silicon/glass interposers are compared in Figure 51. The coupling in silicon/glass interposers become similar as shown in Figure 51. To explain the increased coupling in silicon interposer, the transfer impedances for silicon/glass interposers have been obtained and shown in Figure 52. There are impedance resonances in the glass interposer. When excited at the resonance frequency, the planes can become a significant source of noise and can act as a source of edge-radiated field emission if the impedance becomes large at these frequencies [41]. Since the planes have unterminated edges, any excitation of the planes creates an electromagnetic wave that travels back and forth between the planes, and over time a standing wave is generated. The standing waves in the cavity increase the via to via coupling for the glass interposer. Since the impedance resonances get suppressed in the silicon interposer due to the lossy silicon compared to the glass interposer as shown in Figure 52, this effect is smaller. Therefore, with power and ground planes, the coupling between lines due to vias is similar for both silicon and glass interposers.

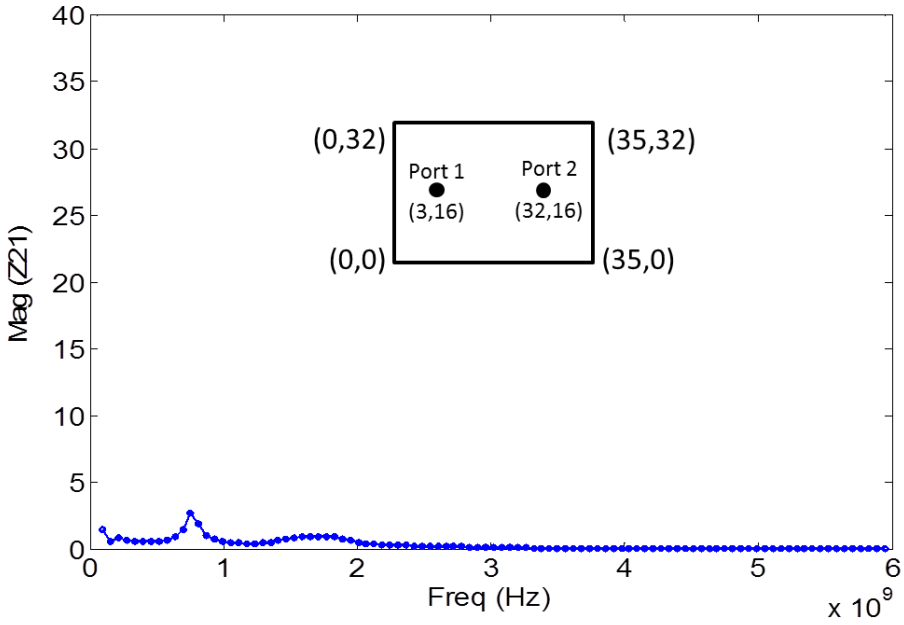


(a)

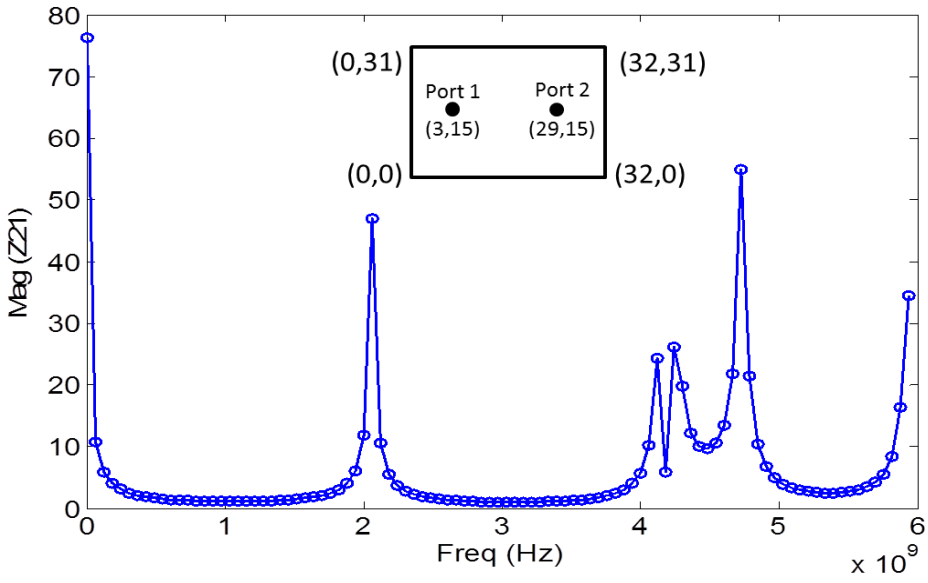


(b)

Figure 51. S-parameters of 8 bit microstrip-via-microstrip transition structure, (a) near end coupling, (b) far end coupling.



(a)



(b)

Figure 52. (a) Silicon interposer transfer impedance, (b) glass interposer transfer impedance.

5.4 SSN Comparison Between Silicon and Glass Interposer

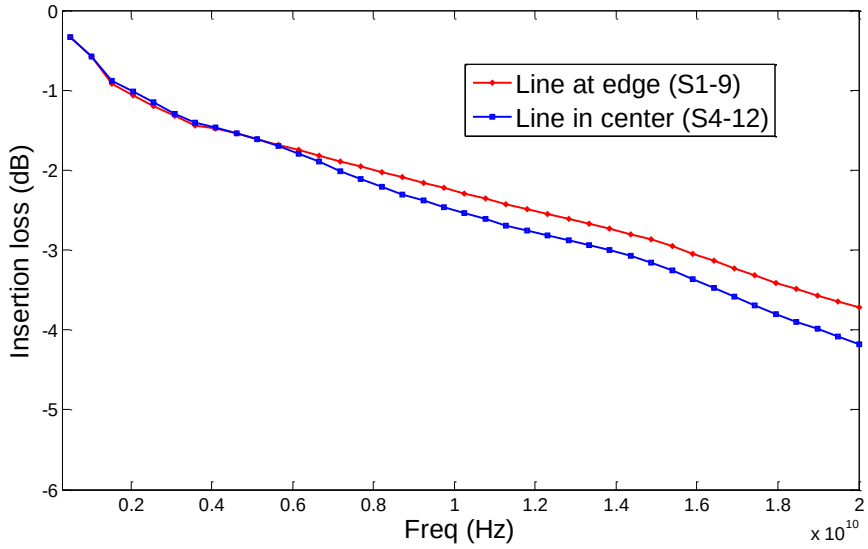
A transmission line carrying a signal will always generate a current on the signal line and the reference plane. The change in reference plane of the signal gives rise to a

discontinuity in the path of the return current. This is called the return path discontinuity (RPD). Vias can cause a RPD due to the change in reference planes when via transition occurs. This RPD leads to the excitation of the power and ground plane pair cavity which induces SSN between the two planes [41].

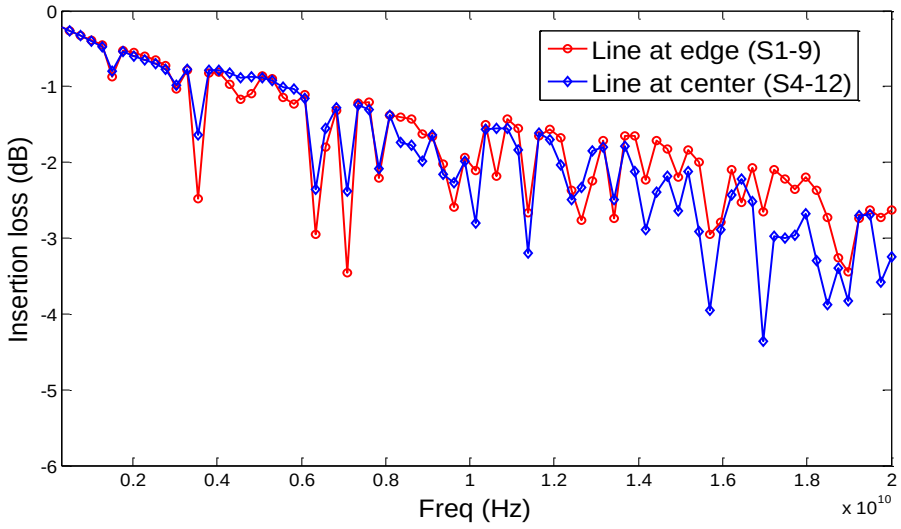
The 8 bit microstrip-via-microstrip transition structure shown in Figure 50, which has a RPD, is co-simulated using the proposed modeling technique to analyze SSN. The SSN voltage is equal to the product of the return current and PDN impedance at the RPD [46]. As the PDN impedance is a function of frequency, the SSN voltage also depends on frequency. A large SSN voltage is induced between P/G planes at the anti-resonant frequency of the PDN impedance, which correspond to the peaks in the insertion loss of the signal. The insertion losses of the signal for silicon and glass interposers are shown in Figure 53. As can be seen from Figure 53, the lossy silicon interposer has higher overall insertion loss compared to the low loss glass interposer. However, there are sharp notches in the insertion loss of the glass interposer compared to the smooth insertion loss of the silicon interposer, since the P/G plane resonances are suppressed in the silicon interposer. The insertion losses for different signals in the same interposer are also compared in Figure 53. The microstrip-via-microstrip transition in the middle (S4-12) shows a larger insertion loss compared to the microstrip-via-microstrip transition at the edge (S1-9) due to the enhanced coupling in the middle.

Figure 54 shows the eye diagram comparison obtained using ADS [47], between glass and silicon interposers for a 5Gbps random bit signal transmitted from port1~port8 to port9~port16. The frequency spectrum of the input random bit stream consists of harmonics distributed across multiple frequencies. Since the harmonics across multiple frequencies can experience varying insertion losses for glass as shown in Figure 53, it can cause uncertainties in signal rise/fall times and also uncertainties in signal amplitudes, resulting in large jitter and reduced eye height as shown in Figure 54. The eye diagrams obtained at port9 and port13 in silicon and glass interposers are also compared in Figure

54. The eye height variability between port9 and port13 is due to the difference in insertion losses between the microstrip-via-microstrip transition in the middle (S1-9) and at the edge (S4-12).

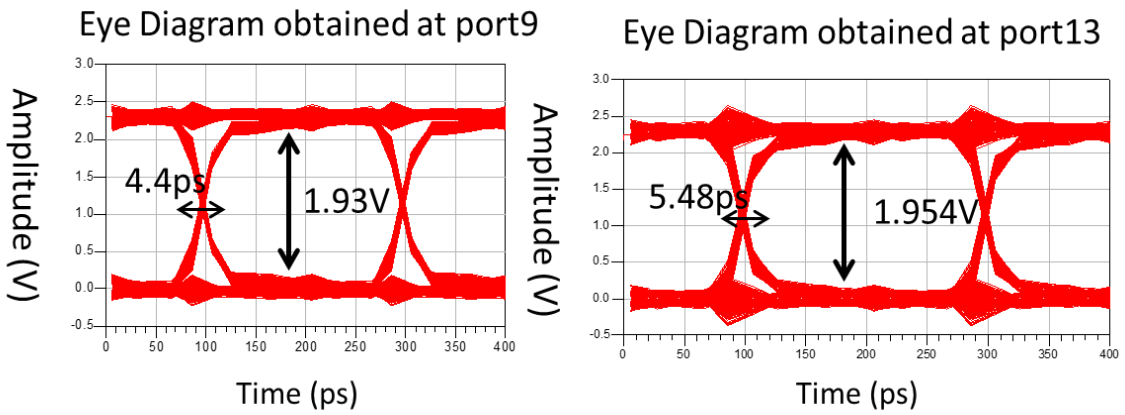


(a)

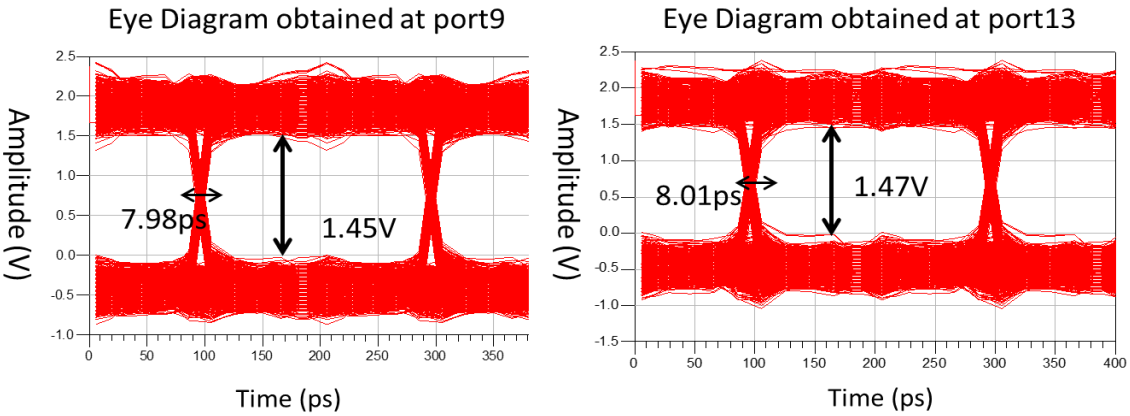


(b)

Figure 53. Insertion losses for 8 bit microstrip-via-microstrip transition structure, (a) Silicon interposer, (b) Glass interposer



(a)



(b)

Figure 54. Eye diagram for 8 bit microstrip-via-microstrip transition structure, (a) Silicon interposer, (b) Glass interposer.

5.5 Summary

This chapter proposed a hybrid modeling approach for PDNs with multiple TSVs, which can be used in power/signal integrity analysis of a PDN with TSVs for 3D systems. P/G plane resonance suppression in silicon interposers and its benefits in improving SSN compared to glass interposers have been discussed. The proposed approach combines M-FDM and an integral equation based solver for TSVs. M-FDM is efficient for modeling multilayer power/ground planes with transmission lines, while the multi-scale TSV structure is modeled separately using specialized basis functions without mesh and later

incorporated into the M-FDM. Therefore, the total number of unknowns required to model the PDN with TSVs can be greatly reduced compared with commercial full-wave solvers. One limitation of this proposed method is that it can not capture the parasitic effects of the transmission lines when they are directly above the silicon interposer. Thus, alternative approaches are needed to model the interposer when the transmission lines are directly above the silicon interposer as shown in Figure 55, which is the focus of CHAPTER 6.

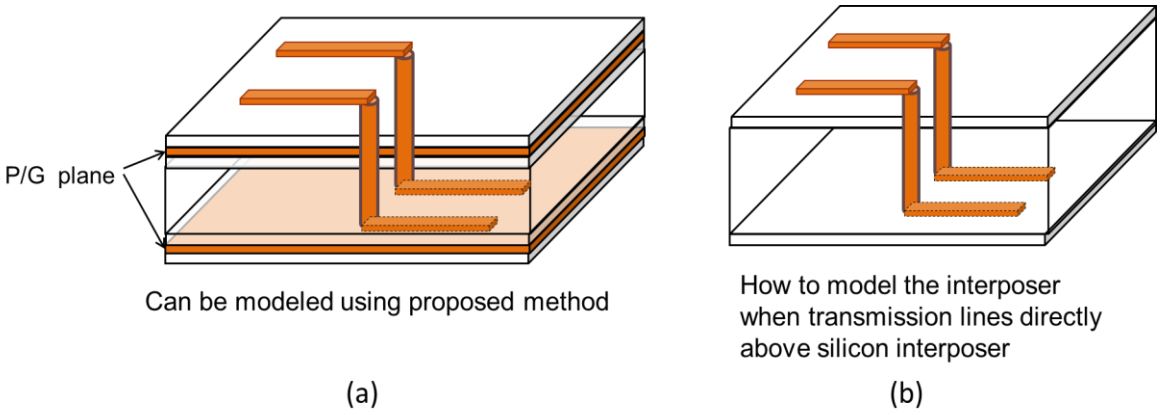


Figure 55. (a) Interposer with P/G planes (b) Transmission lines directly above silicon interposer.

CHAPTER 6

FDFD MODELING OF SIGNAL PATHS WITH TSVS IN SILICON INTERPOSER

6.1 Introduction

This chapter proposes an efficient method to address the problem of modeling signal paths in silicon interposers without power/ground planes [48]. The proposed method utilizes the 3-D finite-difference frequency-domain (FDFD) method to model the redistribution layer (RDL) transmission lines to capture the parasitic effects of multiple transmission lines on a lossy silicon interposer. TSVs are modeled using an integral equation based solver which uses cylindrical modal basis functions. A new formulation for incorporating a multiport network into the 3-D FDFD formulation is presented to include the parasitic effects of TSV arrays in the system matrix. The overall matrix is divided into several subdomains and solved by a divide-and-conquer approach in a parallel manner. The accuracy and efficiency of the proposed method is demonstrated by simulating several RDL-TSV-RDL transition structures.

The major contributions of this chapter are as follows:

(1) A new formulation for incorporating a multiport network with Y -parameters into 3-D FDFD is presented. Although several previous papers [36, 49-52] have developed the formulation on incorporating Y -parameters into FDTD, FEM, there is no previous work incorporating a multiport network into the 3-D FDFD method.

(2) Extending the divide-and-conquer formulation [53, 54] to handle the multiport network incorporated into FDFD method. Since TSVs are incorporated into FDFD method as a multiport network, details on handling the coupling between subdomains due to TSV coupling is presented.

6.2 Modeling of signal paths in silicon interposer

In this section, the basic formulation for the interconnect problem is presented. As shown in Figure 56, the interconnect problem is split into two separate problems: (1) Modeling of multiple RDL transmission lines on lossy silicon substrates using the FDFD method and (2) Modeling of TSV arrays. The TSV arrays are modeled using the integral equation based solver and incorporated into the FDFD solver as a multiport network.

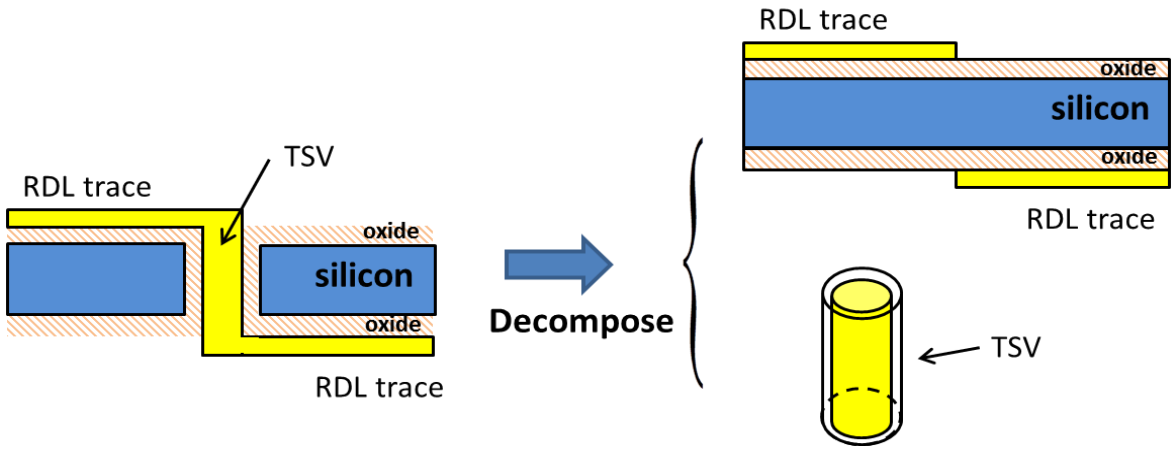


Figure 56. Decomposition of the signal path problem into two problems.

6.2.1 Modeling of Multiple RDL Traces on Lossy Silicon Interposers

The FDFD method is utilized to model the arbitrary routing of the RDL traces on the silicon interposer. The FDFD formulation is based on the susceptance element equivalent circuit (SEEC) solver [55-57] which solves Maxwell's equation using the Yee grid [58]. The formulation is briefly discussed in this section.

The differential form of Maxwell's equations in the frequency domain can be written as:

$$\nabla \times \vec{H} = j\omega\vec{D} + \sigma\vec{E} + \vec{J}_s \tag{33}$$

$$\nabla \times \vec{E} = -j\omega\vec{B} \tag{34}$$

$$\nabla \cdot \vec{D} = \rho \tag{35}$$

$$\nabla \cdot \vec{B} = 0 \tag{36}$$

where $\vec{E}$ and $\vec{H}$ are the electric and magnetic field vectors respectively, $\vec{D}$ and $\vec{B}$ are the related field/flux density vectors respectively, $\vec{J}$ is the external current density source vector, ω is the frequency in radians, σ is the position-dependent conductivity of the medium, and ρ is the electric charge density. The above vector equations for an isotropic, inhomogeneous medium can be written in scalar form in three dimensions as:

$$j\omega\varepsilon E_x = \frac{\partial H_z}{\partial y} - \frac{\partial H_y}{\partial z} - \sigma E_x \tag{37}$$

$$j\omega\varepsilon E_y = \frac{\partial H_x}{\partial z} - \frac{\partial H_z}{\partial x} - \sigma E_y \tag{38}$$

$$j\omega\varepsilon E_z = \frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y} - \sigma E_z \tag{39}$$

$$j\omega\mu H_x = -(\frac{\partial E_z}{\partial y} - \frac{\partial E_y}{\partial z}) \tag{40}$$

$$j\omega\mu H_y = -(\frac{\partial E_x}{\partial z} - \frac{\partial E_z}{\partial x}) \tag{41}$$

$$j\omega\mu H_z = -(\frac{\partial E_y}{\partial x} - \frac{\partial E_x}{\partial y}) \tag{42}$$

Substituting for the magnetic fields in the electric field equations (37)-(38), and discretizing the above equation using the Yee grid, the following equation (43) can be obtained.

$$(\mathbf{G} + s\mathbf{C} + \frac{\mathbf{\Gamma}}{s})\mathbf{E} = \mathbf{BI} \tag{43}$$

where, $\mathbf{G}, \mathbf{C}, \mathbf{\Gamma} \in \Re^{P\times P}$ represent the coefficient matrices for the given system, $\mathbf{E} \in C^{P}$ represents the vector of the unknown electrical field, $\mathbf{B} \in \Re^{P\times N}$ is the selector matrix for the excitation matrix $\mathbf{I} \in \Re^{N\times N}$, P is the number of unknowns, N is the number of ports and s is the Laplace variable. Essentially, equation (43) is the nodal analysis form of Maxwell's equations. PMC (perfect magnetic conductor) and PEC (perfect electric conductor) conditions are enforced by opening and shorting nodal points along the boundaries of the simulation domain, respectively.

The benefits of using FDFD are that it can model irregular routing of RDL traces on silicon interposers and can capture the different modes (slow wave mode and quasi-TEM mode) of the signal traces on Si-SiO2 double-layer system [59].

6.2.2 Integration of TSVs and RDL traces

The cylindrical TSV structure requires a large number of mesh elements to approximate when using the rectangular grids in FDFD method, therefore, TSV arrays can be modeled using an integral equation based solver. The response of TSV arrays can be incorporated into the FDFD modeling of RDL traces as a multiport network to obtain the system level response of silicon interposer, as shown in Figure 57.

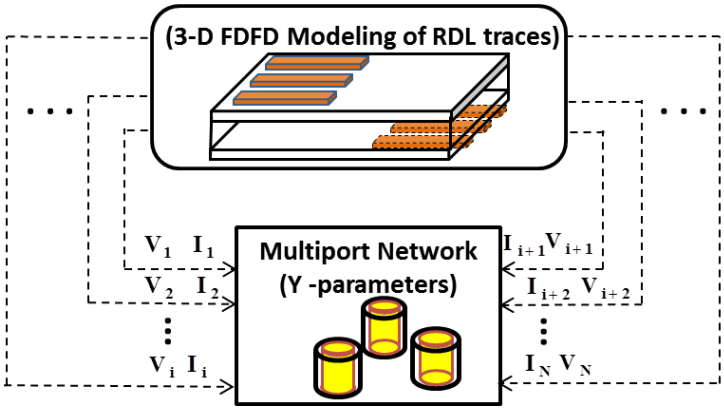


Figure 57. Incorporating multiport network into 3-D FDFD.

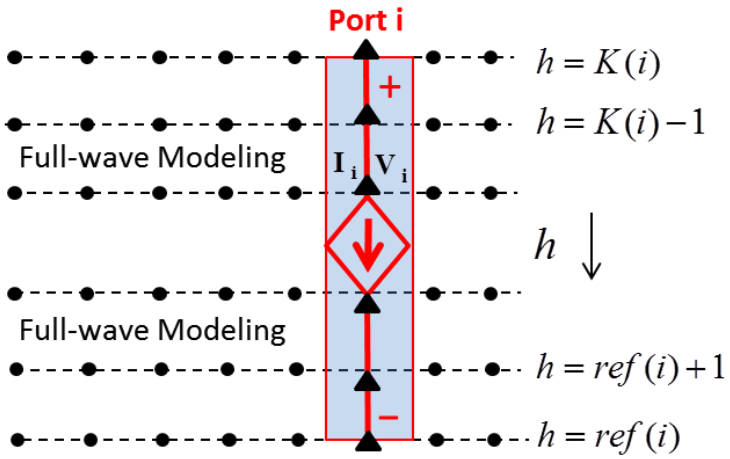


Figure 58. Cross-sectional view of port i which occupies multiple cells in FDFD Yee grid.

The multiport network with Y-parameters can be described using the dependent current source I_i and voltages V_i according to the following equation:

$$I_i(V_1, V_2 \cdots V_N) = \sum_{j=1}^{N} Y_{ij} V_j \qquad i = 1 \sim N \tag{44}$$

where index i represents the port index of the multiport network and N represents the total number of ports. Each port of the multiport network may occupy multiple grids in the Yee grid as shown in Figure 58, where port i is represented by a current source I_i flowing along the *h*- direction. In the Yee grid, the voltage V_j can be written in terms of the *h*- component of electric field E_h as:

$$V_j = \sum_{h=ref}^{j} E_h \Delta h \tag{45}$$

where *ref* represents the voltage reference node in the Yee grid. After substituting equation (45) into equation (44), the current source I_i expressed as current density can be obtained as:

$$J_i(V_1 \cdots V_N) = \frac{I_i(V_1 \cdots V_N)}{Area} = \sum_{j=1}^{N} Y_{ij} \sum_{h=ref}^{j} \frac{E_h \Delta h}{Area} \tag{46}$$

where $Area$ is the cross-sectional area of the Yee cell. At each port i of the multiport network, the equivalent current source $J_i(V_1 \cdots V_N)$ must be applied to all the FDFD nodes from the reference node $[x(i), y(i), ref(i)]$ to the port definition node $[x(i), y(i), K(i)]$ along the *h*- direction in the Yee grid, as shown in Figure 58. This can be described using the matrix operation expressed in Figure 59, where $\mathbf{A} = \mathbf{G} + s\mathbf{C} + \frac{\mathbf{\Gamma}}{s} \in \Re^{P \times P}$ is the system matrix obtained using FDFD before the multiport network is incorporated, $\mathbf{A}_{\mathbf{sys}} \in \Re^{P \times P}$ is the overall system matrix after the multiport network is incorporated, P is the number of unknowns, $[x(i), y(i), ref(i)+m]$, $[x(i), y(i), K(i)-n]$ represent the column (row) number of the matrix where the current density J_i must be stamped and N is the total number of ports.

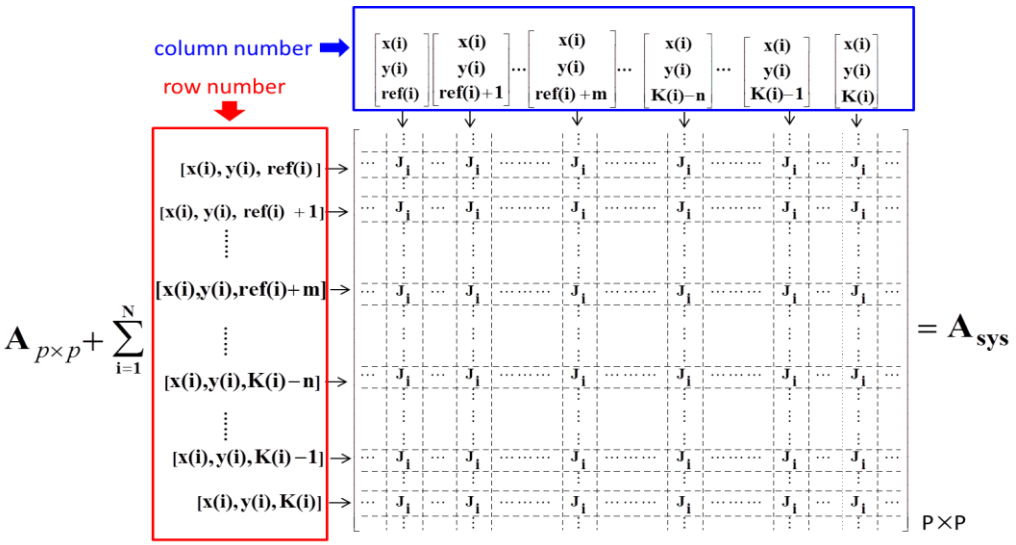


Figure 59. Matrix operation for incorporating multiport network into 3-D FDFD

The benefit of using this approach is that the TSVs which are cylindrical and require a large number of mesh elements to approximate using FDFD method can be modeled separately and later incorporated into the FDFD simulation as a multiport network. This

approach does not consider the coupling between TSVs and RDL traces. It is concluded in [60] that the TSV-to-RDL coupling is negligible if the ratio of TSV length and TSV diameter is larger than 5. The accuracy of this approach is validated in section 6.4.

6.3 Divide-and-Conquer Method

In this section, a divide-and-conquer method using parallel computing is presented to solve the system matrix equation:

$$\mathbf{A}_{sys}\mathbf{E} = \mathbf{BI} \tag{47}$$

where **B** and **I** take the same meaning as in equation (43). The formulation for the divide-and-conquer approach is extended from [53, 54] to solve the interconnect problem where TSVs are incorporated as a multiport network and therefore there is coupling between subdomains due to coupling between TSVs.

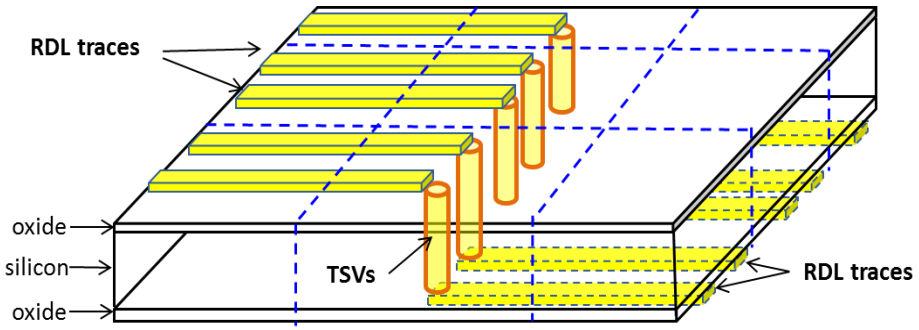


Figure 60. RDL traces and TSVs in silicon interposer. Dot lines show how the subdomains are created.

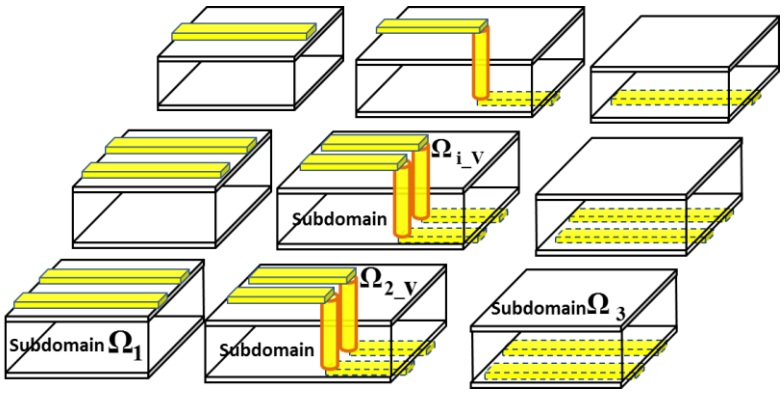


Figure 61. *M* subdomains of the silicon interposer shown in Figure 39.

The RDL traces and TSV transition structure shown in Figure 60 is denoted as Ω with boundary $\partial\Omega$. This structure can be divided into M subdomains Ω_i and M interfaces Γ_i as shown in Figure 61. The interfaces should not overlap with the locations of TSVs since TSVs are incorporated as a multiport network and Y-parameters of TSVs can not be stamped at the interfaces. The subdomains can be created arbitrarily provided that the interfaces do not overlap with the locations of TSVs. The subdomain is denoted as Ω_{i_v} if there are TSVs in this subdomain. The interface between the subdomains is defined as $\Gamma_i = \partial\Omega_i \bigcap \partial\Omega_j$. As a result, the following equations (48) and (49) must be satisfied for the completeness of the entire domain Ω.

$$\Omega = \Omega_1 \bigcup \cdots \bigcup \Omega_{i\_v} \cdots \bigcup \Omega_M \bigcup \Gamma \tag{48}$$

where $\Gamma = \Gamma_1 \bigcup \cdots \bigcup \Gamma_M$

$$\Omega_i \bigcap \Omega_j = \varnothing \text{ and } \Gamma_i \bigcap \Gamma_j = \varnothing \text{ when } i \neq j \tag{49}$$

According to the definitions in equation (48) and (49), there are two types of subdomains. (1) Subdomains without TSVs (denoted as Ω_i), where there is no direct coupling of this subdomain to other subdomains since the couplings are stored as interfaces Γ_i. (2) Subdomains with TSVs (denoted as Ω_{i_v}), where the coupling of this subdomain to other subdomains still exists due to coupling between TSVs, as shown in Figure 62.

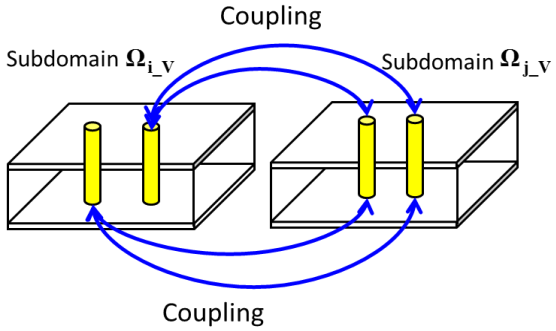


Figure 62. Coupling between two subdomains due to the coupling between TSVs.

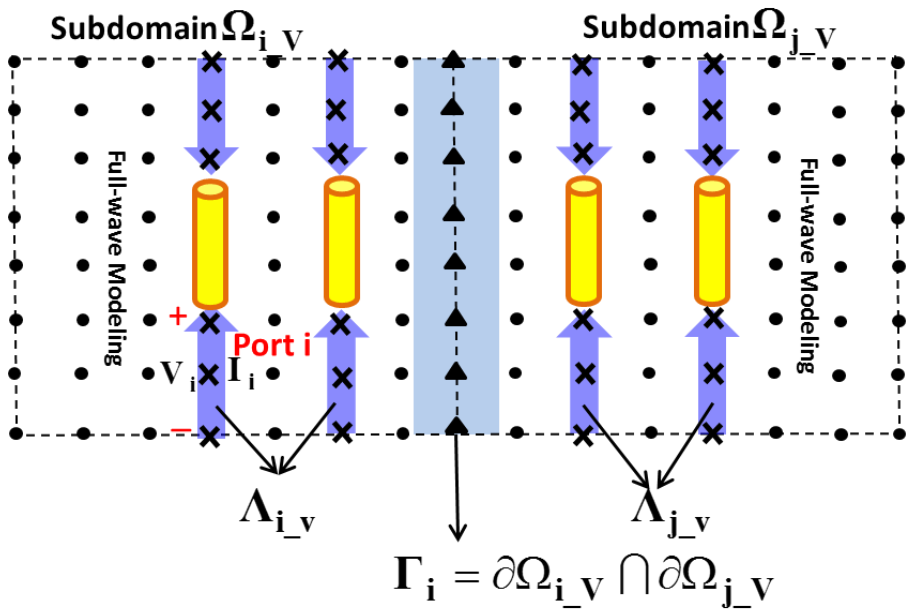


Figure 63. Cross-sectional view of two subdomains with TSVs in the FDFD grid. Triangle dots: interface unknowns between subdomains. X-shaped dots: the unknowns that introduce coupling due to TSvs.

The coupling is induced by the unknowns in the nodes (denoted as Λ_{i_v}) where the current density $J_i(V_1 \cdots V_N)$ in equation (11) has been applied, as shown in Figure 63. In order to utilize the divide-and-conquer and parallel computing method to solve each subdomain simultaneously, there should be no coupling between subdomains. Therefore, the unknowns in Λ_{i_v} are removed from subdomains Ω_{i_v} and placed into the corresponding interface unknowns Γ_{i_v}. As a result, equations (48) and (49) can be rewritten as equations (50) and (51).

$$\Omega = \Omega_1 \bigcup \cdots \bigcup (\Omega_{i\_v} - \Lambda_{i\_v}) \cdots \bigcup \Omega_M \bigcup \Gamma \tag{50}$$

where $\Gamma = \Gamma_1 \bigcup \cdots \bigcup (\Gamma_{i\_v} + \Lambda_{i\_v}) \cdots \bigcup \Gamma_M$

$$\Omega_i \bigcap \Omega_j = \varnothing \text{ and } \Gamma_i \bigcap \Gamma_j = \varnothing \text{ when } i \neq j \tag{51}$$

The unknowns, namely the field variables on the grids, are reordered starting with the ones in subdomains Ω_1, followed by those in Ω_2, $\cdots$, $\Omega_{i\_\mathrm{v}} - \Lambda_{i\_\mathrm{v}}$, $\cdots$, Ω_M, and ending with those on interfaces Γ as defined in equations (50)and (51). After reordering, the matrix equation (47) can be converted to the matrix equation:

$$\begin{bmatrix} \mathbf{A}_{11} & & & & & & \mathbf{C}_1 \\ & \mathbf{A}_{22} & & & & & \mathbf{C}_2 \\ & & \ddots & & & & \vdots \\ & & & \mathbf{A}_{ii\_v} & & & \mathbf{C}_{i\_\mathrm{v}} \\ & & & & \ddots & & \vdots \\ & & & & & \mathbf{A}_{MM} & \mathbf{C}_M \\ \mathbf{C}_1^T & \mathbf{C}_2^T & \cdots & \mathbf{C}_{i\_\mathrm{v}}^T & \cdots & \mathbf{C}_M & \mathbf{\Gamma} \end{bmatrix} \begin{bmatrix} \mathbf{e}_1 \\ \mathbf{e}_2 \\ \vdots \\ \mathbf{e}_{i\_\mathrm{v}} \\ \vdots \\ \mathbf{e}_M \\ \mathbf{e}_\Gamma \end{bmatrix} = \begin{bmatrix} \mathbf{b}_1 \\ \mathbf{b}_2 \\ \vdots \\ \mathbf{b}_{i\_\mathrm{v}} \\ \vdots \\ \mathbf{b}_M \\ \mathbf{b}_\Gamma \end{bmatrix} \tag{52}$$

where $\mathbf{A}_{ii}$ or $\mathbf{A}_{ii\_\mathrm{v}}$ is the matrix corresponding to subdomain Ω_i or $(\Omega_{i\_\mathrm{v}} - \Lambda_{i\_\mathrm{v}})$. The vector $\mathbf{e}_1, \mathbf{e}_2, \cdots, \mathbf{e}_{i\_\mathrm{v}}, \cdots \mathbf{e}_M$ represents the field unknowns of subdomains. The vector $\mathbf{x}_\Gamma$ represents the field unknowns on the interface. There is no direct coupling between the unknowns of any subdomains and the coupling between the subdomains and interfaces can be represented by the submatrices $\mathbf{C}_i$ or $\mathbf{C}_{i\_\mathrm{v}}$. If the number of unknowns in each subdomain Ω_i or $(\Omega_{i\_\mathrm{v}} - \Lambda_{i\_\mathrm{v}})$ is defined as n_i and the number of unknowns on the interface Γ is defined as n_s, then the matrix sizes of $\mathbf{A}_{ii}$ ($\mathbf{A}_{ii\_\mathrm{v}}$), $\mathbf{C}_i$ ($\mathbf{C}_{i\_\mathrm{v}}$), $\mathbf{\Gamma}$ are $n_i \times n_i$, $n_i \times n_s$ and $n_s \times n_s$,respectively.

The Schur complement system [53] is given by

$$\mathbf{S}\mathbf{e}_\Gamma = \mathbf{g} \tag{53}$$

where $\mathbf{S} = \mathbf{C}_\Gamma - \sum_{i=1}^{M} \mathbf{C}_i^T \mathbf{A}_{ii(ii\_v)}^{-1} \mathbf{C}_i$ and $\mathbf{g} = \mathbf{b}_\Gamma - \sum_{i=1}^{M} \mathbf{C}_i^T \mathbf{A}_{ii(ii\_v)}^{-1} \mathbf{b}_i$

It can be seen that the subdomains $\mathbf{A}_{ii}$ or $\mathbf{A}_{ii\_v}$ are independent of each other, so that each term $\mathbf{C}_i^T \mathbf{A}_{ii(ii\_\mathrm{v})}^{-1} \mathbf{C}_i$ in the summation $\sum_{i=1}^{M} \mathbf{C}_i^T \mathbf{A}_{ii(ii\_\mathrm{v})}^{-1} \mathbf{C}_i$ can be calculated simultaneously

in a parallel manner. Once the Schur complement has been solved, equation (54) can be decoupled by solving the subdomain problem:

$$\mathbf{A}_{ii(ii\_v)}\mathbf{e}_{i(i\_v)} = \mathbf{g}_i \tag{54}$$

where $\mathbf{g}_i = \mathbf{b}_i - \mathbf{C}_{i(i\_v)}\mathbf{x}_\Gamma$. The subdomain problems can be solved in parallel since the subdomains $\mathbf{A}_{ii}$ and $\mathbf{A}_{ii\_v}$ are independent of each other. The parallel divide-and-conquer algorithm can be summarized as:

(1) Reorder the system matrix $\mathbf{A}_{\mathbf{sys}}$ according to the subdomains and interfaces defined in equations (50) and (51) to obtain the matrix equation (52).

(2) Use parallel computing to calculate the summation $\sum_{i=1}^{M}\mathbf{C}_i^T\mathbf{A}_{ii(ii\_v)}^{-1}\mathbf{C}_i$ and then obtain the Schur complement matrix $\mathbf{S}$.

(3) Solve equation (53) for interface unknowns $\mathbf{e}_\Gamma$.

(4) Solve subdomains (54) simultaneously.

6.4 Numerical Examples

This section applies the proposed modeling approach to various RDL transmission lines connected to TSVs. The first two examples consist of an RDL-TSV-RDL and a differential RDL-TSV-RDL transition structure. These two examples are used to validate the accuracy of the proposed approach in Section 6.2 for incorporating a multiport network into FDFD. In the third example, a five RDL-TSV-RDL transition structure is simulated to consider the coupling effects between multiple RDL transmission lines and TSVs. In the fourth example, the RDL traces are routed irregularly on the silicon interposer and connected to a 7×2 TSV array. This example shows that the proposed approach is able to handle irregular routing of RDL traces and larger TSV arrays. Finally in the fifth example, multiple long RDL traces are considered and an eight RDL-TSV-

RDL transition structure is simulated. The efficiency of the proposed approach has been compared with a direct solver and an iterative quasi-minimal residual (QMR) method [57, 61].

6.4.1 RDL-TSV-RDL Transition Structure

The first example with dimensions and port setup is shown in Figure 64. Two 4 μm thick silicon dioxide layers (with dielectric constant $\varepsilon_r = 3.9$) are on both sides of 200 μm thick silicon substrate (with dielectric constant $\varepsilon_r = 11.9$ and silicon conductivity $\sigma = 10 S/m$). The length and width of the RDL trace is 2.4 mm/20 mm and 40 μm respectively. The length, radius and oxide liner thickness of the TSV is fixed at 200 μm, 15 μm and 1 μm respectively. The entire structure is enclosed in a perfect electric conductor box with dimensions $400\mu m \times 2400\mu m \times 280\mu m$ / $400\mu m \times 20mm \times 280\mu m$ and is discretized using a cell size of $20\mu m \times 40\mu m \times 4\mu m$. Figure 65 shows the FDFD mesh grid for modeling RDL traces. This structure is solved directly without dividing into subdomains after the TSVs are incorporated as a multiport network into FDFD. The RDL trace model in CST Microwave Studio (MWS) is chosen with thickness of 10 μm and conductivity of $\sigma = 5.8 \times 10^7 S/m$.

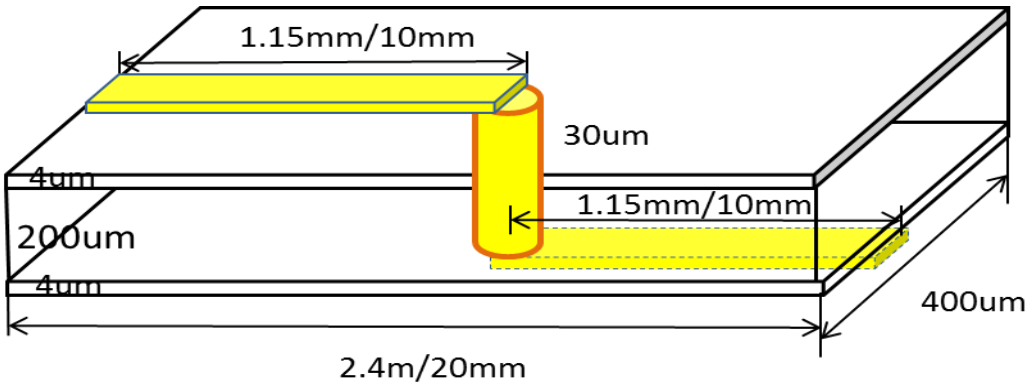


Figure 64. RDL-TSV-RDL transition structure.

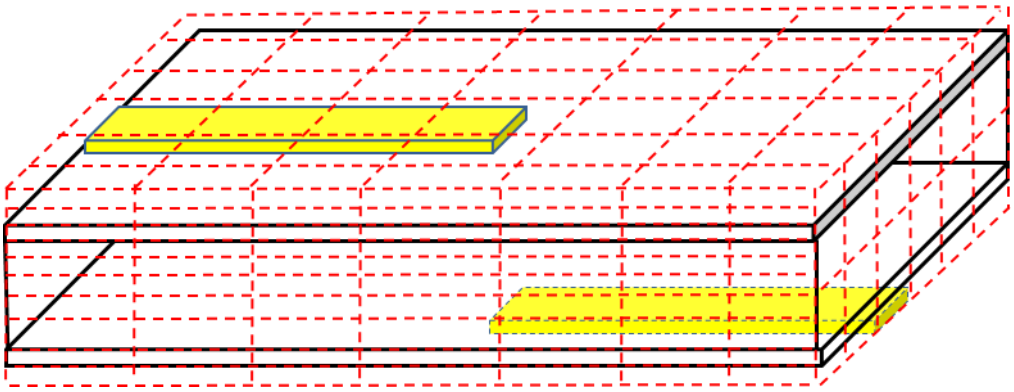
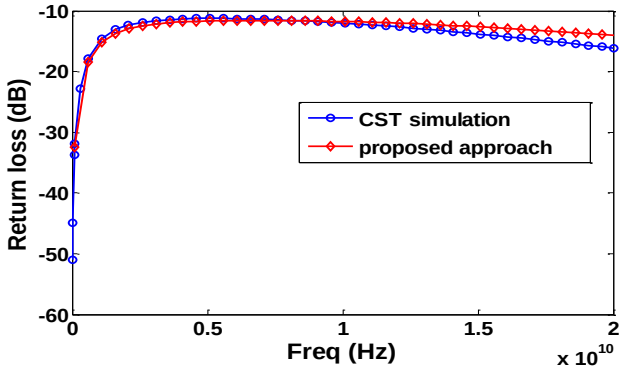
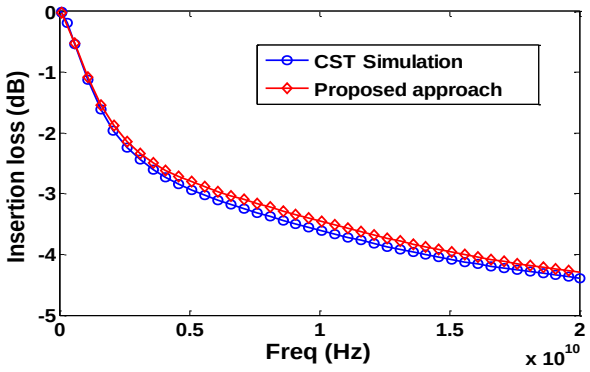


Figure 65. FDFD mesh grid for modeling RDL traces

As can be seen from Figure 66 and Figure 67, the insertion loss and return loss data for this transition structure from the proposed modeling approach and CST Microwave Studio show good correlation over a bandwidth of 20GHz.

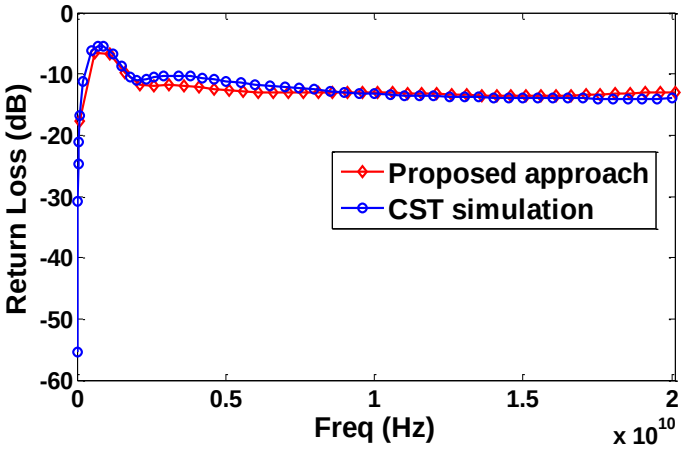


(a)

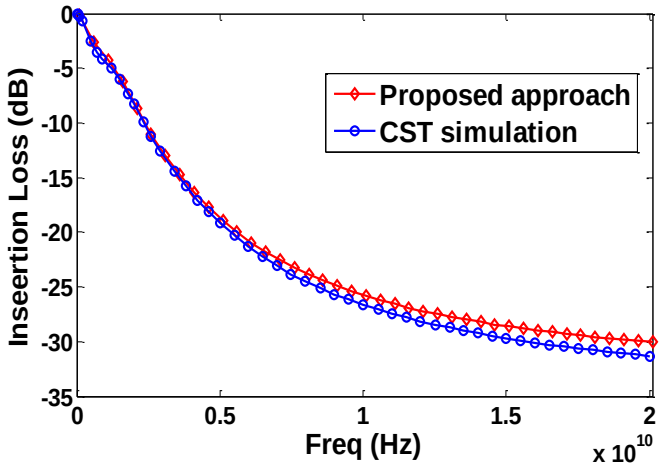


(b)

Figure 66. S-parameters of one RDL-TSV-RDL transition structure with RDL length 2.4mm, (a) Return loss, (b) Insertion loss.



(a)



(b)

Figure 67. S-parameters of one RDL-TSV-RDL transition structure with RDL length 20mm, (a) Return loss, (b) Insertion loss.

6.4.2 Five RDL-TSV-RDL Transition Structure

In the second example, multiple RDL transmission lines and TSV arrays are considered. The five RDL-TSV-RDL transition structure with dimensions and port definition is shown in Figure 68. Two 4 μm thick silicon dioxide layers are on both sides of a 200 μm thick silicon substrate. The length, width and spacing of the multiple RDL traces are 1.2 mm, 40 μm and 20 μm respectively. The length, radius, pitch and oxide thickness of the 5×1 TSV arrays are 200 μm, 15 μm, 60 μm and 1 μm respectively. The entire

structure is enclosed in a perfect electric conductor box with dimensions $600\mu m \times 1200\mu m \times 280\mu m$ and is discretized using a cell size of $10\mu m \times 50\mu m \times 4\mu m$. This structure is divided into 15 subdomains with each subdomain the size of $200\mu m \times 240\mu m \times 280\mu m$ and the divide-and-conquer approach is utilized to solve each subdomain simultaneously.

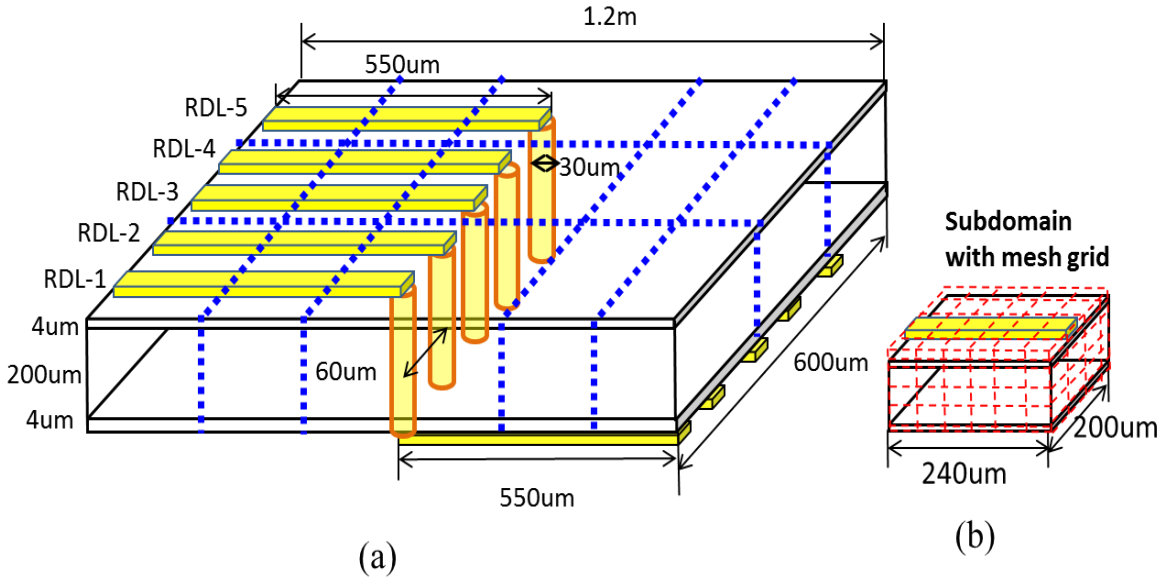


Figure 68. (a) Five RDL-TSV-RDL transition structure, dotted lines shows how the subdomains are created. (b) Subdomain with mesh grids.

The computational times and memory consumption to simulate the RDL-TSV-RDL transition structure using the proposed method, direct solver and iterative QMR method are compared in Table 4. The direct solver in Matlab is a variant of LU decomposition that finds triangular factors L, U so that $A = LU$, and then the system matrix is solved based on the LU decomposition. The QMR method [61] is an iterative method that start from an initial guess and improve the approximation until an absolute error is less than the pre-defined tolerance. All the simulations were performed on a computer with two Intel 2.4 GHz 6-core processors with 48GB memory. As can be seen from Table 4, the proposed method is efficient and consumes less memory compared to direct solver which

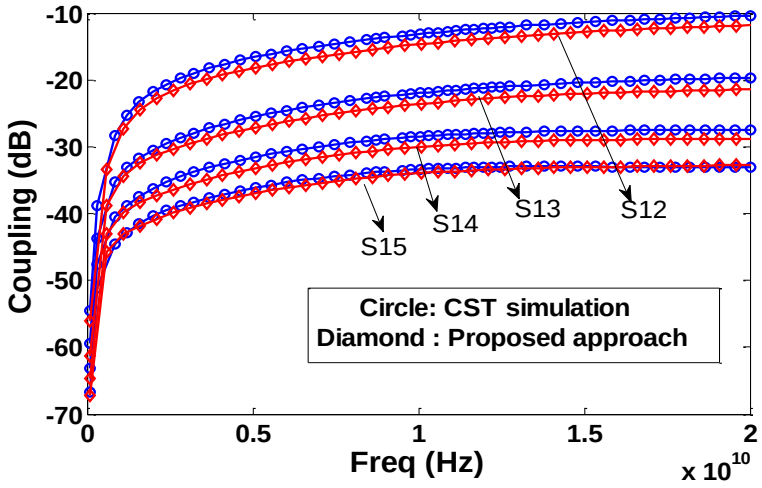
requires about 27-45GB memory. Although the QMR method uses only a small amount of memory, the computational time is too long.

The coupling between RDL-TSV-1 and other RDL-TSVs (RDL-TSV-2, RDL-TSV-3, RDL-TSV-4, RDL-TSV-5) are compared with CST [29] simulations and show good correlation up to 20GHz as illustrated in Figure 69(a). The correlation indicates that the proposed method captures all the coupling effects of the TSV arrays and multiple RDL traces.

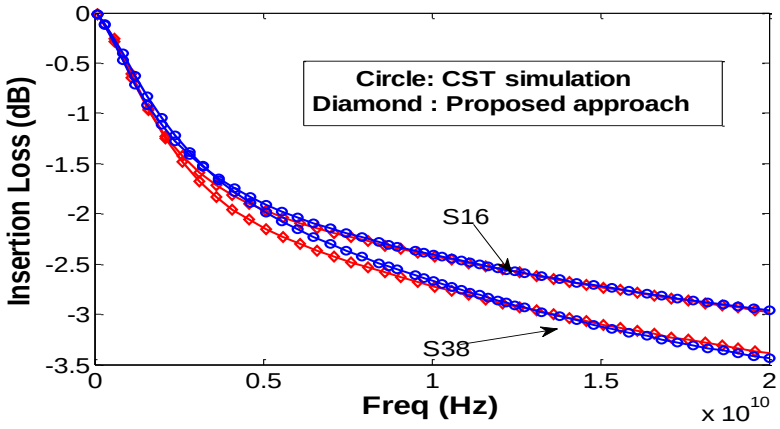
The insertion loss illustrated in Figure 69(b) shows good correlation with CST simulations up to 20 GHz. It can be seen that the RDL-TSV-RDL transition in the middle (S38) shows a larger insertion loss compared to the RDL-TSV-RDL transition at the edge (S16) due to the enhanced coupling in the middle.

Table 4. Comparison of the proposed method, direct solver, QMR method, and CST

Example		CPU time per freq. (sec.) / memory (GB)		
	Direct solver	QMR [61]	CST [29]	Proposed method
Case 2:	482s /~27GB	>3600s /~0.9 GB	~700s/~6.3GB	131s /~ 3.7GB
Case 3:	>1200s /~37GB	>3600s /~0.9GB	~1200s/~12GB	358s/~6GB
Case 4:	>1200s /~45GB	>3600s /~0.9GB	N/A	550s/~8.5GB



(a)



(b)

Figure 69. S-parameters of five RDL-TSV-RDL transition structure, (a) Coupling S15, S14, S13, and S12, (b) Insertion loss S16 and S38.

6.4.3 Irregular RDL Transmission Line Routing With Large TSV Arrays

This example considers irregular routing of the RDL transmission lines on a silicon substrate and large TSV arrays. The structure with dimensions and port definition is shown in Figure 70. Two $4\,\mu m$ thick silicon dioxide layers are on both sides of a $200\,\mu m$ thick silicon substrate. The length, radius, pitch in x direction, pitch in y direction and oxide thickness of the 7×2 TSV array are $200\,\mu m$, $15\,\mu m$, $80\,\mu m$, $100\,\mu m$ and $1\,\mu m$ respectively. The geometries of the RDL traces are described in Figure 70. The entire

structure is enclosed in a perfect electric conductor box with dimensions $900\mu m \times 1200\mu m \times 280\mu m$ and is discretized using a cell size of $20\mu m \times 20\mu m \times 4\mu m$. This structure is divided into 20 subdomains with each subdomain the size of $220\mu m \times 240\mu m \times 280\mu m$ and each subdomain is solved simultaneously using the divide-and-conquer approach. The computational times and memory consumption to simulate this structure using the proposed method, direct solver and iterative QMR method are compared in Table 4.

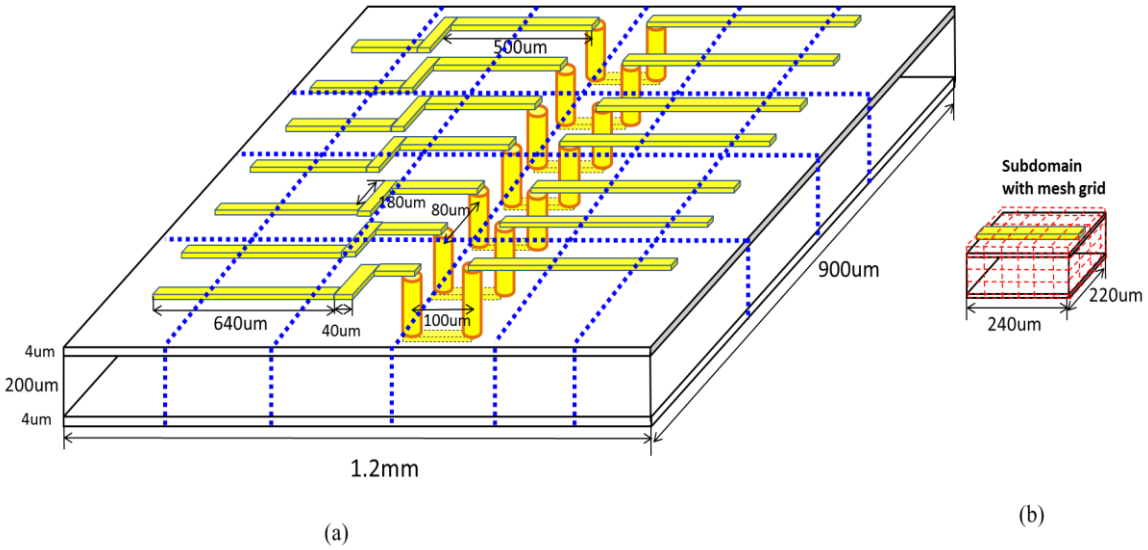
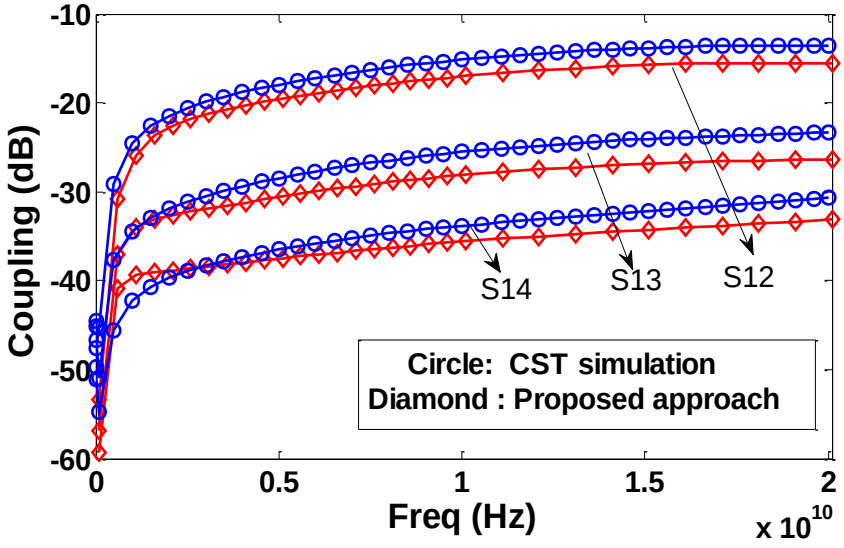
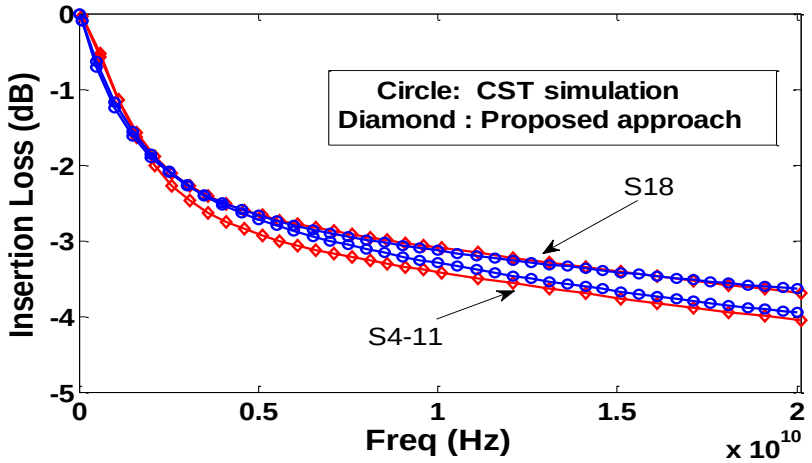


Figure 70. (a) Irregular RDL traces routing with TSV array, dotted lines show how the subdomain are created. (b) Subdomain with mesh grids.

The insertion loss and coupling of this structure obtained from the proposed approach and full-wave simulation are compared in Figure 71. Good correlation with the results from CST MWS shows that the proposed method is applicable to general irregular geometric configurations of RDL transmission lines.



(a)



(b)

Figure 71. S-parameters of seven irregular RDL-TSV-RDL transition structure. (a) Coupling S12, S13, and S14. (b) Insertion loss at the edge (S18) and in the center (S4-11).

6.4.4 Eight Long RDL Transmission Line to TSV Transitions

This example applies the proposed modeling method to multiple long RDL transmission lines connected to a 8×1 TSV array. The eight RDL-TSV-RDL transition structure with dimensions and port definition is shown in Figure 72. Two $4\,\mu m$ thick silicon dioxide layers are on both sides of a $200\,\mu m$ thick silicon substrate. The length, width and spacing

of the multiple RDL traces are 10 mm, 40um and 20um respectively. The length, radius, pitch and oxide thickness of the 8×1 TSV arrays are 200um, 15um, 80 μm and 1 μm respectively. The entire structure is enclosed in a perfect electric conductor box with dimensions $800\mu m\times10mm\times280\mu m$ and is discretized using a cell size of $20\mu m\times40\mu m\times4\mu m$. This structure is divided into 21 subdomains with each subdomain the size of $260\mu m\times1400\mu m\times280\mu m$ and each subdomain is solved simultaneously using the divide-and-conquer approach. The computational times and memory consumption to simulate this structure using the proposed method, direct solver and iterative QMR method are compared in Table 4.

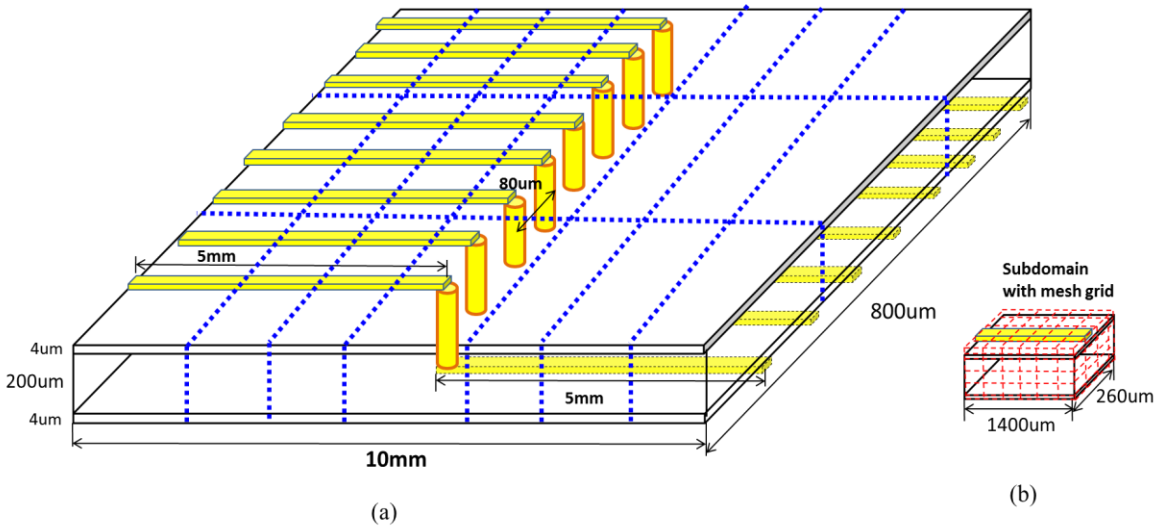
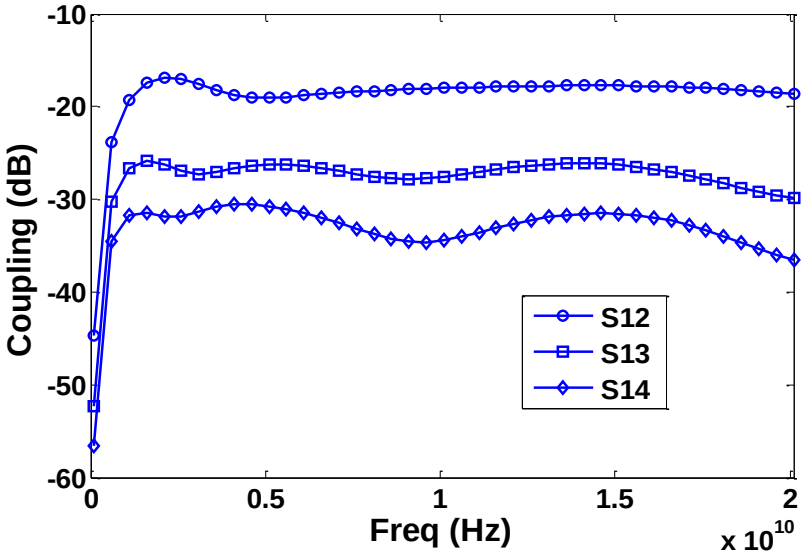
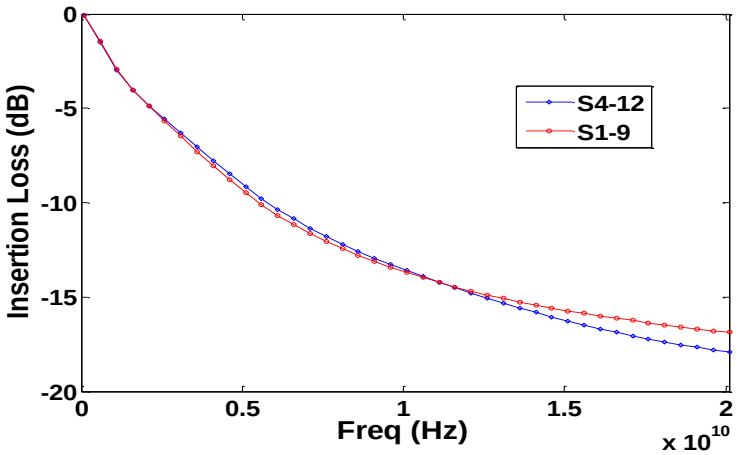


Figure 72. (a) Multiple long RDL traces routing with 8×1 TSV array, dotted lines show how the subdomains are created. (b) Subdomain with mesh grids

The insertion loss and coupling of this structure obtained from the proposed approach are shown in Figure 73. There are some resonances in the coupling due to the long RDL traces. In addition, due to the long lines directly over the silicon, the insertion loss is very high.



(a)



(b)

Figure 73. S-parameters of eight RDL-TSV-RDL transition structure, (a) Coupling S12, S13, and S14, (b) Insertion loss at edge (S19) and in the center (S4-12).

6.5 Summary

This chapter presents an efficient EM-based modeling approach for the RDL transmission lines and TSVs in silicon interposers for 3-D integration. In this approach, TSV arrays are modeled using an integral equation based solver without meshing and RDL transmission lines are modeled using FDFD method. A new formulation for

incorporating a multiport network is presented to incorporate the responses of TSV arrays into the FDFD modeling of RDL traces. A divide-and-conquer approach is used to solve the entire system matrix. The proposed approach has the advantage that the multi-scale structures such as TSVs which require large amount of mesh elements to approximate using FDFD can be modeled separately and the complex system can be divided into subdomains which can be solved simultaneously. The validation examples show good correlation between the proposed approach and full-wave EM simulations. The capability to address a large number of RDL transmission lines and TSVs shows that the proposed modeling approach provides for a better modeling environment for electrical design of the signal paths in silicon interposer for 3D systems.

CHAPTER 7

FDFD NON-CONFORMAL DOMAIN DECOMPOSITION FOR MODELING OF INTERCONNECTIONS IN SILICON INTERPOSER

7.1 Introduction

The 3-D Finite-Difference Frequency-Domain (FDFD) method based on the susceptance element equivalent circuit (SEEC) has been presented for solving a variety of electromagnetic (EM) problems [55]. The equivalent circuit-based full-wave solver offers several advantages: 1) use of SPICE [62] for full-wave simulations and 2) use of circuit-based numerical techniques [56]. However, as the problem size increases, the huge requirement in terms of time and memory quickly becomes a bottleneck. Domain decomposition is a technique that allows modeling each domain independently based on its feature size. Using domain decomposition, the total number of unknowns can be greatly reduced and simulation efficiency can be accelerated, especially when modeling multi-scale structures. The equivalent circuit based 3-D FDFD method requires conformal grids at interfaces as described in CHAPTER 6 to approximate derivatives in space. The electrical fields on the interfaces are related to two domains and can only be derived in equations with conformal mesh grids on the interfaces using the finite-difference scheme. Therefore, using different mesh grids in each domain which results in non-conformal grids at the interface between domains can be a difficult problem to solve using the FDFD method.

In the past, several finite-element based non-conformal domain decomposition methods have been presented for solving electromagnetic problems [63, 64], DC voltage drop and thermal problems [65, 66]. A finite-difference domain decomposition using characteristic basis functions for solving electrostatic problems has been proposed in [67]. However, there is no previous work on non-conformal domain decomposition of the SEEC based

frequency domain solver, which can generate a susceptance element equivalent circuit model which can then be combined with multi-point model order reduction technique [56]. This chapter proposes a 3-D Finite-Difference Frequency-Domain (FDFD) non-conformal domain decomposition method [68]. The non-conformal domain decomposition approach allows non-matching grids between neighboring domains, which enables modeling of individual subdomains independently using different mesh grids based on the feature size. Field continuity at interfaces between domains is enforced by introducing Lagrange multipliers and vector basis functions at the interfaces. The domain decomposition method is first applied to model RDL traces on silicon interposers. Later, the formulation for incorporating a multiport network into non-conformal domain decomposition is presented to include the parasitic effects of TSV arrays into the system matrix. The efficiency and advantages using the proposed method is demonstrated by simulating interconnections in silicon interposers [69].

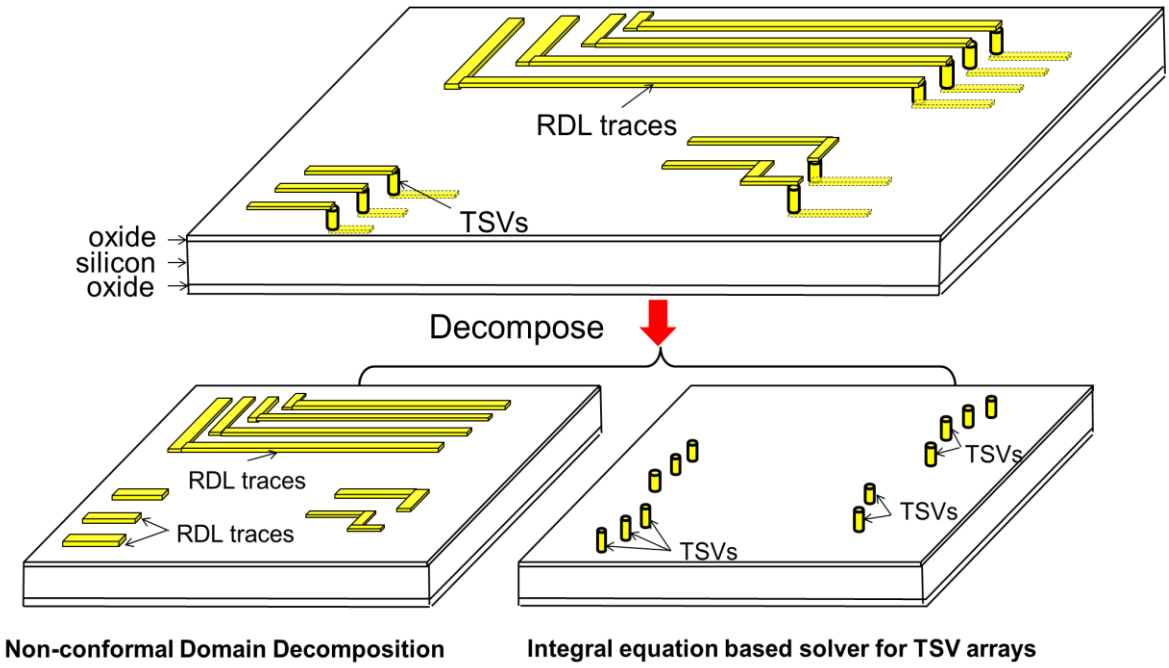


Figure 74. Decomposition of the interconnect problem into two problems

7.2 Modeling of Interconnections in Silicon Interposer

A silicon interposer with RDL traces and TSVs is shown in Figure 74. The RDL traces above the silicon substrate are routed with different densities in different areas. The interconnect problem is decomposed into two problems and can be modeled in three steps: 1) Modeling of RDL traces on the silicon interposer using non-conformal domain decomposition, 2) Modeling of TSV arrays, and 3) Incorporation of TSVs into non-conformal FDFD method.

7.2.1 3-D FDFD Non-conformal Domain Decomposition

In this section, 3-D FDFD based non-conformal domain decomposition is presented and utilized to model multiple RDL traces on a silicon interposer. The FDFD formulation for a single domain is presented in Chapter 6. For a single domain, the system matrix can be obtained as in equation (55) as presented in Chapter 6.

$$(\mathbf{G} + s\mathbf{C} + \frac{\mathbf{\Lambda}}{s})\mathbf{E} = \mathbf{KI} \tag{55}$$

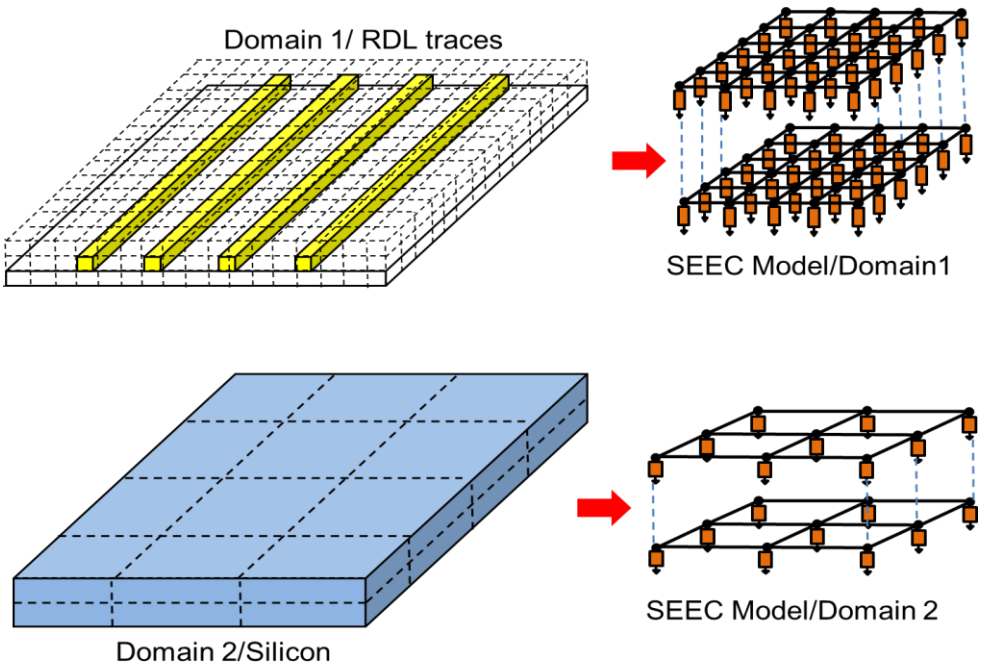


Figure 75. Two domains with non-matching grids at interfaces

A silicon interposer with multiple RDL trace routing is shown in Figure 75. Because of the feature scale difference between the metal layer, the oxide layer, and the silicon substrate, the silicon interposer can be divided into separate subdomains including the metal/oxide layer and silicon substrate. The metal/oxide domain and silicon substrate domain can be meshed independently using different mesh grids. Thus, the meshing grids from the metal/oxide layer do not overlap with grids from the silicon substrate domain and therefore the required meshing cells are greatly reduced.

At the interface, the continuity of electric field and magnetic field need to be maintained. For two subdomains with a common interface, by assuming $\lambda^k = j\omega\mu J_z\big|_{\Gamma_{inter}}$, where λ^k denotes a function from Lagrange multiplier space, we have the relationship of $-\lambda^{(1)} = \lambda^{(2)} = \lambda$ [70], where the weak continuity across the interface can be established and the following equations for domains and interface can be derived:

$$(\mathbf{G}^i + s\mathbf{C}^i + \frac{\mathbf{\Gamma}^i}{s})\mathbf{E}^i - \boldsymbol{\lambda}^i = \mathbf{K}^i\mathbf{I}^i \tag{56}$$

$$(\mathbf{G}^j + s\mathbf{C}^j + \frac{\mathbf{\Gamma}^j}{s})\mathbf{E}^j - \boldsymbol{\lambda}^j = \mathbf{K}^j\mathbf{I}^j \tag{57}$$

$$\int_{\Gamma_{inter}} (E^i - E^j)\varphi dl = 0 \tag{58}$$

where E^k is the field in domain k and φ is the basis function for the Lagrange multiplier. Because of the point-wise FDFD formulation in equation (56) and equation (57), a continuous representation of the E field and φ are required to compute the integral equation. In addition, the divergence condition $\nabla\cdot(\varepsilon E) = 0$ in source-free regions needs to be satisfied. Therefore, vector basis functions are introduced [71] for representing the E fields at the interfaces, which are used as shown in Figure 76 and expressed as:

$$N_1 = \frac{1}{\Delta y}(y_c + \frac{\Delta y}{2} - y)\hat{x} \tag{59}$$

$$N_2 = \frac{1}{\Delta y}(y - y_c + \frac{\Delta y}{2})\hat{x} \tag{60}$$

$$N_3 = \frac{1}{\Delta x}(x_c + \frac{\Delta x}{2} - x)\hat{y} \tag{61}$$

$$N_4 = \frac{1}{\Delta x}(x - x_c + \frac{\Delta x}{2})\hat{y} \tag{62}$$

The electric fields on each rectangular element can be expressed as the combination of the vector basis functions $E^e = \sum_{i=1}^{4} E_i N_i$. The Lagrange multiplier on each rectangular element can also be expressed as the combination of the vector basis functions $\lambda^e = \sum_{i=1}^{4} b_i \varphi_i$, where φ_i is the vector basis function defined in equation (63)-(66).

$$\varphi_1 = \frac{1}{\Delta y}(y_c + \frac{\Delta y}{2} - y)\hat{x} \tag{63}$$

$$\varphi_2 = \frac{1}{\Delta y}(y - y_c + \frac{\Delta y}{2})\hat{x} \tag{64}$$

$$\varphi_3 = \frac{1}{\Delta x}(x_c + \frac{\Delta x}{2} - x)\hat{y} \tag{65}$$

$$\varphi_4 = \frac{1}{\Delta x}(x - x_c + \frac{\Delta x}{2})\hat{y} \tag{66}$$

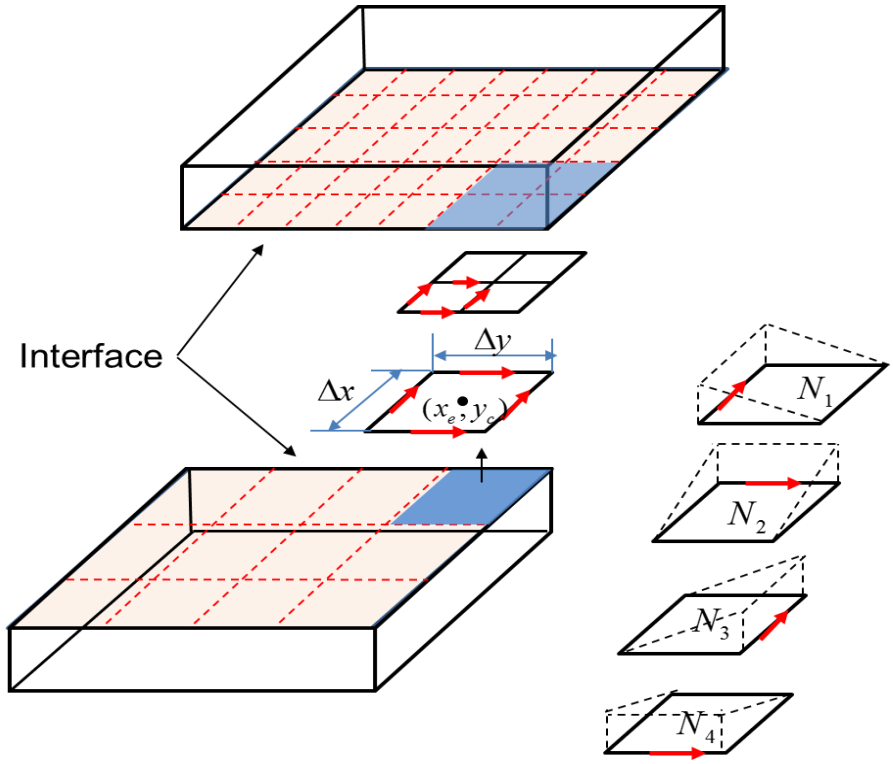


Figure 76. Vector basis functions for the E fields at the interfaces.

As a result, the field and the Lagrange multiplier on the interface can be expressed as $E = \sum_{i=1}^{\text{inter}} E_i^e$ and $\lambda = \sum_{i=1}^{\text{inter}} \lambda_1^e$, respectively. By multiplying both sides of equation (56) and equation (57), integrating over the interface and after some mathematical manipulations, the following equations can be obtained:

$$(\mathbf{G}^1 + s\mathbf{C}^1 + \frac{\mathbf{\Lambda}^1}{s})\mathbf{E}^1 - \frac{1}{\Delta x_1 \Delta y_1 \Delta z_1} \sum_{i=1}^{\text{inter\_1}} \int_{\Gamma_{\text{inter\_1}}} b_i \varphi_i N_j = \mathbf{K}^1 \mathbf{I}^1 \tag{67}$$

$$(\mathbf{G}^2 + s\mathbf{C}^2 + \frac{\mathbf{\Lambda}^2}{s})\mathbf{E}^2 - \frac{1}{\Delta x_2 \Delta y_2 \Delta z_2} \sum_{i=1}^{\text{inter\_2}} \int_{\Gamma_{\text{inter\_2}}} b_i \varphi_i N_j = \mathbf{K}^2 \mathbf{I}^2 \tag{68}$$

Equation (69) can be derived from equations (58), (67), (68) for the 3-D problem with two domains.

$$\begin{bmatrix} \mathbf{G}^1 + s\mathbf{C}^1 + \dfrac{\mathbf{\Gamma}^1}{s} & & \alpha^1\mathbf{B}^1 \\ & \mathbf{G}^2 + s\mathbf{C}^2 + \dfrac{\mathbf{\Gamma}^2}{s} & -\alpha^2\mathbf{B}^2 \\ \mathbf{B}^1 & -\mathbf{B}^2 & 0 \end{bmatrix} \begin{bmatrix} \mathbf{E}^1 \\ \mathbf{E}^2 \\ \mathbf{b} \end{bmatrix} = \begin{bmatrix} \mathbf{K}^1\mathbf{I}^1 \\ \mathbf{K}^2\mathbf{I}^2 \\ 0 \end{bmatrix} \tag{69}$$

where $\alpha^1 = 1/\Delta x_1 \Delta y_1 \Delta z_1$ and $\alpha^2 = 1/\Delta x_2 \Delta y_2 \Delta z_2$ are scaling factors to maintain the conservation of charge at interfaces. $\mathbf{K}^1\mathbf{I}^1$ and $\mathbf{K}^2\mathbf{I}^2$ are excitation vectors associated with port excitations in domain 1 and domain 2, respectively.

To observe the field continuity between two domains, a test case with two domains is simulated as shown in Figure 77. Each domain is meshed independently with mesh ratio 2:1 at interface. The E_x, E_y E_z fields distribution in two domains are shown in Figure 78. It can be seen from that the E field is continuous between two domains with non-matching grids.

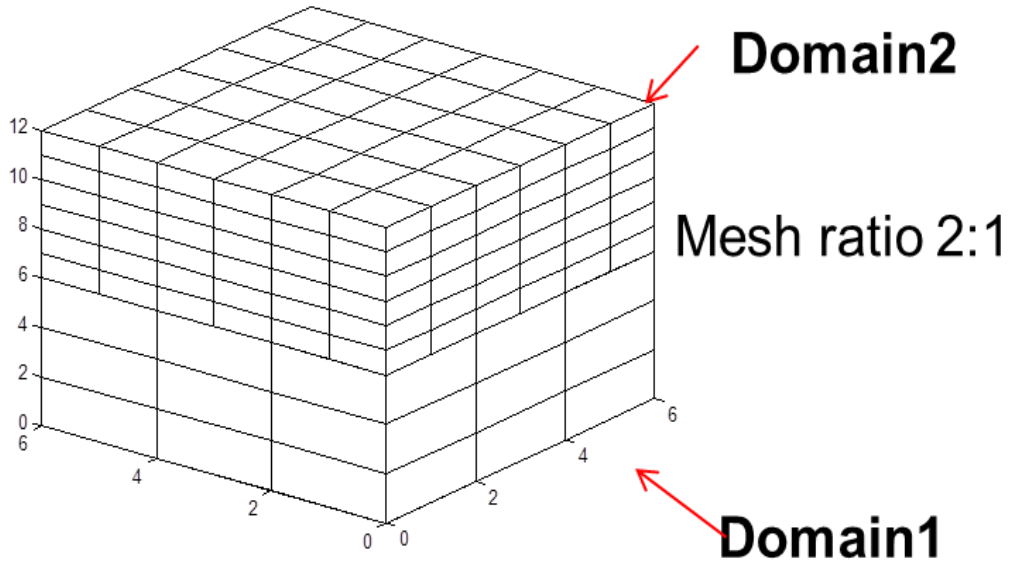
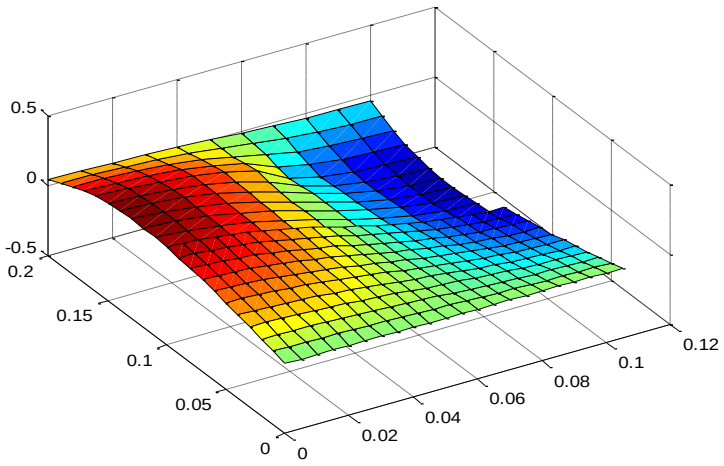
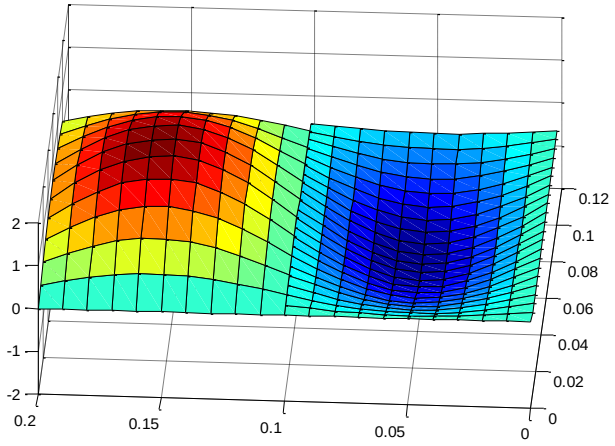


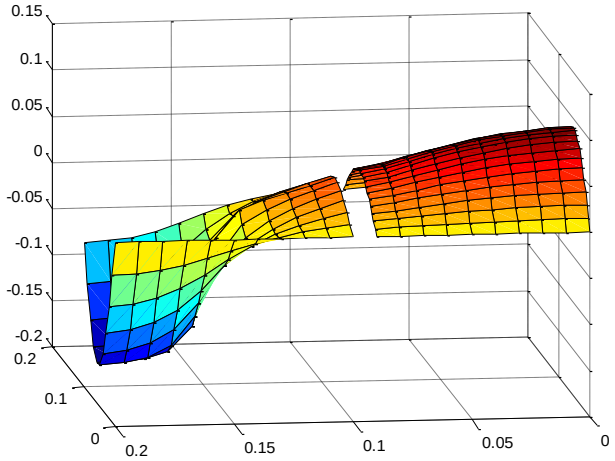
Figure 77. Two domains with non-matching grid at interface.



(a)



(b)



(c)

Figure 78. (a) Tangential Ex field distribution, (b) Tangential Ey field distribution, (c) Normal Ez field distribution.

For an integrated system, which is divided into subdomains, the generalized system equation can be written as:

$$\begin{bmatrix} \mathbf{A}^1 & & & & \alpha^1\mathbf{B}^1 \\ & \mathbf{A}^2 & & & \alpha^2\mathbf{B}^2 \\ & & \ddots & & \vdots \\ & & & \mathbf{A}^n & \alpha^n\mathbf{B}^n \\ \mathbf{B}^1 & \mathbf{B}^2 & \cdots & \mathbf{B}^n & \end{bmatrix} \begin{bmatrix} \mathbf{E}^1 \\ \mathbf{E}^2 \\ \vdots \\ \mathbf{E}^n \\ \mathbf{b} \end{bmatrix} = \begin{bmatrix} \mathbf{K}^1\mathbf{I}^1 \\ \mathbf{K}^2\mathbf{I}^2 \\ \vdots \\ \mathbf{K}^n\mathbf{I}^n \\ 0 \end{bmatrix} \tag{70}$$

where $\mathbf{A}^k = \mathbf{G}^k + s\mathbf{C}^k + \frac{\mathbf{\Lambda}^k}{s}$ denotes the susceptance element equivalent circuit model [55] in each domain.

7.2.2 Incorporating TSVs into Non-conformal Domain Decomposition

The cylindrical TSV structure requires a large number of mesh elements to approximate due to the rectangular grid in FDFD. Therefore, TSV arrays are modeled separately using the integral equation based solver and the response is incorporated into the non-conformal DDM as a multiport network. The formulation for incorporating multiport a network into non-conformal DDM is extended from CHAPTER 6. As a result, the system-level response of the silicon interposer with RDL traces and TSVs can be obtained. The TSV-to-RDL coupling is negligible when the ratio of TSV length to TSV diameter is larger than 5. Therefore the coupling between TSV and RDL traces has been neglected in this paper. This section presents details on incorporating multiport network across multiple domains, as shown in Figure 79.

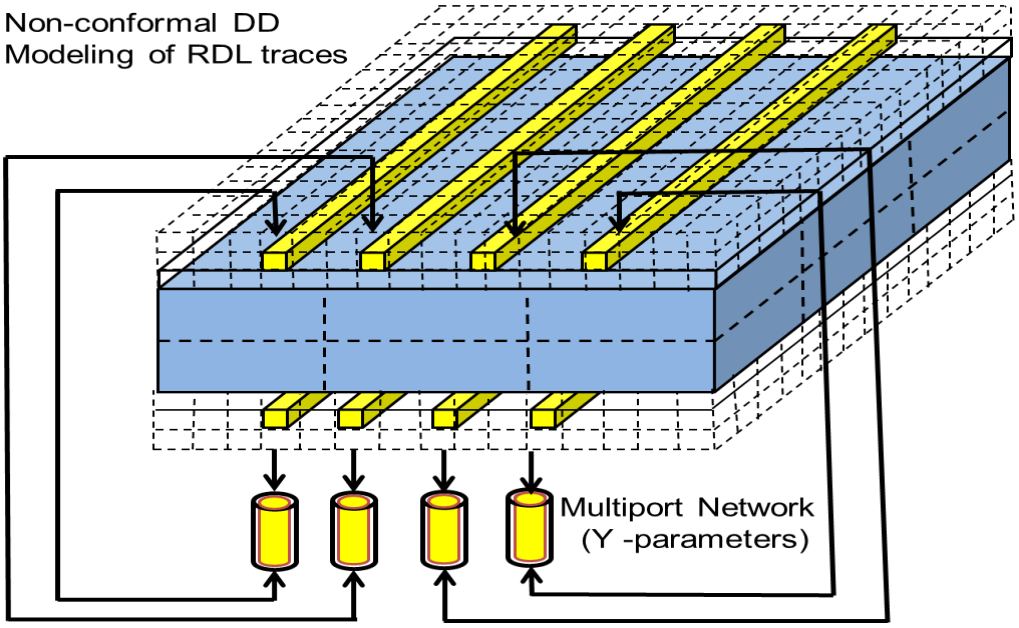


Figure 79. Incorporating multiport network into non-conformal domain decomposition.

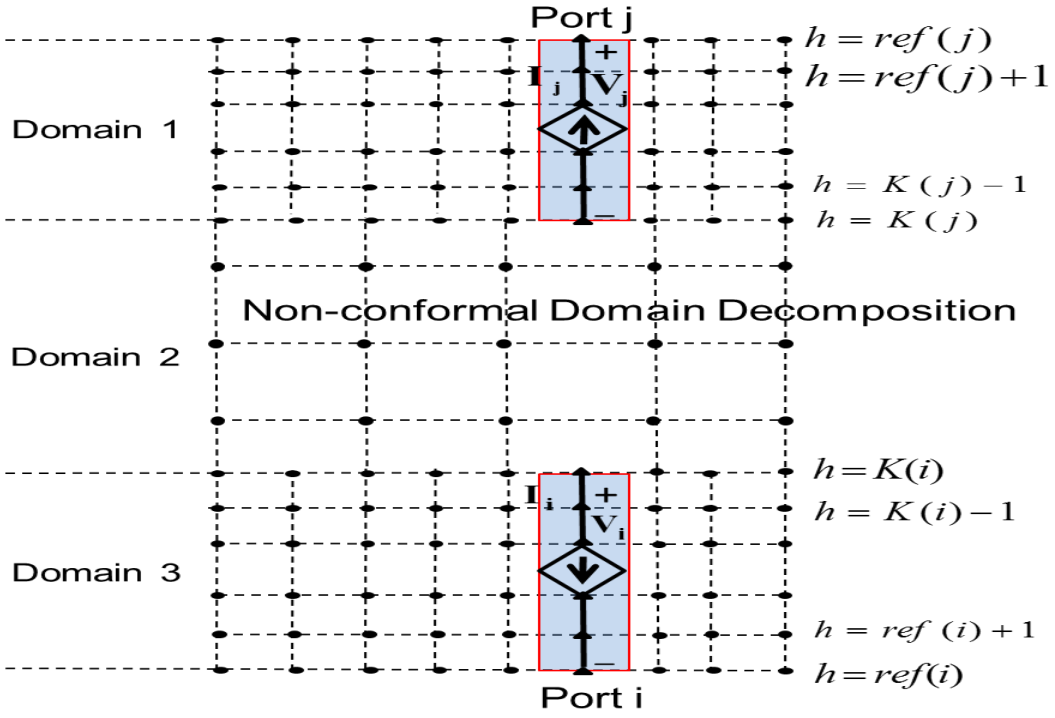


Figure 80. Cross-sectional view of ports in different domains. Ports representing current sources occupy several FDFD grids.

For simplicity, we consider a multiport network that crosses three domains, as shown in Figure 80, where the ports are in domain 1 and domain 3. Therefore, the multiport

network can be described using the current and voltage relation according to the following equation:

$$I_i(V_1, V_2 \cdots V_N) = \sum_{k=1}^{N_1} Y_{ik} V_k + \sum_{k=1}^{N_3} Y_{ik} V_k \qquad i = 1 \sim N \tag{71}$$

where index i represents the port index of the multiport network and N_1, N_3 represents the total number of ports in domain 1 and domain 3, respectively. Each port of the multiport network may be in different domains and occupy multiple grids in the Yee grid, as shown in Figure 80, where port i is represented by a current source I_i flowing along the *h*-direction. In the Yee grid, the voltage V_k can be written in terms of the *h*- component of electric field E_h as:

$$V_k = \sum_{h=ref}^{k} E_h \Delta h \tag{72}$$

where ref represents the voltage reference node in the Yee grid. After substituting equation (72) into equation (71), the current source I_i expressed as current density can be obtained as:

$$J_i(V_1 \cdots V_N) = \frac{I_i(V_1 \cdots V_N)}{Area} = \sum_{k=1}^{N_1} Y_{ik} \sum_{h=ref}^{k} \frac{E_h \Delta h}{Area} + \sum_{k=1}^{N_3} Y_{ik} \sum_{h=ref}^{k} \frac{E_h \Delta h}{Area} \tag{73}$$

where $Area$ is the cross-sectional area of the Yee cell. At each port i of the multiport network, the equivalent current source $J_i(V_1 \cdots V_N)$ must be applied to all these FDFD nodes from the reference node $[ref(i)]$ to the port definition node $[K(i)]$ along the *h*-direction in the Yee grid in different domains, as shown in Figure 80. This can be described by the matrix operation expressed in Figure 81, where $\mathbf{A_{sys}}$ is the overall system matrix after the multiport network is incorporated, P_1, P_2, P_3 is the total number of unknowns in domain 1, domain 2, domain 3, respectively. $[ref(i)+m]$, $[K(i)-n]$ represents the column (row) number of the matrix where the current density

J_i must be stamped and N_1, N_3 is the total number of ports in domain 1 and domain 3, respectively.

$$\begin{bmatrix} \mathbf{A}^1_{P_1\times P_1} & & & \alpha^1\mathbf{B}^1 \\ & \mathbf{A}^2_{P_2\times P_2} & & \alpha^2\mathbf{B}^2 \\ & & \mathbf{A}^3_{P_3\times P_3} & \alpha^3\mathbf{B}^3 \\ \mathbf{B}^1 & \mathbf{B}^2 & \mathbf{B}^3 & \end{bmatrix} + \sum_{i=1}^{N_1} \begin{matrix} \\ [\mathrm{ref(i)}]\rightarrow \\ \vdots \\ [\mathrm{ref(i)+m}]\rightarrow \\ \vdots \\ [\mathrm{K(i)-n}]\rightarrow \\ \vdots \\ [\mathrm{K(i)}]\rightarrow \end{matrix} \begin{matrix} [\mathrm{ref(i)}] & \cdots & [\mathrm{ref(i)+m}] & \cdots & [\mathrm{K(i)-n}] & \cdots & [\mathrm{K(i)}] \\ \downarrow & & \downarrow & & \downarrow & & \downarrow \\ J_i & \cdots & J_i & \cdots & J_i & \cdots & J_i \\ \vdots & & \vdots & & \vdots & & \vdots \\ J_i & \cdots & J_i & \cdots & J_i & \cdots & J_i \\ \vdots & & \vdots & & \vdots & & \vdots \\ J_i & \cdots & J_i & \cdots & J_i & \cdots & J_i \\ \vdots & & \vdots & & \vdots & & \vdots \\ J_i & \cdots & J_i & \cdots & J_i & \cdots & J_i \end{matrix}_{P_1\times P_1} + \sum_{j=1}^{N_3} \begin{matrix} \\ [\mathrm{ref(j)}]\rightarrow \\ \vdots \\ [\mathrm{ref(j)+m}]\rightarrow \\ \vdots \\ [\mathrm{K(j)-n}]\rightarrow \\ \vdots \\ [\mathrm{K(j)}]\rightarrow \end{matrix} \begin{matrix} [\mathrm{ref(j)}] & \cdots & [\mathrm{ref(j)+m}] & \cdots & [\mathrm{K(j)-n}] & \cdots & [\mathrm{K(j)}] \\ \downarrow & & \downarrow & & \downarrow & & \downarrow \\ J_i & \cdots & J_i & \cdots & J_i & \cdots & J_i \\ \vdots & & \vdots & & \vdots & & \vdots \\ J_i & \cdots & J_i & \cdots & J_i & \cdots & J_i \\ \vdots & & \vdots & & \vdots & & \vdots \\ J_i & \cdots & J_i & \cdots & J_i & \cdots & J_i \\ \vdots & & \vdots & & \vdots & & \vdots \\ J_i & \cdots & J_i & \cdots & J_i & \cdots & J_i \end{matrix}_{P_3\times P_3} = \mathbf{A}_{\mathrm{sys}}$$

Figure 81. Matrix operation for incorporating multiport network into FDFD non-conformal domain decomposition.

7.3 System Matrix Solver

This section describes the details on applying the non-conformal domain decomposition method for modeling RDL traces on a silicon interposer and approaches used to solve the system matrix after TSVs are incorporated.

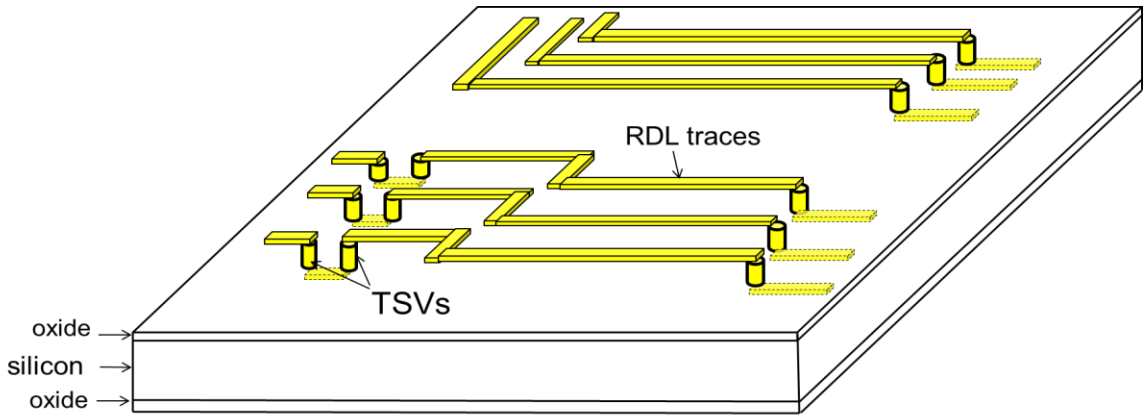


Figure 82. RDL traces and TSVs in silicon interposer.

The RDL traces and TSV transition structure is shown in Figure 82. Because of the feature scale difference between the metal/oxide layer and the silicon substrate, the interposer can be divided vertically into subdomains with different mesh grid sizes. For a

silicon interposer with an irregular RDL density, domains can also be divided along the $x-$ and $y-$ directions to reduce the total number of unknowns, as shown in Figure 83.

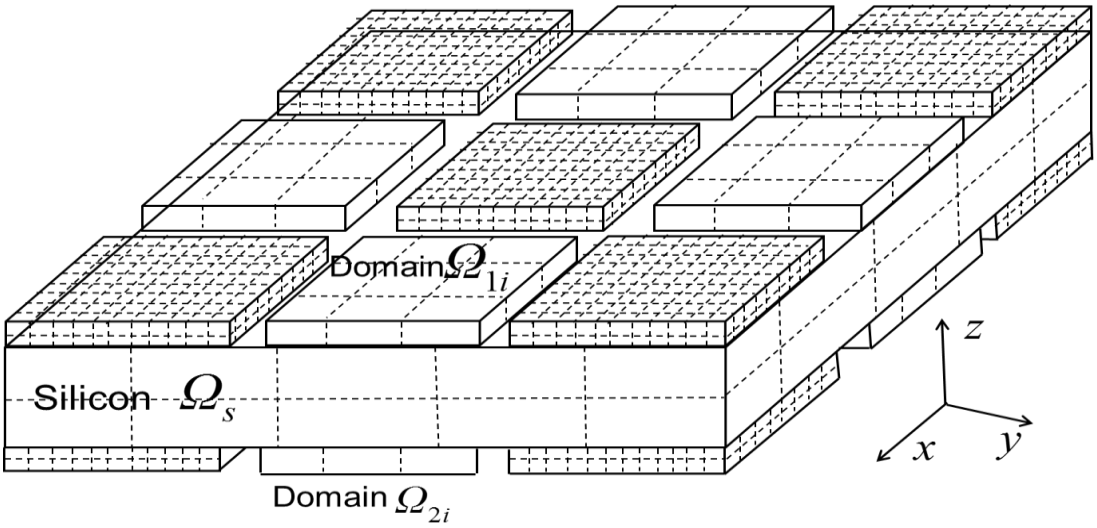


Figure 83. Silicon interposer divided into subdomains in $x-$, $y-$, $z-$direction.

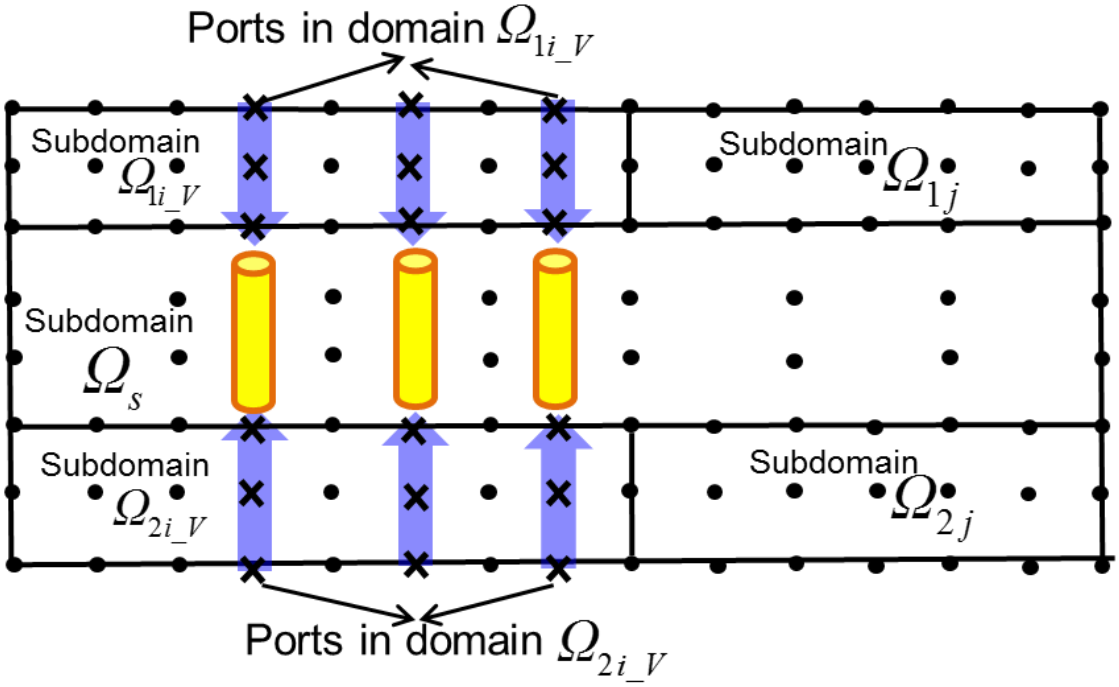


Figure 84. Cross-sectional view of subdomains with TSVs in the DDM. X-shaped dots represents ports of TSVs stamped.

As shown in Figure 84, there are two types of subdomains after domain partitioning: subdomains without current density representing the ports of TSVs stamped (denoted

as Ω_{1i}/Ω_{2i}) and subdomains with current density representing the ports of TSVs stamped (denoted as $\Omega_{1i\_v}/\Omega_{2i\_v}$), where there will be coupling between subdomains Ω_{1i_v} and Ω_{2i_v} due to the coupling between TSVs. The coupling is induced by the unknowns in the nodes, where the current density has been applied. To utilize parallel computing to solve subdomains simultaneously, there should be no coupling between subdomains. Therefore, subdomains with ports of TSV array stamped are grouped into one subdomain for parallel computing (for example, subdomain Ω_{1i_v} and subdomain Ω_{2i_v} are grouped into one subdomain). As a result, the system matrix can be reordered as:

$$\begin{bmatrix} \mathbf{A}_{11} & & & & & & & & \mathbf{B}_{11} \\ & \mathbf{A}_{21} & & & & & & & \mathbf{B}_{21} \\ & & \ddots & & & & & & \vdots \\ & & & \mathbf{A}_{1i\_v} & & & & & \mathbf{B}_{1i\_v} \\ & & & & \mathbf{A}_{2i\_v} & & & & \mathbf{B}_{2i\_v} \\ & & & & & \ddots & & & \vdots \\ & & & & & & \mathbf{A}_{1M} & & \mathbf{B}_{1M} \\ & & & & & & & \mathbf{A}_{2M} & \mathbf{B}_{2M} \\ \mathbf{B}_{11}^T & \mathbf{B}_{21}^T & \cdots & \mathbf{B}_{1i\_v}^T & \mathbf{B}_{2i\_v}^T & & \mathbf{B}_{1M}^T & \mathbf{B}_{2M}^T & \end{bmatrix} \begin{bmatrix} \mathbf{e}_{11} \\ \mathbf{e}_{21} \\ \vdots \\ \mathbf{e}_{1i\_v} \\ \mathbf{e}_{2i\_v} \\ \vdots \\ \mathbf{e}_{1M} \\ \mathbf{e}_{2M} \\ \mathbf{e}_{\Gamma} \end{bmatrix} = \begin{bmatrix} \mathbf{k}_{11} \\ \mathbf{k}_{21} \\ \vdots \\ \mathbf{k}_{1i\_v} \\ \mathbf{k}_{2i\_v} \\ \vdots \\ \mathbf{k}_{1M} \\ \mathbf{k}_{2M} \\ 0 \end{bmatrix} \tag{74}$$

where $\mathbf{A}_{1i}/\mathbf{A}_{2i}$ and $\mathbf{A}_{1i\_v}/\mathbf{A}_{2i\_v}$ is the matrix corresponding to subdomain Ω_{1i}/Ω_{2i} or $\Omega_{1i\_v}/\Omega_{2i\_v}$.The vector $\mathbf{e}_{11},\mathbf{e}_{21}\ldots\mathbf{e}_{1M},\mathbf{e}_{2M}$ represents the field unknowns of subdomains. The Schur complement system [22], [23] is given by

$$\mathbf{S}\mathbf{e}_{\Gamma} = \mathbf{g} \tag{75}$$

where

$\mathbf{S} = -\sum_{i=1}^{M-M_v} \mathbf{B}_{1(2)i}^T \mathbf{A}_{1(2)i}^{-1} \mathbf{B}_{1(2)i} - \sum_{i=1}^{M_v} \begin{bmatrix} \mathbf{B}_{1i\_v}^T & \mathbf{B}_{2i\_v}^T \end{bmatrix} \begin{bmatrix} \mathbf{A}_{1i\_v} & \\ & \mathbf{A}_{1i\_v} \end{bmatrix}^{-1} \begin{bmatrix} \mathbf{B}_{1i\_v} \\ \mathbf{B}_{2i\_v} \end{bmatrix}$ and

$\mathbf{g} = -\sum_{i=1}^{M-M_v} \mathbf{B}_{1(2)i}^T \mathbf{A}_{1(2)i}^{-1} \mathbf{k}_{1(2)i} - \sum_{i=1}^{M_v} \begin{bmatrix} \mathbf{B}_{1(2)i}^T & \mathbf{B}_{1(2)i}^T \end{bmatrix} \begin{bmatrix} \mathbf{A}_{1i\_v} & \\ & \mathbf{A}_{1i\_v} \end{bmatrix}^{-1} \begin{bmatrix} \mathbf{B}_{1i\_v} \\ \mathbf{B}_{2i\_v} \end{bmatrix}$. It can be seen that the subdomains $\mathbf{A}_{1i}, \mathbf{A}_{2i}$ and $\begin{bmatrix} \mathbf{A}_{1i\_v} & \\ & \mathbf{A}_{2i\_v} \end{bmatrix}$ are independent of each other, so that

each term $\mathbf{B}_{1(2)i}^{T}\mathbf{A}_{1(2)i}^{-1}\mathbf{B}_{1(2)i}$ or$[\mathbf{B}_{1i_v}^{T} \quad \mathbf{B}_{2i_v}^{T}]\begin{bmatrix}\mathbf{A}_{1i_v} & \\ & \mathbf{A}_{1i_v}\end{bmatrix}^{-1}\begin{bmatrix}\mathbf{B}_{1i_v}\\ \mathbf{B}_{2i_v}\end{bmatrix}$ in the summation can be calculated simultaneously in a parallel manner. Once the Schur complement has been solved, equation (74) can be decoupled by solving the subdomain problem:

$$\mathbf{A}_{1(2)i}\mathbf{e}_{1(2)i}=\mathbf{g}_i \text{ or } \begin{bmatrix}\mathbf{A}_{1i\_v} & \\ & \mathbf{A}_{2i\_v}\end{bmatrix}\begin{bmatrix}\mathbf{e}_{1i\_v}\\ \mathbf{e}_{2i\_v}\end{bmatrix}=\mathbf{g}_i \tag{76}$$

where $\mathbf{g}_i=\mathbf{k}_i-\mathbf{B}_{i(i\_v)}\mathbf{e}_\Gamma$ or $\mathbf{g}_i=\begin{bmatrix}\mathbf{k}_{1i\_v}\\ \mathbf{k}_{2i\_v}\end{bmatrix}-\begin{bmatrix}\mathbf{B}_{1i\_v}\\ \mathbf{B}_{2i\_v}\end{bmatrix}\mathbf{e}_\Gamma$. The subdomain problems can be solved in parallel since the subdomains $\mathbf{A}_{1(2)i}$ and $\begin{bmatrix}\mathbf{A}_{1i\_v} & \\ & \mathbf{A}_{2i\_v}\end{bmatrix}$ are independent of each other. The flow that for applying DDM and solving the system matrix in Figure 82 can be summarized as follows.

(1) Partitioning the silicon interposer into three domains along $z-$ direction.

(2) Partitioning the metal/oxide layer into subdomains according to the RDL traces routing densities.

(3) Reordering the system matrix according to domains where TSVs are stamped.

(4) Using parallel computing to calculate the summation $\mathbf{S}=-\sum_{i=1}^{M-M_v}\mathbf{B}_{1(2)i}^{T}\mathbf{A}_{1(2)i}^{-1}\mathbf{B}_{1(2)i}-\sum_{i=1}^{M_v}[\mathbf{B}_{1i\_v}^{T} \quad \mathbf{B}_{2i\_v}^{T}]\begin{bmatrix}\mathbf{A}_{1i\_v} & \\ & \mathbf{A}_{1i\_v}\end{bmatrix}^{-1}\begin{bmatrix}\mathbf{B}_{1i\_v}\\ \mathbf{B}_{2i\_v}\end{bmatrix}$ and then obtaining the Schur complement matrix $\mathbf{S}$.

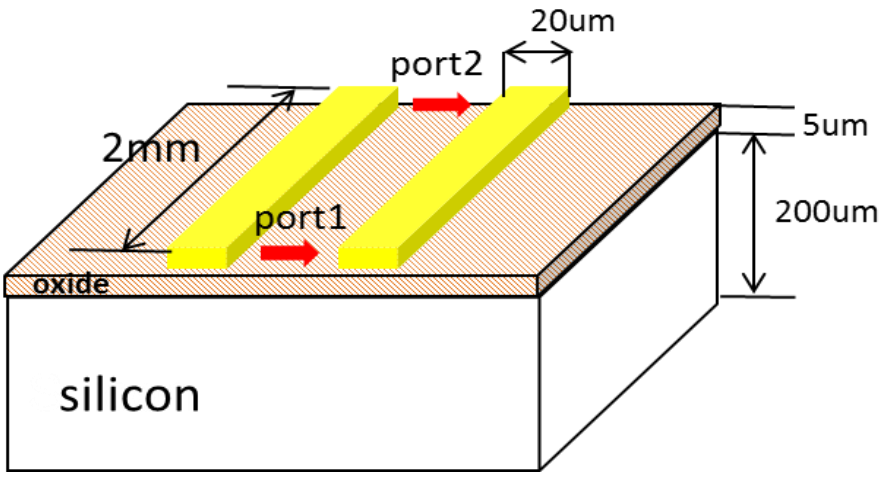
(5) Solving equation (75) for interface unknowns $\mathbf{e}_\Gamma$.

(6) Solving subdomains (76) simultaneously.

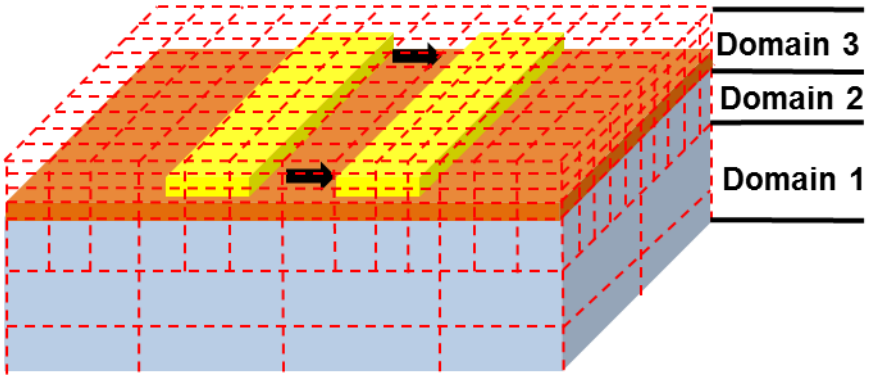
7.4 Numerical Examples

7.4.1 RDL traces on silicon interposers

The section applies the DDM method to model RDL traces on lossy silicon substrates. The first example with dimensions and port setup is shown in Figure 85(a). A $5\,\mu m$ thick silicon dioxide layer (with dielectric constant $\varepsilon_r = 3.9$) is on a $200\,\mu m$ thick silicon substrate (with dielectric constant $\varepsilon_r = 11.9$ and silicon conductivity $\sigma = 10 S/m$). The length, spacing and width of the RDL traces are $2\,mm$, $20\,\mu m$ and $20\,\mu m$, respectively. The entire structure is enclosed in a perfect electric conductor box with dimensions $400\mu m \times 2000\mu m \times 220\mu m$. To apply the non-conformal domain decomposition method, this structure is divided into 3 domains as shown in Figure 85(b). Since the oxide layer is thin and the width of RDL traces is narrow, we need to use fine mesh grids for the oxide and metal layers and coarse mesh grids can be used for the silicon substrate. Therefore, each domain is discretized using different cell sizes, the cell size for domain 1, domain 2 and domain 3 are $50\mu m \times 100\mu m \times 50\mu m$, $10\mu m \times 100\mu m \times 50\mu m$ and $10\mu m \times 100\mu m \times 5\mu m$, respectively. The S-parameters calculated using the non-conformal domain decomposition method are compared with the 3-D FDFD method (without DD) and CST Microwave Studio (MWS) [29]. As can be observed from Figure 86, the insertion loss and return loss data from non-conformal DD, FDFD and CST MWS show good correlation over a bandwidth of 20GHz. The total unknowns, computational time and memory consumption are reduced by $8\times$, $4\times$ and $3\times$ using non-conformal DD compared to FDFD, as shown in Table 5. All simulations were performed on a computer with two Intel 2.4-GHz CPUs with 48-GB memory.

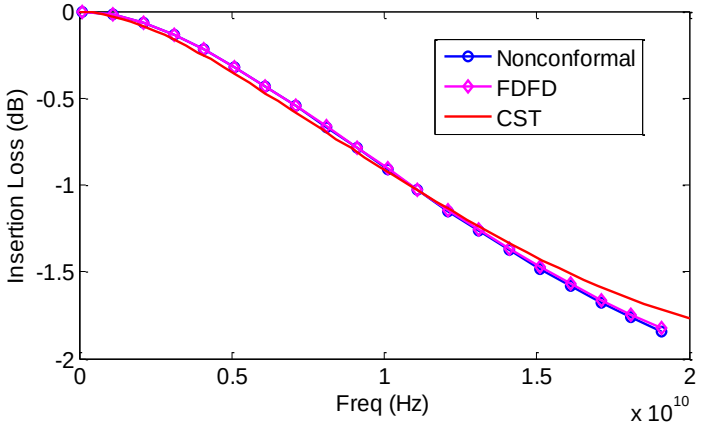


(a)

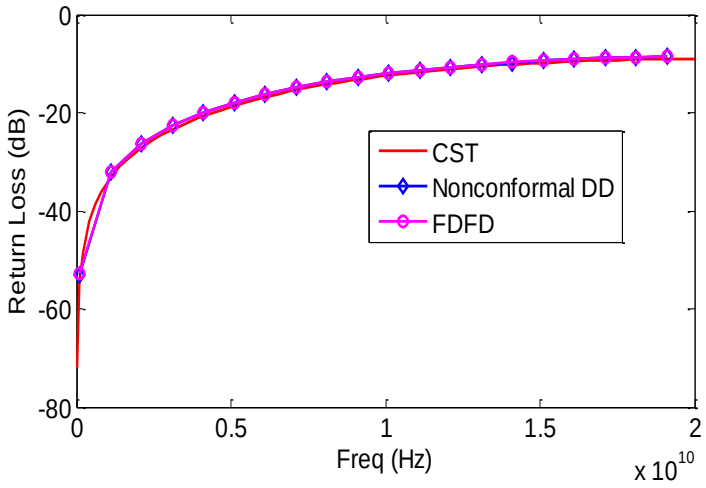


(b)

Figure 85. RDL transmission line pair, (a) Geometry, (b) Non-conformal DD.



(a)



(b)

Figure 86. S-parameters of RDL transmission line pair, (a) Insertion loss, (b) Return Loss.

Table 5 Comparison of non-conformal DD and FDFD

Example	Total unknowns / CPU time per freq. (sec) / memory (GB)	
	Non-conformal DD	FDFD
Case A:	13,080/~11s/1.4GB	108,000/~40s/5GB
Case B:	19,800/~18s/2GB	162,000/~49s/7GB

In the second example, multiple RDL transmission lines with port dimensions and port definition, as shown in Figure 87(a), is simulated. A $5\,\mu m$ thick silicon dioxide layer (with dielectric constant $\varepsilon_r = 3.9$) is on a $200\,\mu m$ thick silicon substrate (with dielectric constant $\varepsilon_r = 11.9$ and silicon conductivity $\sigma = 10 S/m$). The length and width of the RDL traces are $2\,mm$ and $20\,\mu m$, respectively. The entire structure is enclosed in a perfect electric conductor box with dimensions $600\mu m \times 2000\mu m \times 220\mu m$. Similar to the first example, this structure is divided into 3 domains as shown in Figure 87(b). Each domain is discretized using different cell sizes. The cell sizes for domain 1, domain 2 and domain 3 are $60\mu m \times 100\mu m \times 50\mu m$, $10\mu m \times 100\mu m \times 50\mu m$ and $10\mu m \times 100\mu m \times 5\mu m$, respectively. The S-parameters calculated using the non-conformal domain decomposition method are compared with the 3-D FDFD method (without DD) and CST MWS. As can be observed from Figure 88, the coupling and insertion loss data from non-conformal DD, FDFD and

CST MWS show good correlation over a bandwidth of 20GHz. The total unknowns, computational time and memory consumption is reduced by 8×, 3×and 3× using non-conformal DD compared to FDFD, as shown in Table 5.

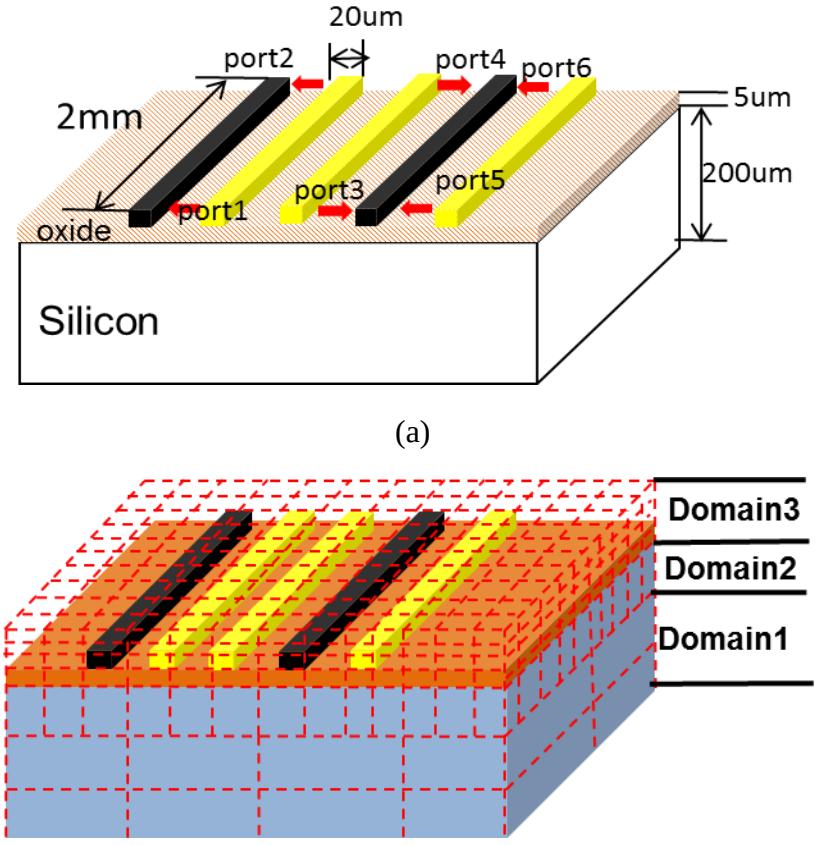
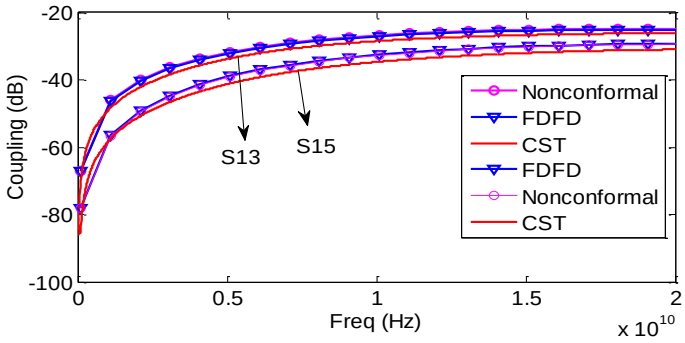
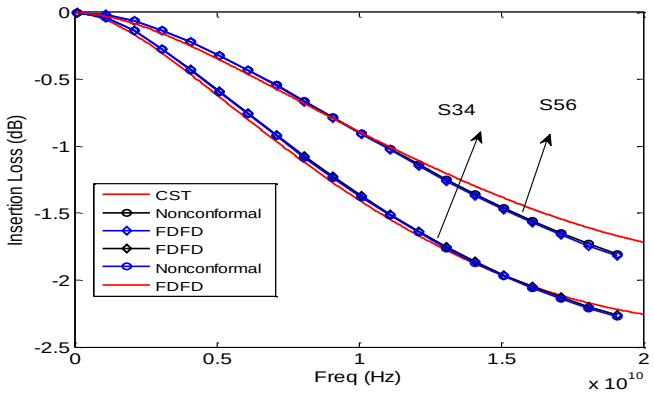


Figure 87. Multiple RDL traces, (a) Geometry (b) Non-conformal DD





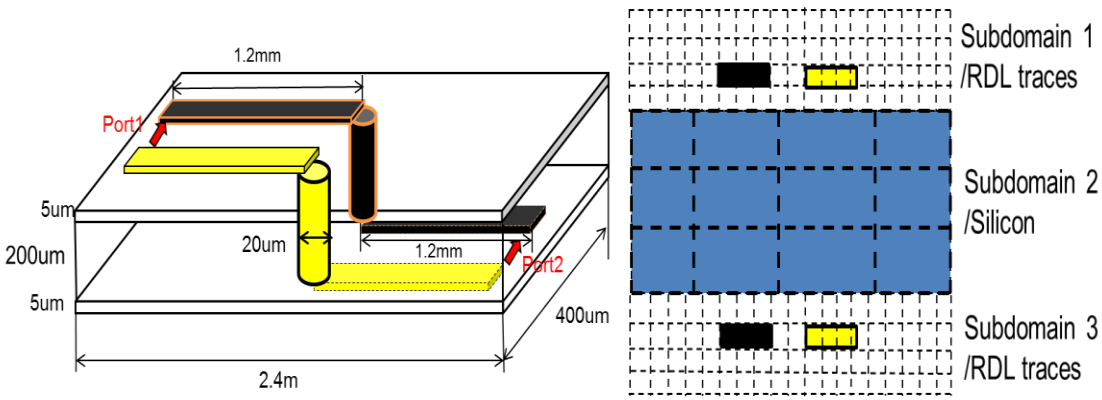
(b)

Figure 88. S-parameters of multiple RDL traces, (a) Geometry, (b) Non-conformal DD.

7.4.2 RDL Traces Connected to TSVs in Silicon Interposer

This section applies the proposed method to model several RDL-TSV-RDL transition structures in silicon interposer.

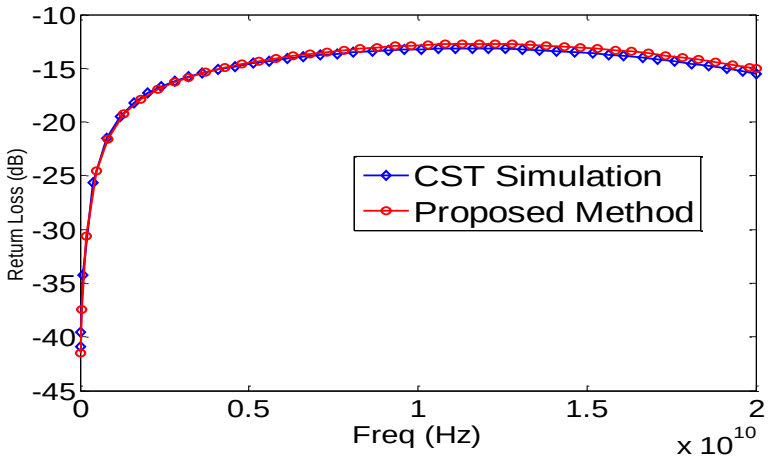
The first example with dimensions is shown in Figure 89. Two 5um thick silicon dioxide layers (with dielectric constant $\varepsilon_r = 4$) are on both sides of a 200um thick silicon substrate (with dielectric constant $\varepsilon_r = 11.9$ and silicon conductivity $\sigma = 10 S/m$). The length and width of the RDL trace is 2.3mm and 20um respectively. The length, radius and oxide liner thickness of the TSV is fixed at 200um, 15um and 1um respectively. This structure is divided vertically into three domains in the $z-$direction as shown in Figure 89(b). Since the coupling between domains is captured using Lagrange multipliers, each domain can be meshed independently. The cell sizes used to discretize each domain are $10um \times 50um \times 5um$, $50um \times 100um \times 40um$ and $10um \times 50um \times 5um$, respectively.



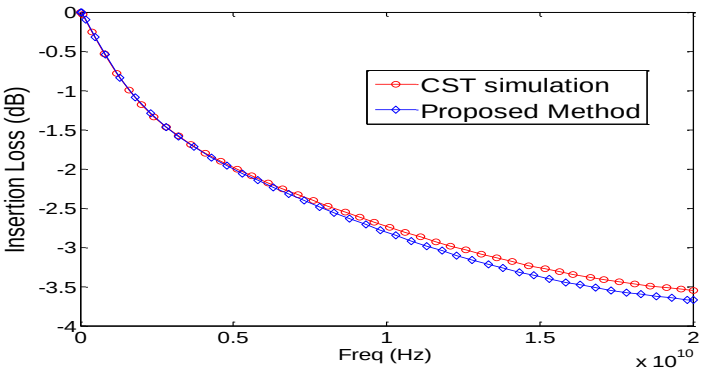
(a) (b)

Figure 89. RDL-TSV-RDL transition structure, (a) Geometry, (b) Cross-sectional view of non-conformal DDM.

The S-parameters calculated using the non-conformal domain decomposition method are compared with CST Microwave Studio (MWS). As can be seen from Figure 90, the insertion loss and return loss data for this transition structure from the proposed modeling approach and CST Microwave Studio shows good correlation over a bandwidth of 20GHz.



(a)



(b)

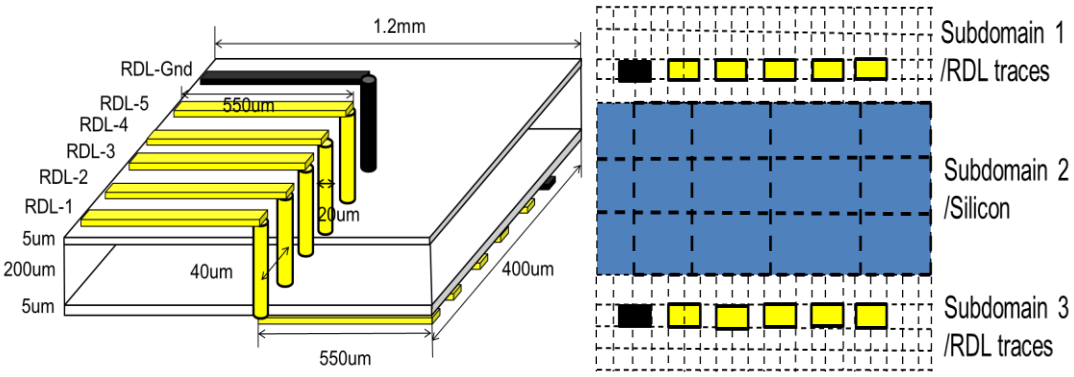
Figure 90. S-parameters of RDL-TSV-RDL transition structure, (a) return loss, (b) insertion loss.

In the second example, multiple RDL traces and TSV arrays are considered. The five RDL-TSV-RDL transition structure with dimensions is shown in Figure 91(a). The length, width and spacing of the multiple RDL traces are 1.2mm, 20um and 20um respectively. The length, radius, pitch and oxide thickness of the 5×1 TSV arrays are 200um, 10um, 40um and 1um respectively. Due to the scale difference between the metal/oxide layer and silicon substrate, this structure is divided vertically into three domains in the $z-$direction as shown Figure 91(b). Since RDL traces are straight lines, the metal/oxide layer is not divided in the $x-$and $y-$directions. Therefore, two interfaces are needed to capture the coupling between the metal/oxide layer and silicon substrate. In this example, the basis functions for the Lagrange multipliers for metal/oxide-silicon substrate interface are selected from the silicon substrate side. The cell sizes used to discretize each domain are $10um\times50um\times5um$, $50um\times50um\times40um$ and $10um\times50um\times5um$, respectively. The total number of unknowns using DDM is 74.9K. Compared with the FDFD method without using DDM which requires 299K unknowns, the number of unknowns is greatly reduced due to the non-conformal domain decomposition approach used. The computational time and memory consumption using DDM are compared with FDFD and CST simulation as shown in Table 6. All the

simulations were performed on a computer with two Intel 2.4 GHz 12-core processors with 48GB memory.

Table 6. Comparison of the proposed method, direct solver and CST.

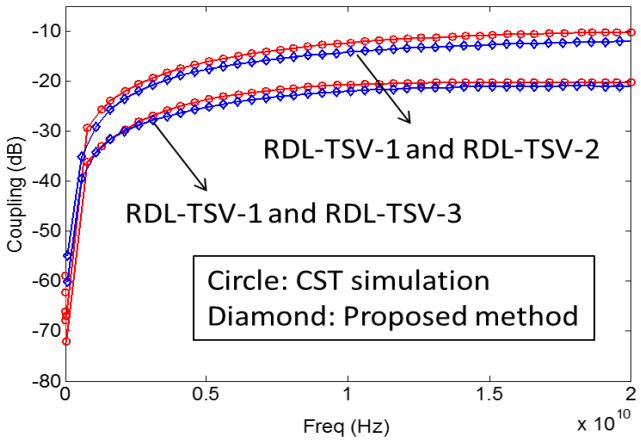
Example	CPU time per freq. (sec.) / memory (GB)		
	Conformal FDFD	CST	Proposed method
Case 2	~500s/20GB	~610s/6GB	~230s/3GB
Case 3	N/A	N/A	~700s/11GB



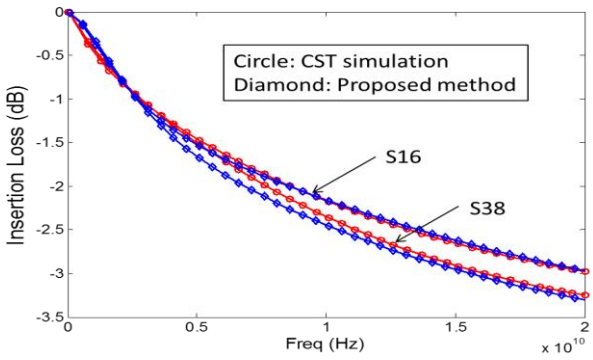
(a) (b)

Figure 91. Five RDL-TSV-RDL transition structure, (a) Geometry, (b) Cross-sectional view of non-conformal DDM.

The coupling between RDL-TSV-1 RDL-TSV-3 and RDL-TSV-3 are compared with CST simulations and show good correlation up to 20GHz as illustrated in Figure 92(a). The correlation indicates that the proposed method captures all the coupling effects of the TSV arrays and multiple RDL traces. The insertion loss illustrated in Figure 92(b) shows good correlation with CST simulations up to 20 GHz. It can be seen that the RDL-TSV-RDL transition in the middle (S38) shows larger insertion loss compared to the RDL-TSV-RDL transition at the edge (S16) due to the enhanced coupling in the middle.



(a)

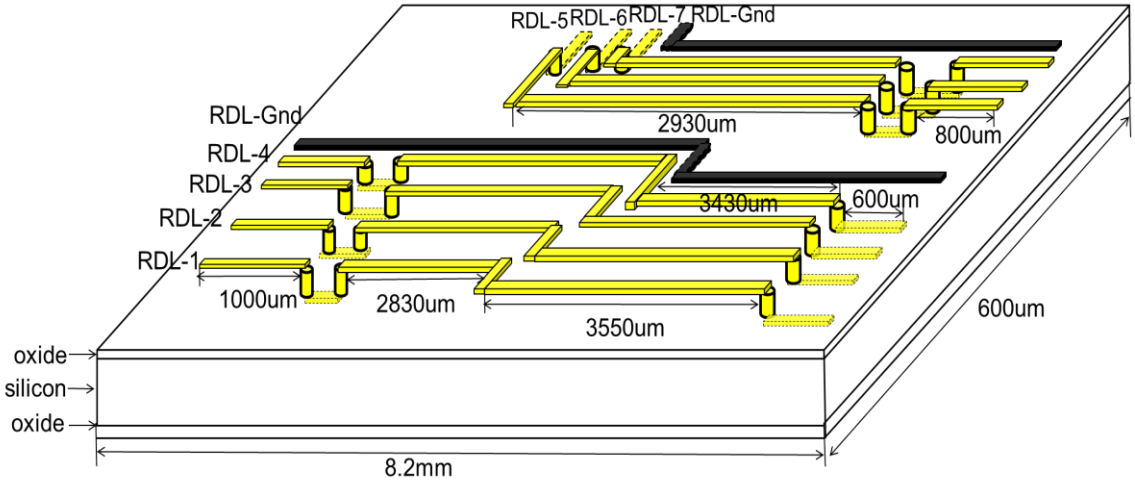


(b)

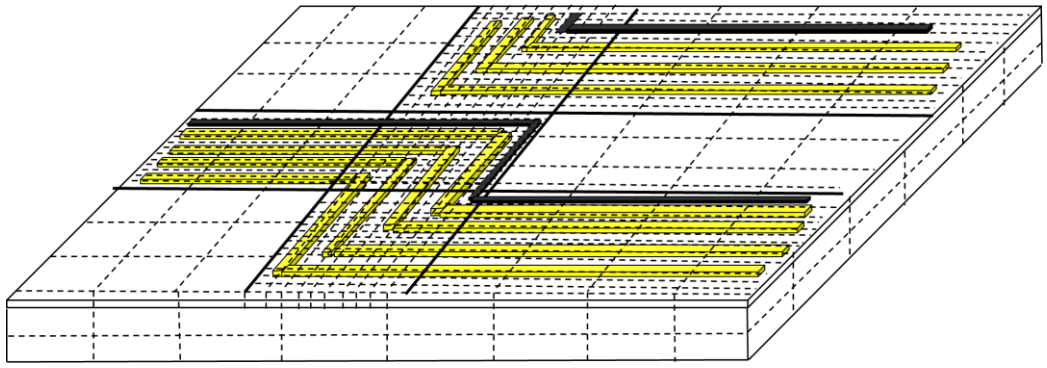
Figure 92. S-parameters of five RDL-TSV-RDL transition structure. (a) Coupling S12, S13, (b) Insertion loss S16 and S38.

This example considers a large silicon interposer with multiple long RDL traces with different routing densities. The silicon interposer with RDL and TSVs with dimensions is shown in Figure 93(a). There are four TSV arrays in this example. For the TSV arrays, the length, radius, pitch and oxide thickness of the TSV array are 200um, 10um, 40um and 1um respectively. This structure is first divided vertically into three domains along the $z-$direction. Since there are different routing densities of RDL traces, the metal layer is also divided along the $x-$and $y-$directions as shown in Figure 93(b). This results in a total number of 19 subdomains. Each subdomain can be meshed independently according

to the feature scale in each subdomain. Therefore, the required total meshed cells and unknowns are reduced dramatically as compared with conventional FDFD. For the initial mesh without domain decomposition, the FDFD required ~10 million unknowns and could not be solved due to memory limits. However, using the DDM, it required only 128K unknowns. The computational time and memory consumption using DDM are compared with FDFD and CST simulations as shown in Table 6.



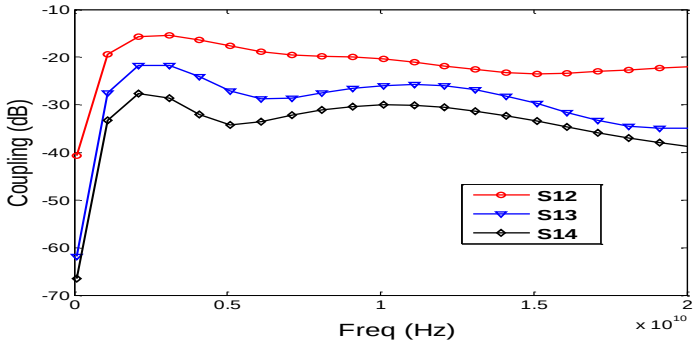
(a)



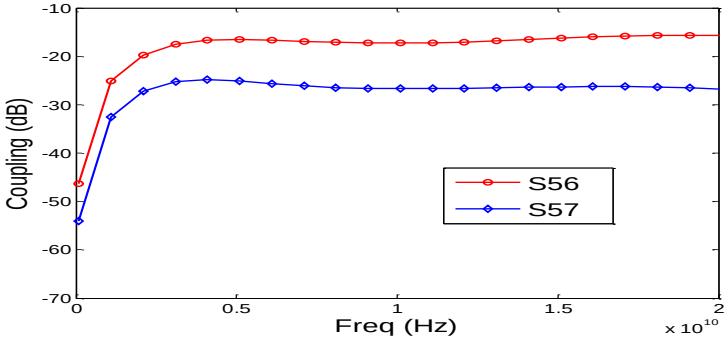
(b)

Figure 93. RDL traces with different routing density and multiple TSV arrays, (a) Geometry, (b) Non-conformal domain decomposition.

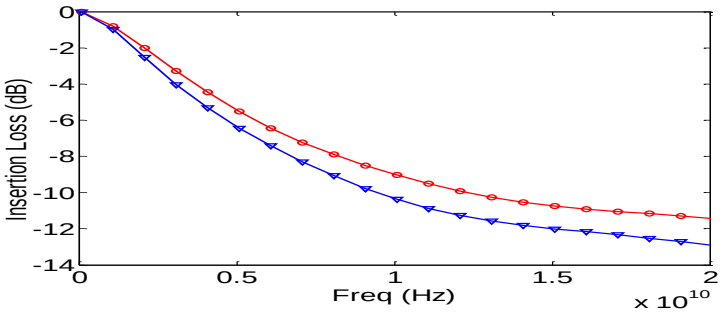
The insertion loss and coupling of this structure obtained from the proposed approach are shown in Figure 94. The insertion loss is very high since long lines are directly over silicon. CST was unable to simulate this structure due to memory limitations.



(a)



(b)



(c)

Figure 94. S-paramters of RDL traces with different routing densities and multiple TSV arrays, (a) Coupling between RDL-1, RDL-2, RDL-3 and RDL-4, (b) coupling between RDL-5, RDL-6, and RDL-7, (c) insertion loss.

7.5 Summary

This chapter presents the formulation of the 3-D FDFD based non-conformal domain decomposition method and is utilized to model the RDL traces with different routing

densities on silicon interposers. TSV arrays were modeled using an efficient integral equation based solver without meshing and later incorporated into the domain decomposition method. By using the non-conformal domain decomposition method, a complex system can be divided into several subdomains and each subdomain can be meshed independently, therefore, system unknowns can be greatly reduced. The total unknowns using non-conformal domain decomposition is reduced 4× in case 1 and case 2 due to the feature scale difference between RDL layer and silicon substrate compared to conformal FDFD method. Since RDL traces have different routing densities in case 3, the domains can be divided according to the RDL trace routing densities to further reduce the total unknowns. The total unknowns reduced will depend on the routing of RDL traces compared to the conformal FDFD method (In case 3, the total unknowns reduced ~40×). The efficiency and advantages using the proposed method were demonstrated by simulating interconnections in silicon interposers.

CHAPTER 8

FUTURE WORK

While the work in this dissertation focuses on modeling and simulation of silicon interposers for 3-D systems, it provides scope for future work in several aspects described as follows:

8.1 TSV-to-Wire Coupling

In the proposed modeling method for interconnections in silicon interposers, the responses of TSVs are stamped into the system matrix of RDL traces. The coupling between TSVs and RDL traces are not considered in the proposed modeling method. However, the TSV-to-wire coupling may not be negligible when TSVs and RDLs fall within certain dimensions (the ratio of TSV length and TSV diameter is less than 5 [60]). Therefore, TSV-to-wire capacitance may need to be considered for accurate modeling of the interconnections in a silicon interposer. Figure 95 shows the interconnections in a silicon interposer and TSV-to-wire capacitance.

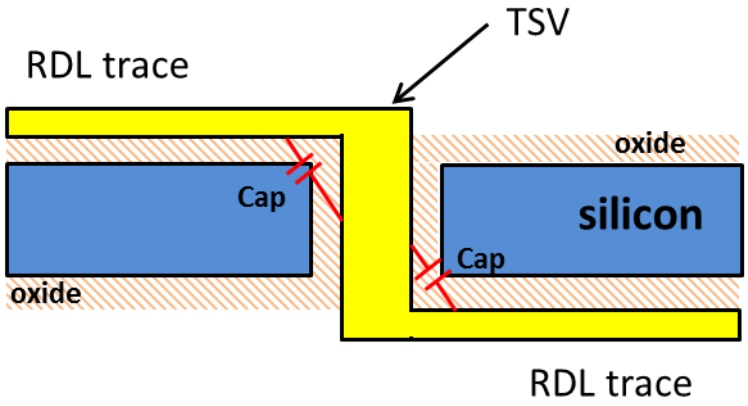


Figure 95. TSV-to-wire coupling.

8.2 Non-conformal Domain Decomposition with Model Order Reduction

The 3-D FDFD non-conformal domain decomposition method has been proposed in this dissertation. The non-conformal domain decomposition method allows modeling each domain independently with non-matching grids at the interfaces. This non-conformal domain decomposition method can be combined with model order reduction (MOR) techniques. MOR method can be applied to an individual domain, therefore, a low-dimensional reduced order model for each domain can be obtained. MOR can reduce the computational complexity of each domain and accelerate simulation time. By combining DDM with MOR, the total number of system unknowns can be reduced further. Figure 96 illustrates the basic idea for system level modeling using DDM and MOR [72].

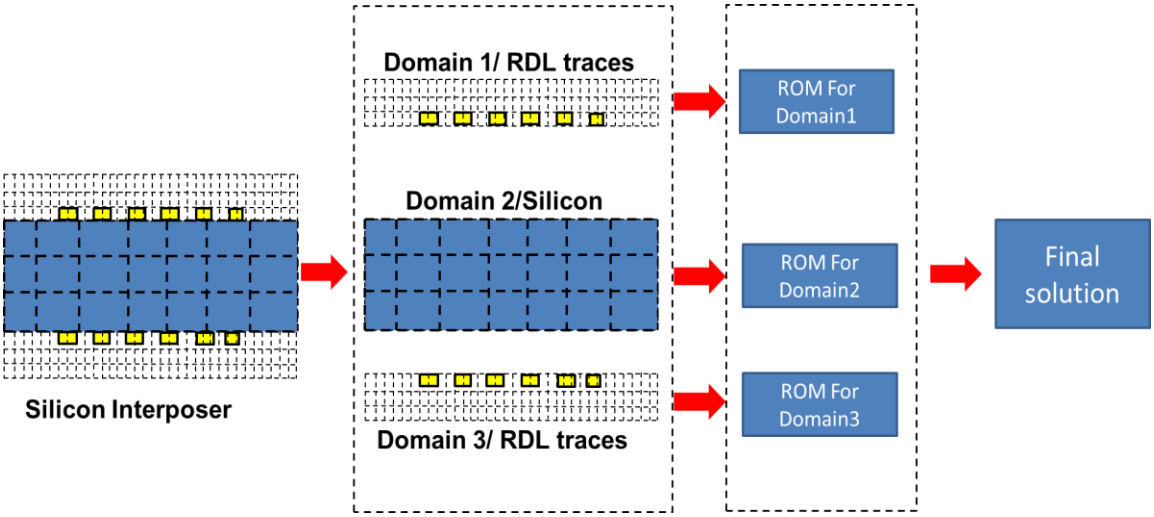


Figure 96. Domain decomposition with model order reduction.

CHAPTER 9

CONCLUSIONS

As the transistor scaling reaches its limits, 3-D integration is becoming a promising technology to continue Moore's law in the future. To enable better and faster design of 3-D systems, efficient and accurate modeling tools are needed. New challenges arise for the computer-aided design and modeling of 3-D integrated systems. As described in Chapter 1 and Chapter 2, the challenges come from several aspects. (1) Multi-scale dimension structures in 3-D systems such as TSVs, (2) Interconnections embedded in a semiconducting medium which is lossy and introduces loss, coupling and distortion, (3) High density TSVs and RDL traces in silicon interposers causing enhanced coupling, and (4) Responses of the PDN become more complicated when a large number of TSVs are included. To address these challenges, several analysis and modeling approaches are developed in Chapter 3-7.

9.1 Contributions

The contributions of this thesis are summarized as follows:

Major Contributions:

9.1.1 Modeling and analysis of simultaneous switching noise in silicon and glass interposers

An efficient approach for modeling the power delivery network with through-silicon vias (TSVs) for 3-D systems is proposed. In the proposed method, power and ground planes are modeled using the multi-layered finite-difference method (M-FDM). TSVs are modeled separately using an integral equation based solver and later incorporated into M-FDM. Using the proposed method, the power/signal integrity of a PDN with TSVs/through-glass vias (TGVs) in a lossy silicon interposer and a low loss glass

interposer is investigated and compared. P/G plane resonances are suppressed in silicon interposers and the benefits of using a silicon interposer is illustrated.

9.1.2 FDFD modeling of signal paths with TSVs in silicon interposers

An approach for modeling signal paths with TSVs based on the FDFD method is proposed. The proposed method utilizes the 3-D finite-difference frequency-domain (FDFD) method to model the redistribution layer (RDL) transmission lines to capture the parasitic effects of multiple transmission lines on a lossy silicon interposer. TSVs are modeled using an integral equation based solver which uses cylindrical modal basis functions. A new formulation for incorporating a multiport network in the 3-D FDFD formulation is presented to include the parasitic effects of TSV arrays into the system matrix. The overall matrix is divided into several subdomains and solved by a divide-and-conquer approach in a parallel manner. The accuracy and efficiency of the proposed method is validated by comparing with 3-D full-wave simulations.

9.1.3 3-D FDFD non-conformal domain decomposition

The 3-D finite-difference frequency-domain (FDFD) non-conformal domain decomposition method is proposed. The proposed method allows modeling individual domains independently using the FDFD method with non-matching meshing grids at interfaces. Field continuity at interfaces between domains is enforced by introducing Lagrange multipliers and vector basis functions at the interfaces. This domain decomposition method has been applied to model RDL traces on silicon interposers. The formulation for incorporating a multiport network into the FDFD non-conformal domain decomposition is derived to include the parasitic effects of TSV arrays in the system matrix. The accuracy and efficiency of the proposed method has been validated by comparing with commercial full-wave solvers.

Minor Contributions:

9.1.4 Coupling analysis of through-silicon via arrays

The coupling effects between TSVs in large TSV array structures are presented. The coupling between TSVs in low resistivity and high resistivity silicon substrates are compared. It concludes that the slow wave mode exists in TSV structures, which induces the long tail of the coupled waveforms. This long tail has a detrimental effect on the signal integrity of the silicon interposer. It also concludes that coupling for low resistivity substrates induces variability in signal integrity across the silicon interposer which can be a major problem.

9.1.5 Electromagnetic modeling of non-uniform TSVs

A hybrid approach for electromagnetic modeling of non-uniform TSV structures is proposed. For non-uniform TSV structures, TSVs are divided vertically into conical and cylindrical sections. The modeling of conical TSVs is presented based on using conical modal basis functions. By using the conical TSV modeling method combined with cylindrical TSV modeling method, complex TSV structures can be modeled efficiently. The accuracy of this hybrid method is validated by comparison with 3-D full-wave simulations.

9.2 Publications

B. Xie and M. Swaminathan, "Coupling analysis of through-silicon via (TSV) arrays in silicon interposer for 3D systems," in *Proc. IEEE Int. Symp. Electromag. Compat.*, Aug. 2011, pp. 16-21.

B. Xie and M. Swaminathan, "Electromagnetic modeling of non-uniform through-silicon via (TSV) interconnections," in *Proc. 16th IEEE Workshop Signal and Power Integrity*, Sorrento Italy, May 2012, pp. 43-46.

B. Xie and M. Swaminathan, "Modeling and analysis of SSN in silicon and glass interposers for 3D systems" in *Proc. 21th Conf. Electrical Performance Electron. Packag. Syst. (EPEPS)*, Oct. 2012 pp. 268-271

J. Xie, **B. Xie**, and M. Swaminathan, "Electrical-thermal modeling of through-silicon via (TSV) arrays in interposer," *Int. J. Numer. Model.,* Sept. 2012.

B. Xie, M. Swaminathan, "FDFD modeling of signal paths with TSVs in silicon interposer*," IEEE Trans. Compon. Packag. Manuf. Technol*., vol. 4, no. 4, pp. 708-717, 2014.

B. Xie, M. Swaminathan, K. J. Han, J. Xie, "3-D FDFD non-conformal domain decomposition method for modeling RDL traces on silicon interposer, " in *Proc. 18th IEEE Workshop Signal and Power Integrity*, Ghent, Belgium, May 2014, pp. 1-4.

B. Xie, M. Swaminathan, K. J. Han, "FDFD non-conformal domain decomposition for the electromagnetic modeling of interconnections in silicon interposer," submitted to *IEEE Trans. on Electromagnetic Compatibility*.

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