Center for Advanced Electronics through Machine Learning (CAEML)

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Background

- A center titled *Center for Advanced Electronics through Machine Learning* (CAEML) has been proposed
- This is an NSF Industry/University Cooperative Research Center consisting of UIUC (Lead), NCSU and GT
- Center focus is on Behavioral Modeling and Optimization of Devices, Circuits, Packaging and Systems through Machine Learning with applications in Digital, RF, Microwave and Mixed-Signal Domains
- The principal investigators (PIs) requested a planning grant from the National Science Foundation (NSF)
- The proposal included 22 letters of interest from industry
  - Indicating a willingness to send a representative to the center planning meeting should the grant be awarded
- Following proposal submission and review, NSF awarded a grant to CAEML
- Center Planning Meeting is scheduled for November 2-3, 2015 in Urbana, IL

Outline

- Better models for better designs
- Machine Learning
- Applications for Behavioral Models in Electronic System Design
- NSF I/UCRC program
  - List of participating faculty

Electronic Design Automation (EDA)

- EDA tools allowed the IC industry to successfully manage 50 years of exponential increase in design complexity[1]
- Simulation is the key tool that has enabled the development of low-cost, safe, energy-efficient electronic systems
  - Ranging from smart phones to airplanes
- Simulation used for both design optimization and verification
- Used for almost every aspect of the design process
  - And, where it is not used, this is because of a lack of adequate models
  - Example: system-level ESD

[1] "NSF Workshop: Electronic Design Automation-Past, Present, and Future", July 8-9, 2009, http://cadlab.cs.ucla.edu/nsf09/

Limits of Modern EDA

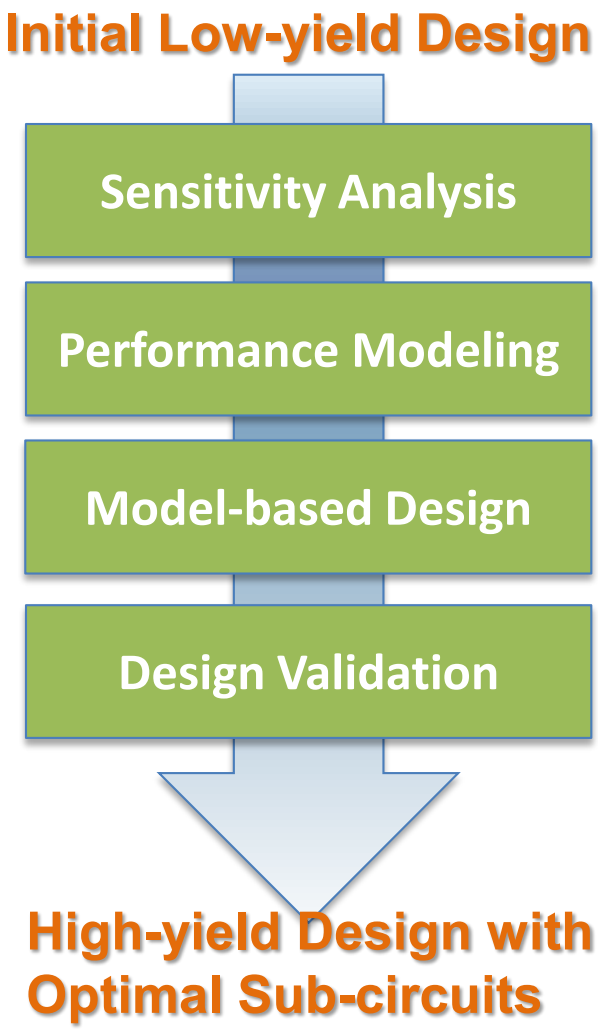
- Today, simulation cannot ensure that an IC will pass qualification testing, but it has reduced the typical number of design "respins" down to just 1 or 2 [2]
- Many of the observed failures during qualification testing are the direct result of an insufficient modeling capability
  - Sources of such failures include mistuned analog circuits, signal timing errors, reliability problems, and crosstalk [2]
- The set of models to support chip-package co-design or circuit-board design are less complete than those for chip design
- A new (better) approach to generating models will advance the capabilities of EDA

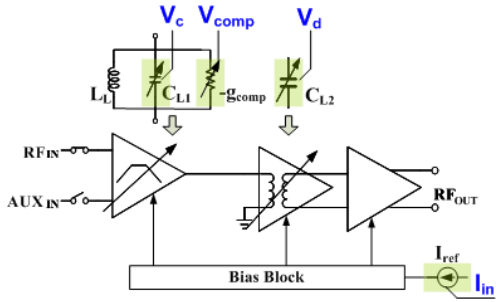
[2] Harry Foster, "2012 Wilson Research Group Functional Verification Study" , http://www.mentor.com/products/fv/multimedia/the-2012-wilson-research-group-functional-verification-studyview

A Hierarchy of Models

- As one moves through the design hierarchy from low level to high level (e.g., from a single device to a consumer electronic product), one uses a different set of models in the simulations
- Only need to represent the response of the object at its external ports, i.e., where it interfaces to the next higher-order system
  - The resulting model is called a *behavioral* model
  - Behavioral modeling can alleviate the IP bottleneck
    - IC suppliers rarely share schematic-level design or technology information with customers
  - Using behavioral models is computationally and energy efficient
- High-level models should be extracted from low-level simulation and/or measurements results
  - Methodology to do this is ad hoc and incomplete
  - CAEML will address this problem

Model-based Design





- Analyze and select efficient calibration knobs.
- Construct parametric performance models with calibration knobs and variations.
- Design and optimize sub-circuits (for yield, power, area, reliability …)

- Computationally efficient, parameterized models allow for design optimization, in addition to verification. Behavioral models may be used for IC design optimization as well as for larger electronic systems.

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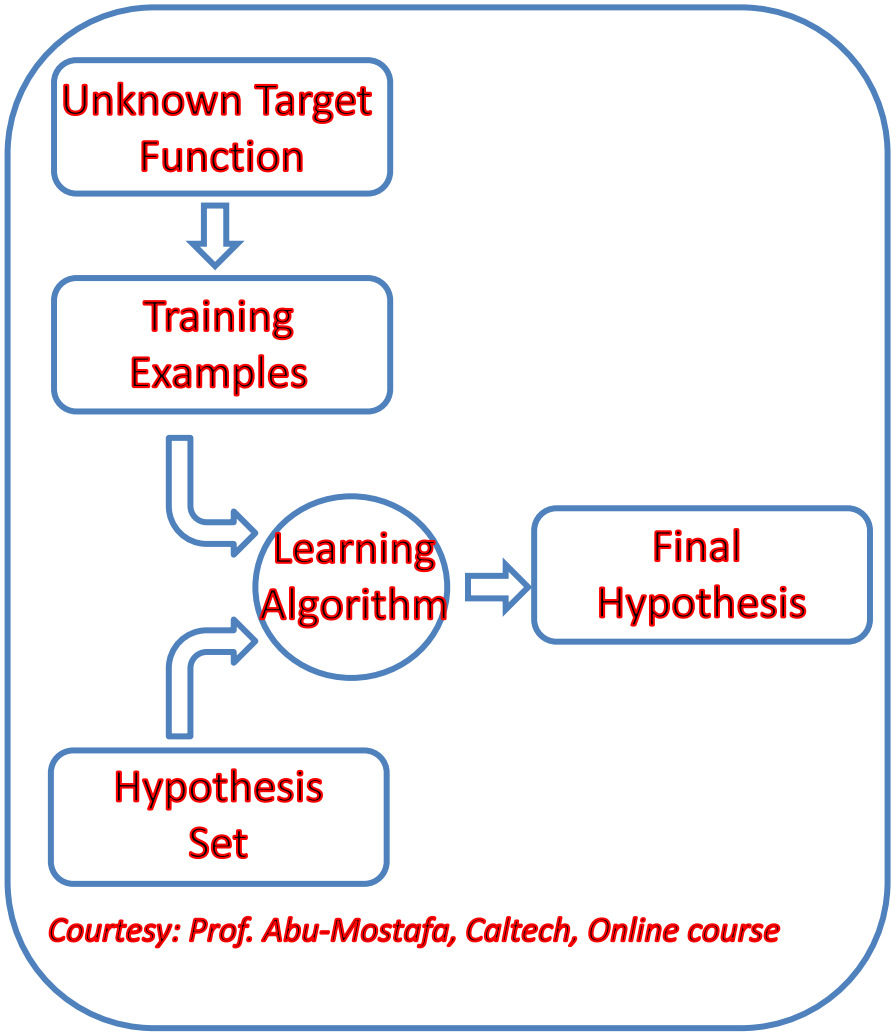
Machine Learning (ML)

- The goal of machine learning is model extraction from data despite the presence of uncertainty, errors and noise.
- The emphasis is on models that provide a good balance between predictive ability and complexity.
- ML is used when the functional relationship between the input (i.e., stimulus) and output (i.e., response) is complex and unknown, and is especially useful when the mapping from input to output includes stochastic effects.

Machine Learning (ML), cont'd



- ML describes an algorithm that takes a set of input-output data and formulates a prediction of the system's output due to an arbitrary input.
- As time progresses, the algorithm gets faster and makes more accurate predictions.
  - **It *learns.***

Electronics Modeling Needs

- A new modeling approach is needed to advance the capabilities of state-of-the-art EDA → ML proposed
- Behavioral models needed for components that are non-linear, time-variant, multi-physics, multi-port

  Today:

  – If component's internal dynamics can be modeled and simulated, behavioral modeling remains challenging and time consuming

  – Or, if response can presently only be observed in measurement, input-output relation must be extracted by trial and error

  – Unavailability of models is a roadblock to advancing the state-of-the-art in EDA

Electronics Modeling by Machine Learning

- ML well known in fields such as computer vision, but more recently has been used to model reliability of communication networks and power grids
  - Many commonalities with ICs and electronic products: heterogeneous, large number of interacting components, multiple ports
- **ML based modeling will provide an unprecedented capability to optimize electronic systems for performance, power and reliability**

Machine Learning Research in CAEML

- Physics-aware modeling
  - Reduce risk of obtaining non-physical results outside the space covered by the input datasets
  - Eliminate large classes of available models
    - ➢ Reduce model extraction time
- Incorporation of component variability
  - Perhaps using chaos expansions
- Quantify minimal training data requirements
- Handling multi-port components
  - Exploit known dependencies between the ports to reduce sample complexity and speed up learning
- Adding an adaptive component that can learn (i.e., incorporate) prior knowledge from multiple designers
  - Use prior knowledge both for learning and testing of models

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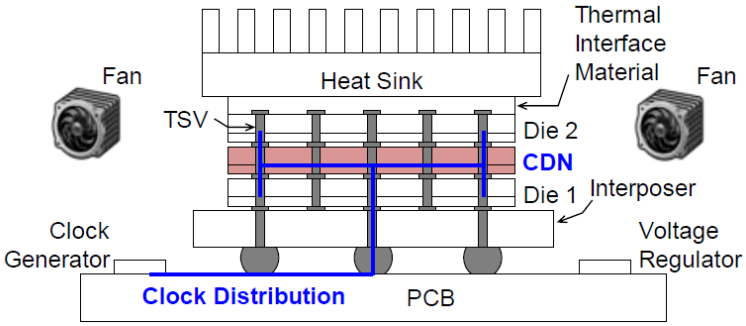
Applications of Behavioral Models

- High-speed link optimization
- Chip-package co-design
- System-level ESD design
- Non-linear PDN simulation
- RF and mm-wave parasitic extraction
- Mixed-signal verification
- And many others …
- **Over the next few months, we seek to have discussions with our prospective industry partners to learn about their biggest needs and interests**

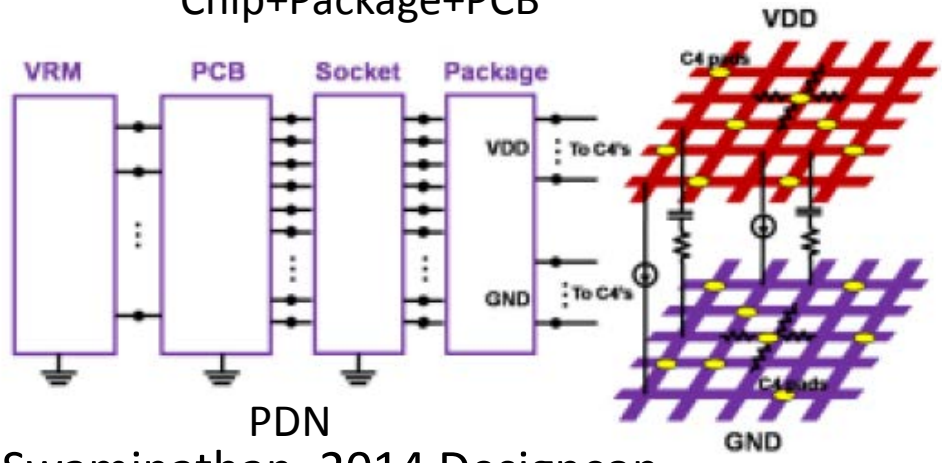
7 Example Projects

- Some of these will likely be among the first projects funded by the CAEML
- Other projects may result from the upcoming industry-university discussions

Power Distribution

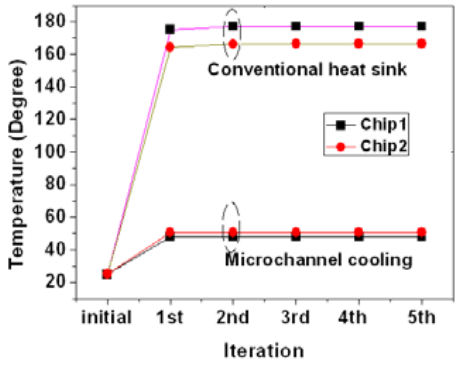


Chip+Package+PCB

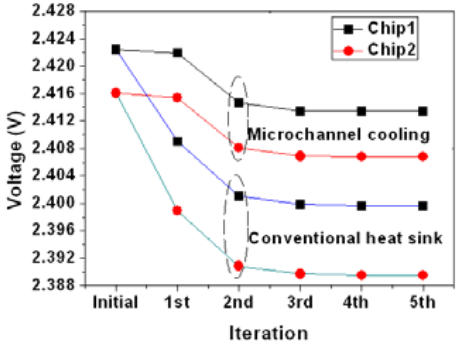


PDN

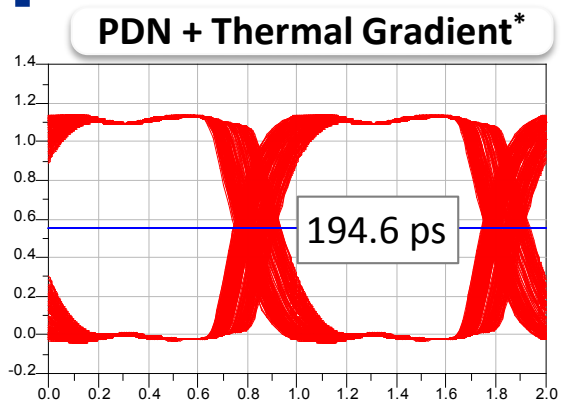
Swaminathan, 2014 Designcon



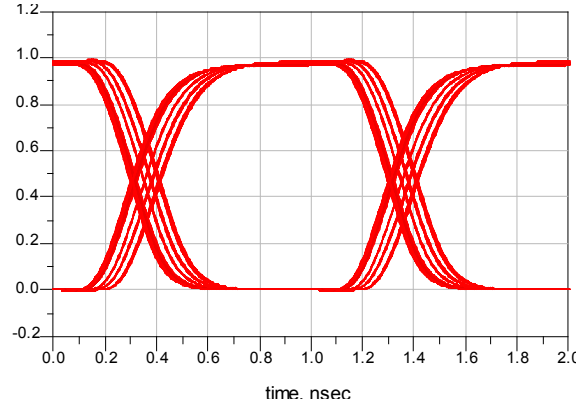
Joule Heating (Temp)



Joule Heating (Voltage)



Before Compensation



After compensation

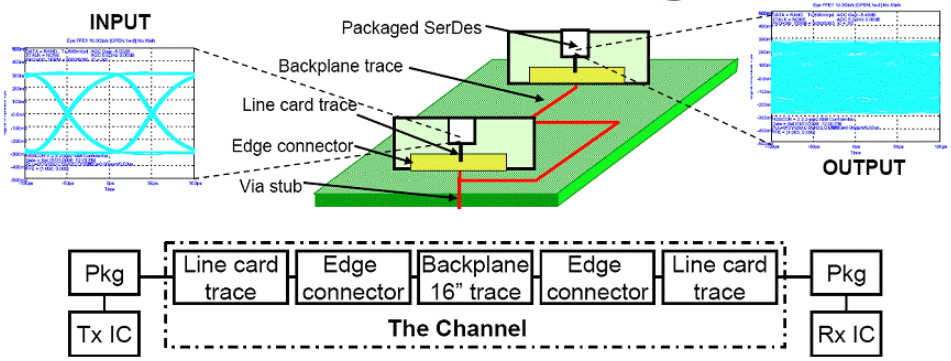
Goal: Compatible, behavioral models of active and passive elements that enable non-linear PDN simulation.

Approach: Use ML to derive models from EM and circuit-level simulation results and measurement data.

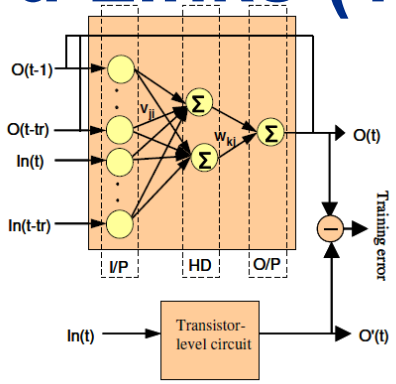
Motivation: PDNs are increasingly non-linear. Temperature-aware compensation techniques such as Dynamic Voltage and Frequency Scaling considering temperature effects become important.

Modeling & Design Optimization of High-Speed Links (1/2)

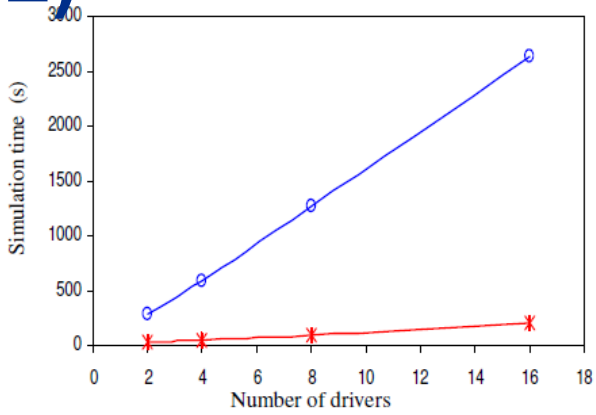
Swaminathan, GT



High Speed Channel

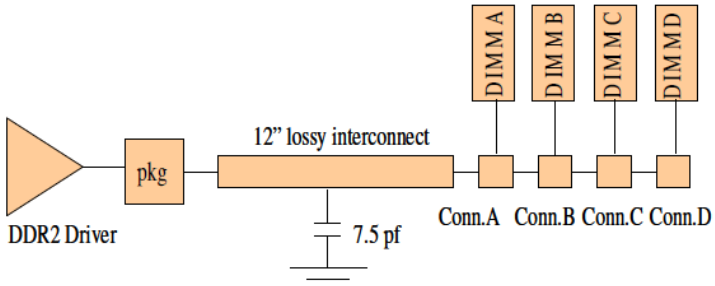


Black Box Model

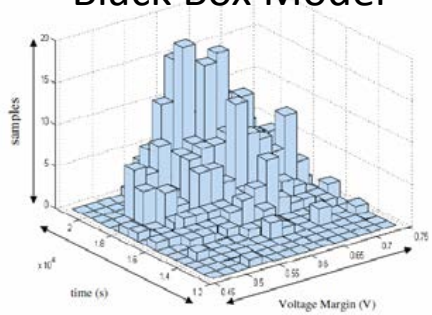


Time savings using Black Box models

Mutnury, 2005 GT PhD Thesis



Memory Channel



Statistical Analysis

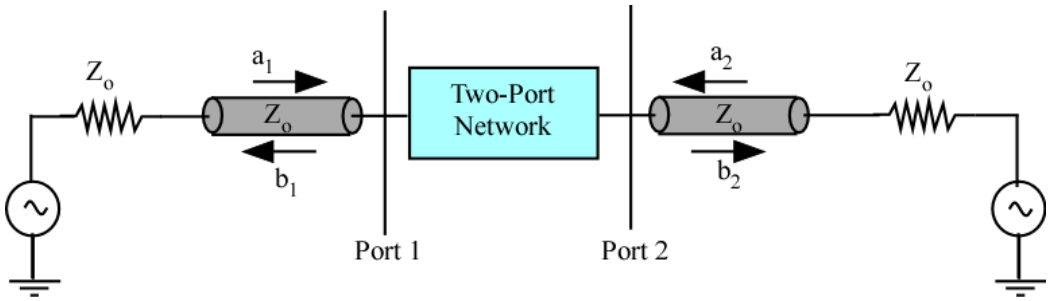
Goal: Extend IBIS methods to create scalable, behavioral models of complex driver and receiver circuits which capture the effects of noise and other non-linear phenomena.

Motivation: The drivers and receivers contain complex pre-emphasis, pre-distortion, equalization and other compensation circuits to enable high-speed signal transmission across lossy media. With Near Threshold Voltage (NTV) signaling, power supply noise, temperature effects and process variations increasingly affect the link performance.

Modeling & Design Optimization of High-Speed Links (2/2)

Schutt-Aine, UIUC

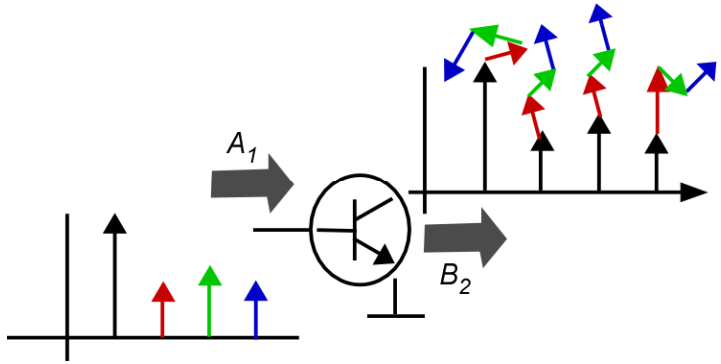
S-parameters



" …most successful behavioral models…"

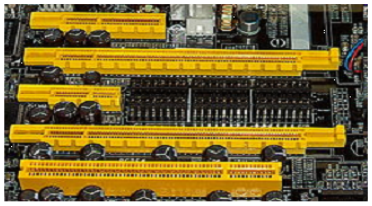
…but only works for LTI…

X-parameters

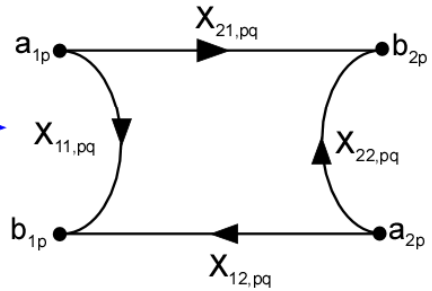


Includes harmonic-to harmonic interactions in addition to port-to-port interactions to capture nonlinear behavior in the frequency domain

Serial Links



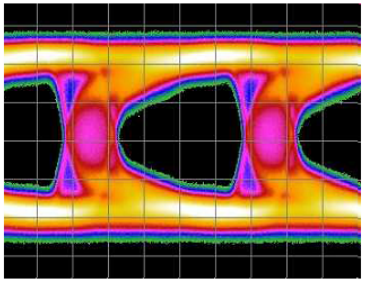
Nonlinear X-Parameters



Model Order Reduction (Multitone)

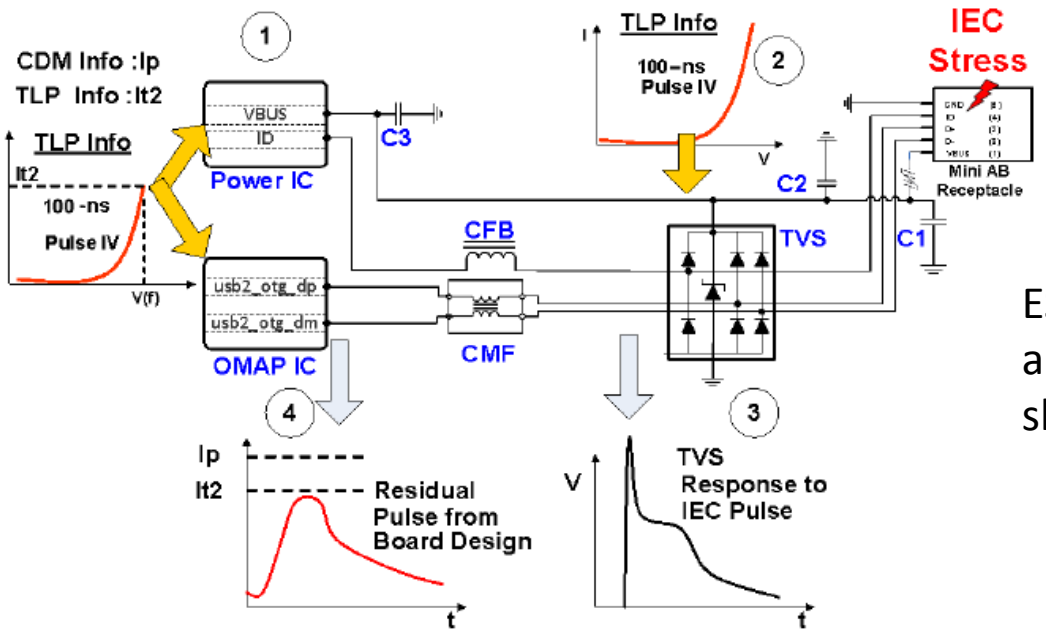
$$\sum_{n=1}^{L} \frac{c_n}{z - a_n}$$

Statistical Simulations



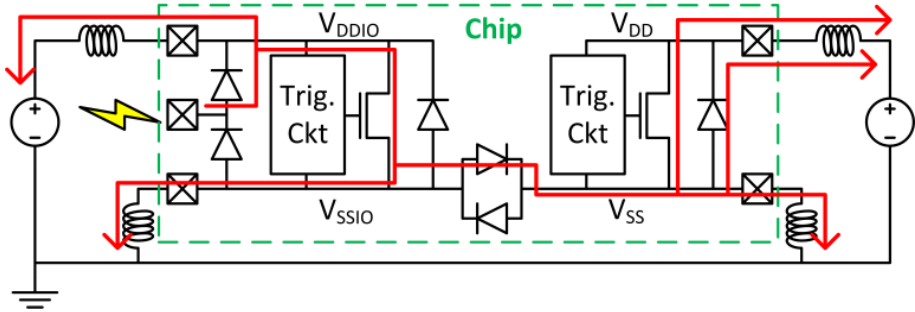
Goal: Demonstrate X-parameters as a framework for behavioral modeling of high-speed links.

System-level ESD Design



[Bertonnaud, 2012 EOS/ESD]

Simulate the residual ESD that's not filtered on-board and its effect on ICs



ESD has many return paths to system ground. Upset and latch-up get triggered in circuit blocks that should be isolated from I/O. [Mertens, UIUC 2014]

<u>Goal</u>: Derive component ESD models so that simulation can be used to design ESD-robust systems.

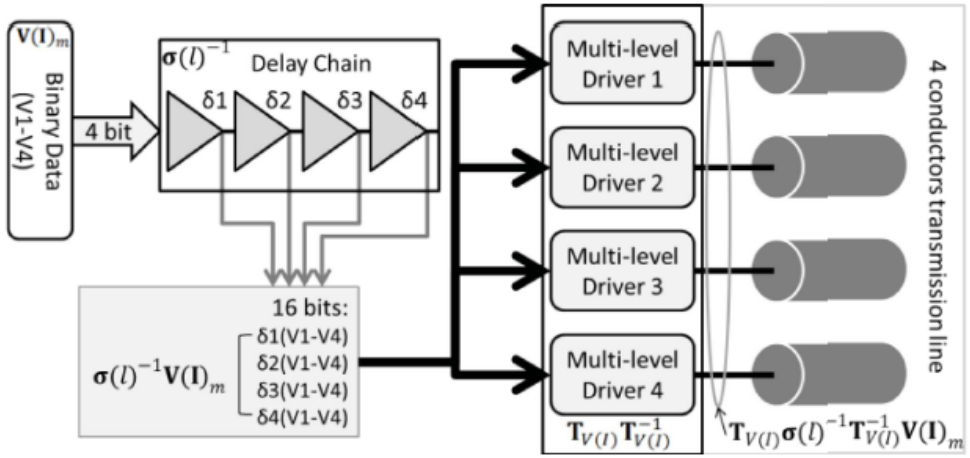
<u>Approach</u>: Use ML to extract behavioral models from measurement data and circuit simulation results.

<u>Motivation</u>: System ESD reliability presently obtained through trial and error testing of system prototypes.

ESD soft failure: Logic upset in domino gates (msmt). Windowing effect complicates modeling. [Thomson, UIUC 2014]

ESD (kV)	Data Upset
$\|V_{PRE}\| \leq 2$	0 %
4	93.3 %
-4	4.2 %
6	20.8 %
-6	12.5 %
8	0 %
-8	0 %
4	30 %
-4	0 %
6	8.3 %
-6	0 %
8	0 %
-8	0 %

Chip-Package Co-design



Yan, 2013 ECTC

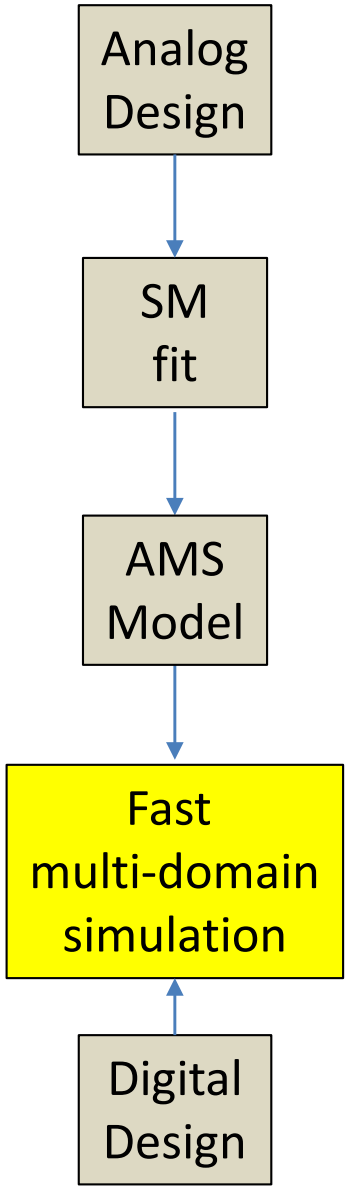
Goal: Cross-domain modeling for chip-package co-design

Approach: Use ML to derive behavioral models for the other domain that capture relevant behaviors and are fast to evaluate. Parameterized models that include design variables.

Motivation: Co-optimization of chip design (floorplan, IO assignment, IO coding, etc.) and package design (SI and PI management features) is currently very expensive in simulation

Mixed-Signal Design Verification

- Problem:
  - High simulation cost to verify digitally-assisted analog circuits for all possible switch settings
    - ➢Both functional and electrical verification affected
    - ➢E.g. Difficulty in Electromigration supply wire sizing
- Solution:
  - Represent analog design using a fast-to-evaluate Behavioral Model obtained via ML
  - Enables fast simulation through a combination of HDL and AMS languages



Layout Assistant for Mixed-Signal Designs

- Problem Statement:
  - Modern designs have over 2,000 design rules and numerous design guidelines, requiring frequent iteration between design and rule checking
- Solution:
  - Create a “Magic” tool for the 21st Century
    - Magic was a 1980s layout tool that incorporated online interactive DRC
  - Use machine learning to give feedback and suggestions on design during the design process

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NSF I/UCRC Program

- Industry/University Cooperative Research Center
- NSF encourages the formation of multi-university centers
- Several research projects under the umbrella of a common research theme
  - Overarching research theme produces core knowledge that enables the various projects
  - Industry needs drive the project selection
    - ➢Industry advisory board (IAB) votes on projects
- Pre-competitive research

I/UCRC Program Overview

- Year 1: Planning grant
  - **No financial contribution from industry**
  - Prospective, industry members of center attend a workshop
    - PIs describe center theme
    - Faculty propose projects
    - Projects ranked by industry
  - PIs write center proposal for NSF
    - Includes description of projects to be funded initially
    - These projects were ranked highest at the workshop
- I/UCR Center
  - 5 years, can be renewed if interest persists
  - Very low overhead (10%)
  - Twice annual research review and IAB meeting
  - New project starts each year, selected by IAB
  - Industry access to students for internships and permanent employment
  - Opportunity for industry engineers to work on campus with researchers

I/UCRC Benefits to Industry

- More bang for your buck
  - NSF pays administrative expenses
  - Industry funds used to support research
  - Funds are pooled
  - 6:1 leveraging of NSF funds*
  - 47:1 leveraging of industry funds*
- Members have rights to IP (non-exclusive)
- Graduate students perform industry-relevant research
  - 30% are hired by the center companies upon graduation*
  - Consistently rated by employers as superior on professional preparation, communication and teamwork than non-I/UCRC students*

*Boot Camp for I/UCRC Planning Grantees, Mar. 13, 2015, National Science Foundation.

I/UCRC Benefits, cont'd

- Industry and academia jointly set research goals
- Industry Advisory Board selects projects for funding
  - Ensures research portfolio remains highly relevant
- Some centers have been in existence for > 25 years
  - High industry satisfaction
- Participants get early access to leading edge research, mentoring of students, student recruitment
  - Option for placement of industry engineers on campus

CAEML Benefits to Industry

- CAEML will help the member companies do business with each other
  - By providing robust models and tools
- IP-obscuring models allow for flow of critical information between customers and suppliers
  - Rationale for the industry to have developed IBIS
  - Machine learning will provide models of much wider scope and accuracy than IBIS can support
- CAEML's foundational research on ML can be applied to applications of specific interest to one company
  - By its own engineers
  - By CAEML students during industry internships
  - Under a separate, sponsored research project

Participating Faculty

- University of Illinois at Urbana-Champaign
  - Andreas Cangellaris
  - Maxim Raginsky
  - Jose Schutt-Aine
- Georgia Institute of Technology
  - Chuanyi Ji
- North Carolina State University
  - Rhett Davis
  - Brian Floyd
- Site directors: Rosenbaum (UIUC), Swaminathan (GT), Franzon (NCSU)

Time Line

- Spring/Summer 2015: Cement commitment of industry partners to attend the planning meeting.
- Spring/Summer 2015: Recruit additional prospective industry members
  - National labs and industry associations also eligible for membership
- Spring/Summer 2015: Hold discussions with prospective partners; learn more about their research needs
- November 2-3, 2015 at UIUC: Planning grant meeting.
  - Attendees: NSF representatives, participating faculty, representatives from interested companies, Center evaluator
  - Objective: Familiarize industry reps with administrative (legal, financial, organizational) details of I/UCRC
  - Objective: Obtain industry rankings and feedback for proposed research projects
  - Goal: Have industry representatives recommend that their companies join the CAEML
- March 2016: Submit full center proposal to NSF.
  - Based on industry interest and support, research may begin in advance of center award