WIRELESS POWER TRANSFER USING INTEGRATED AND EMERGING TECHNOLOGIES

A Dissertation
Presented to
The Academic Faculty

By

Colin A. Pardue

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology

August 2018

WIRELESS POWER TRANSFER USING INTEGRATED AND EMERGING TECHNOLOGIES

Approved by:

Dr. Madhavan Swaminathan
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Saibal Mukhopadhyay
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Hua Wang
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Arijit Raychowdhury
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Paul Kohl
School of Chemical and Biomolecular Engineering
Georgia Institute of Technology

Date Approved: April 20, 2018

2 Corinthians 3:5 - Not that we are competent in ourselves to claim anything for ourselves, but our competence comes from God.

ACKNOWLEDGEMENTS

To expand on my dedication, God deserves the singular credit for this dissertation. To Him belongs all credit for the relationships and friendships I've developed that have helped me, my passion for engineering, major decisions I've made, ideas and inspiration, and my foundation during my most frustrating moments. As a Christian, I know God has a purpose for me getting a PhD, and He wouldn't let my shortcomings prevent His plan. And for that I am endlessly grateful. Even if you don't believe in the existence of God, then I would say it's still undeniable that my faith in God sustained me.

But acknowledgements aren't fun if I only recognize God, so I need to recognize a few others. First, my advisor Dr. Swaminathan. The opportunities he granted me to pursue many different research paths, culminating in this dissertation, gave me plentiful interesting research thrusts to pursue. In addition, Dr. Swaminathan provided superior guidance in research objectives, publications, industry connections, and presentations that was all the mentorship a PhD student needs and then some. An advisor in every sense of the word. I also need to mention the postdocs Dr. Anto K Davis and Mohamed Bellaredj. Both of them were crucial in meeting various research objectives, as noted in the following dissertation. It was a pleasure working with both of you and I hope you benefited from working with me even half as much as I did with you. I also would like to thank my reading committee members Dr. Saibal Mukhopadhyay and Dr. Hua Wang and other defense committee members Dr. Arijit Raychowdhury and Dr. Paul Kohl for their feedback, and more importantly, their time and attendance at my defense since this is never an easy thing for any GT professor. Thanks to fellow PhD students (current and graduated), with Hakki, Sridhar, Huan, Satyan, Kyuhwan, Majid, and David particularly helpful during my PhD time. I appreciate your support during my graduate studies, as well all the other Swami Ph.D. students, visiting students, visiting scholars, masters students, and more too numerous to count.

To my family, Dad, Mom, Jacob, and Grace, who let me vent and provided encour-

agement, I thank you. Also to my late grandmother Kazuko Bryant, who might have been more proud of my intellectual accomplishments than anyone else. To all my friends, I came to Atlanta knowing no one and now find leaving all the friends I've made here the hardest part about graduating. I particularly want to single out Jason, Michael, Philip, the Wynns, Ruben, and Daniella as well as fellow students I met at GT studying for the Prelim and sharing many (sometimes embarassing) memories with, the rest of my FBA Mission Possible family (I don't use this word lightly), the Reynolds and Alaska Mission Trip teams, and all the Mary George crew. To my future dog, I've told myself I can adopt you once I graduate so you might have been the strongest incentive I had.

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SUMMARY

To support the next generation of compact low power devices, a wireless power transfer solution needs to have an improved combination of receiver coil area and efficiency. This dissertation examines RF near field coupling as a means to minimize coil area while maximizing efficiency in integrated, regulated systems. Presented contributions include the efficiency analysis, design procedure, and integration challenges for high efficiency RF near field coupling systems. Along the way, the use of a reverse power distribution network and integrated inductors are explored. A few designs are fabricated and measured, showing a superior combination of receiver coil area and efficiency for low power applications. While RF near field coupling is only a viable solution for select applications, this dissertation serves as a guide for understanding the various challenges and considerations for designing regulated, RF near field coupling systems.

CHAPTER 1
INTRODUCTION

1.1 Motivation

According to Intel, the world will have 200 billion smart devices by the year 2020, corresponding to 26 smart devices per person on the planet [1]. With these devices connected through the Internet of Things (IoT), the application space is seemingly endless in support of industry, healthcare, urban environments, and at home. The 'things' in the IoT have limitless combinations of size, energy consumption, technological complexity, and load application power.

One problem common to all IoT devices however is power delivery and regulation. If there are truly 200 billion smart devices within the next couple of years, creative solutions for powering these devices would enable the IoT to expand beyond current hardware limitations. Specifically, relying solely on batteries and the grid is not an ideal solution. Batteries become costly in high volume and need to be replaced - an inconvenience at best and completely impractical at worst. Providing wired power delivery requires a physical connection, limiting the placement and location of an IoT device while being subject to physical wear and tear on the devices. Wireless power transfer (WPT) offers a convenient, contactless charging solution for various applications. WPT is especially discussed and used in conjunction with the IoT. The design objectives for a WPT system changes greatly depending on the application (i.e. load power), each with their unique challenges. The objective of this thesis is to demonstrate a fully integrated receiver solution for milliwatt-scale wireless charging applications.

1.2 Survey of Wireless Power Transfer Techniques

Various WPT systems have been demonstrated in prior literature. WPT systems may be generally evaluated by 3 main metrics: efficiency, transmission distance, and receiver area. The tradeoffs between these metrics are shown in Fig. 1.1. Receiver area for the purpose of this dissertation is defined specifically by the area of the power transfer element, such as an antenna or an inductor. It is impossible to be superior to all other WPT systems in all 3 of these areas. For a given transmission distance and receiver area, for example, there will be a fundamental limit to efficiency that cannot be exceeded. For higher efficiency, one of the other two metrics has to be sacrificed. For low power applications, receiver area is a more important consideration than for higher power applications. The application space for milliwatt-scale loads includes wearables, biomedical devices such as hearing aids and implantables, and various small IoT devices (ex: sensors). Wireless power transfer systems have been designed to support mW load power previously, such as for compact smart everyday objects [2], implantables and biomedical devices [3], [4], electronic shelf label [5], and wearables [6]. As many of these electronics are already small in size, it is imperative for a WPT solution to have a fully integrated receiver with small area and high efficiency to support these devices, sacrificing transmission distance to accomplish these goals. With high efficiency, a low power source can be used to charge the devices, decreasing potential interference issues that will only become a bigger concern as the number of wireless devices continues to increase.

A sample implementation of an integrated RF near field coupling system for low power, compact IoT devices is shown in Fig. 1.2. This system consists of the RF WPT near field receiver coil, RF rectifier, PDU (or power management unit), battery or energy storage device, low power IoT module (such as microcontroller units and/or wireless connectivity chips), and application hardware (such as sensors). This dissertation focuses on the integrated design of the power transfer front end - the RF near field coupling, rectification, and

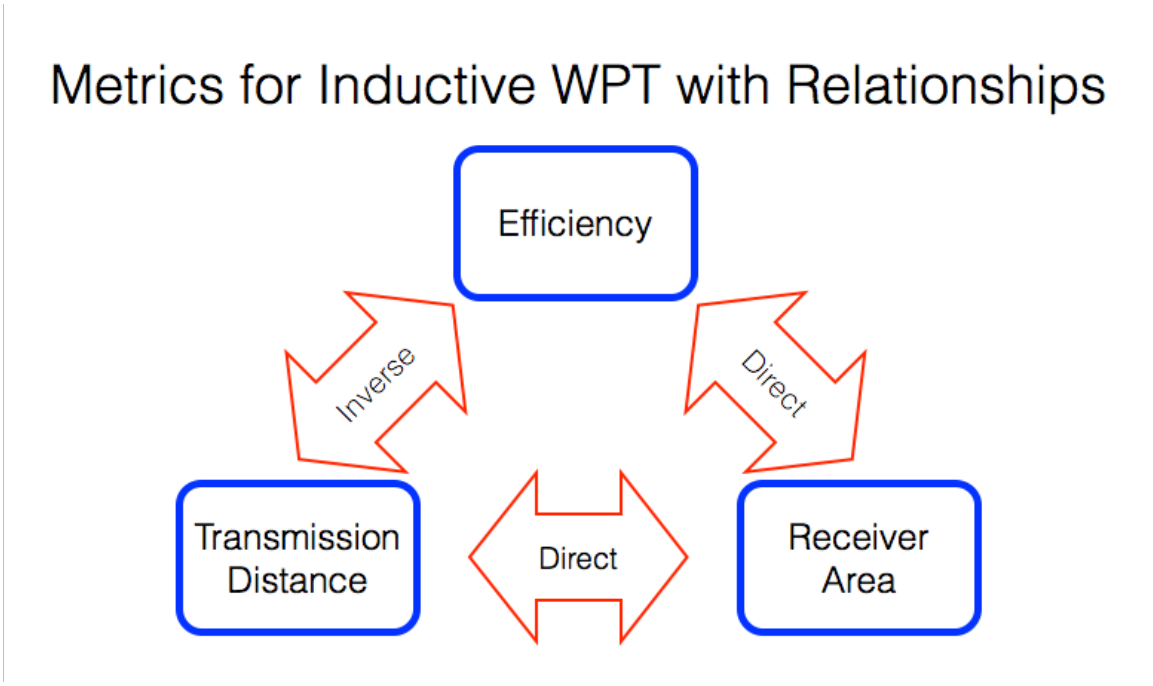

Figure 1.1: Relationships between the main metrics for inductive resonant coupling WPT systems

PDU. The back end - the battery, IoT module, and application hardware - are not shown in this dissertation but modeled as a resistor load for demonstration. This back end is very common among IoT implementations. For low power sensors, the load power is commonly in the 0.1-5mW range for temperature sensors, humidity sensors, positional sensors, accelerometers, etc. Rather than power these sensors continuously, an IoT module with MCU/transceiver capabilities interfaces with the application hardware and wirelessly connects to the IoT cloud, operating on demand. Examples of low power IoT modules include the Dialog Semiconductor DA14580 SmartBond(TM) SoC (15 mW active power consumption), Radiocrafts RC18x0 radio module platform (5.5 mA/22 mA, receiver/transmit current consumption), Texas Instruments CC2640R2F SimpleLinkTMBluetooth low energy Wireless MCU (5.9 mA/9.1 mA active consumption), STMicroelectronics BlueNRG Bluetooth modules (7.7 mA/8.2 mA active consumption), and Maxim Integrated MAX32620 low power MCU (122μW/MHz active consumption). By pairing the control/connectivity modules with the application hardware, endless IoT applications may be supported. For

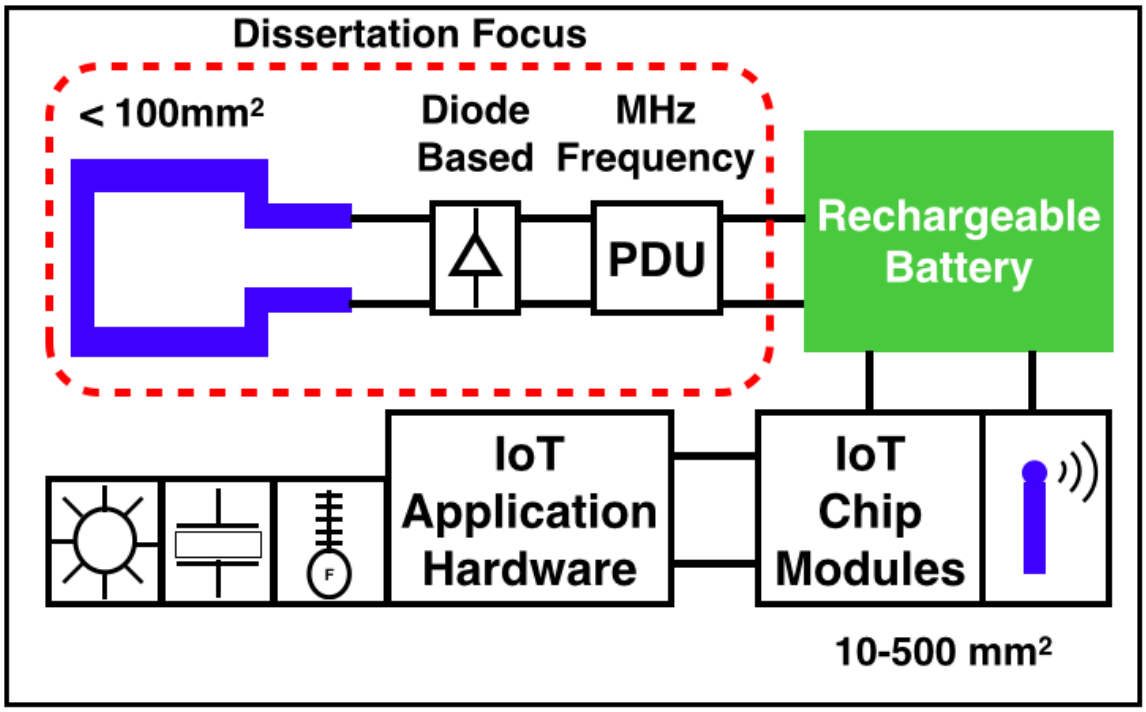

Figure 1.2: Example implementation of integrated RF near field coupling for IoT applications

instance, Dialog Semiconductor partnered with Bosch Sensortec to develop a low power smart sensor platform for IoT devices [7]

The main motivation for developing ultra-low power IoT modules is to preserve battery life. Even so, eventually the battery or energy storage module will need recharging. While the active power consumption of the aforementioned IoT modules is variable and load application dependent, the general range is 1-50 mW. This is where the objectives of this dissertation apply. IoT applications prefer wireless power transfer solutions, replacing the need for connection to the grid and need for a physical charging port on the device (crucial for compact devices). For this level of power consumption, near field coupling is the ideal solution. Energy harvesting is commonly used in conjunction with the IoT because it does not need a dedicated power source. RF energy harvesting has been demonstrated in [8]-[11], but these implementations require a bulky antenna integrated with the receiver. The amount of harvestable RF energy according to [12] may not for suitable for many mW loads

and battery charging applications. Alternative forms of energy harvesting, such as solar [13] and thermoelectric [14], also require a bulky off board harvester that is not suitable for integrated WPT receiver. To this point, energy harvesting is ideal for applications such as self-sustaining, low power, batteryless sensors and devices but not for wireless charging of compact IoT platforms.

Farfield power transfer is another commonly used technology for IoT applications. With farfield power transfer, the receiver may be far from the power source, increasing the convenience for device recharging. Unlike energy harvesting, farfield power transfer is capable of transmitting sufficient power to the receiver to support low power IoT devices. In [15], a distributed farfield WPT system was developed for wireless charging of low power IoT devices. However, this implementation requires an off board, bulky dipole antenna. Furthermore, to increase the receiver output power depending on application needs, a potentially harmful source power may be used, though this may be avoided through the use of distributed control algorithms such as demonstrated in [16]. The more significant issue is farfield power transfer is unable to provide the combination of low device area and output power necessary for compact IoT platforms. A small area antenna (8 mm^2) for farfield WPT was demonstrated in [17], but with only 1 μW output power. Conversely, farfield power transfer systems providing milliwatt-scale output power, as is suitable for low power IoT devices, have large antenna area even at RF as seen in [18] (17,000 mm^2, 2.45 GHz) and [19] (8,000 mm^2, 1.85 GHz). While some low power IoT devices will prefer the convenience and transmission distance provided by farfield WPT, compact devices needing an integrated receiver solution will not find a suitable combination of output power and device area supported by this method.

Capacitive wireless power transfer delivers power through an electrical field. Examples of these systems include [20] and [21]. These papers discuss capacitive power transfer as an alternative to near field inductive resonant coupling, showing capacitive power transfer maintains efficiency better when the receiver is flexible (and flexed) or in the case of lateral

misalignment. Neither of these cases are a focus of this dissertation.

Inductive based wireless power transfer is the most commonly used technique for WPT systems. Inductive power transfer (IPT) is differentiated here from near field inductive resonant coupling. IPT operates as a transformer, with a secondary coil in close proximity to the primary to subtend as much of the magnetic flux generated from the primary as possible. Few recent demonstrations use IPT, most commonly seen with very high power output for applications such as vehicle charging [22]. IPT systems are generally characterized by very large coil area, small transmission distance, and very high efficiency.

Most recently demonstrated systems in academic literature and almost all commercially available systems utilize near field resonant inductive coupling (RIC). RIC transfers power in an oscillating magnetic field generated by a transmit coil to a receive coil tuned to the same resonant frequency. This power transfer efficiency is not just dependent on the coupling coefficient, as with IPT, but on the quality factor of the inductors as well. Because of this, the transmission distance may be increased OR the coil area decreased while maintaining good efficiency. For RIC systems, the WPT design metrics show a strong correlation with load power. This is shown in Fig. 1.3, where each listed reference includes a complete RIC or IPT system consisting of at least a 2-4 resonant coil link and rectifier (complete details on these numbers and references are provided in a table in the appendix) [23]-[53]. As seen from the graphic, higher power applications are often designed with high transmission distance and efficiency, at the cost of large coil area. On the other hand, RIC systems with small coil area and small transmission distance favor lower power, as is appropriate for this dissertation. However, the smaller coil area, lower load power demonstrations also have low efficiency, as shown in the graphic. This dissertation focuses on a near field coupling receiver that achieves both high efficiency and small coil area at the expense of transmission distance.

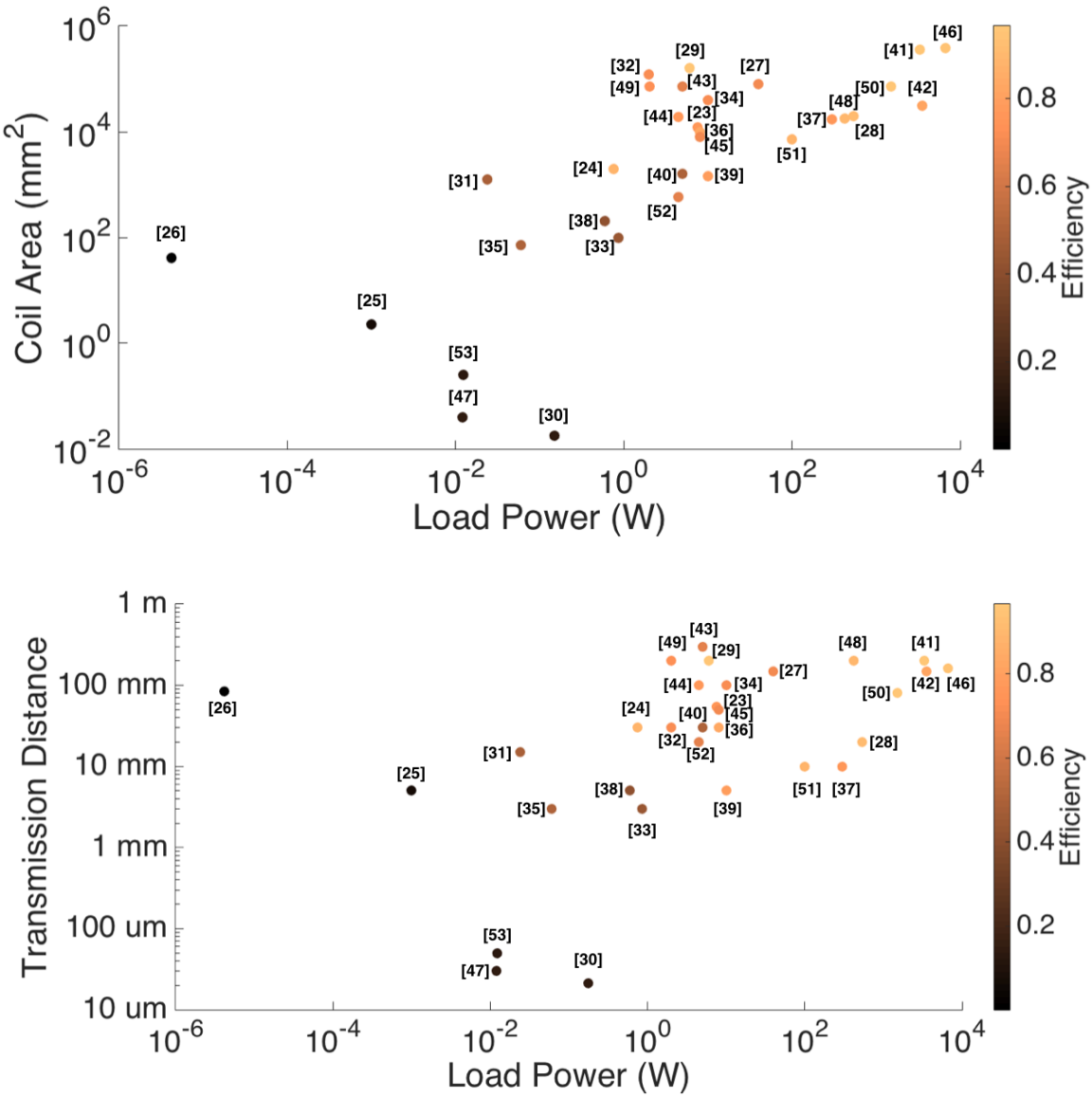

Figure 1.3: Characteristics of RIC systems in academic literature, relating to their coil area, transmission distance, load power, and efficiency

1.3 Effect of Frequency on Resonant Inductive Coupling

The maximum power transfer efficiency (PTE) for a pair of inductive resonant coupling coils is given by (1.1), where k is the coupling coefficient and Q_1, Q_2 are the quality factor of the coils. Almost all of the WPT systems from Fig. 1.3 operate at high kHz or low MHz frequency. A main objective in this dissertation is to show that by operating the coils with a RF source frequency, the area of the coils may be greatly reduced without sacrificing power transfer efficiency. The quality factor of an inductor, shown in (1.2), may be increased 3 ways: decreasing the resistance, increasing the inductance, or increasing the source frequency. These quantities are interdependent. For example, increasing the frequency will increase the resistance due to skin effect at minimum.

$$\eta_{PTE,max} = \frac{k^2 Q_1 Q_2}{(1 + \sqrt{1 + k^2 Q_1 Q_2})^2} \tag{1.1}$$

$$Q_n = \frac{2\pi freq_{RFsource} L_n}{R_n} \tag{1.2}$$

However, by increasing the source frequency by a couple of orders of magnitude compared to most resonant coupling demonstrations, the same quality factor may be achieved with a couple of orders of magnitude inductance reduction. This leads to substantial potential for area decrease. While the resistance must be more carefully considered at RF, RF operation offers the best potential for high PTE, low area inductive resonant coupling coils.

Increasing the frequency to decrease circuit area is well established in electrical engineering, and this may be seen with resonant inductive coupling work. Figure 1.4 shows a comprehensive comparison of prior demonstrated RIC coils. The scope of the cited work is increased from Fig. 1.3, as some references include just two power transfer coils and no AC-DC conversion, others 4 coils with rectifier, and other works 2 coils with an inverter, rectifier, and power distribution unit (PDU) in a complete system suitable for a fully integrated wireless charging receiver (essentially, if a reference has at least 2 coils operated at

Table 1.1: RF Inductive Coupling Coils in Literature

Reference	Frequency	Load Power	Transmission Distance	Coil Area	Efficiency	Rectifier	PDU
[25]	986 MHz	1 mW	5 mm	2.25 mm^2	7%	Y	Y
[56]	4.7 GHz	0.1 μW	1.2 mm	0.01 mm^2	1%	N	N
[54]	5.8 GHz	10 μW	1 mm	0.01 mm^2	1%	N	N
[47]	1 GHz	12 mW	30 μm	0.04 mm^2	14%	Y	N
[64]	460 MHz	10 μW*	200 mm	100 mm^2	0.6%	N	N

resonance, it can be included in the table). However, Fig. 1.4 is merely intended to give a sense of how operating frequency plays a major role in inductor size for resonant inductive coupling coils (with complete details provided in a table in the appendix). The RF near field coupling coils in Fig. 1.4 have the smallest coil area, while the lowest frequency systems have the largest receiver coil area. However, these low coil area systems also share another trait - low efficiency. Table 1.1 shows a comparison of just the near field coupling demonstrations that have a RF source frequency. This table shows that while operating near field coupling coils with RF source frequency and smaller size is not new, accomplishing this with a very high efficiency, fully integrated receiver has not been previously demonstrated. A creative RF WPT system with very small coil size and use of backscattering in the RF-DC conversion is demonstrated in [25], but the efficiency and load power (1 mW and below) is much lower than suitable for this dissertation. A chip-chip RF WPT system is demonstrated in [47], but this work prioritizes coil area much more than efficiency, as is appropriate for a chip implementation. The other three works only demonstrate the coils themselves with no RF-DC conversion. This is the problem this dissertation addresses - achieving high efficiency and small coil size in an integrated, regulated WPT receiver.

A more suitable benchmark for this dissertation is found in Table 1.2, where each reference demonstrates an inductive WPT system with regulated output, but at lower frequency. In [23], a high efficiency WPT system is shown but with lower frequency and accordingly large coil size. A regulating rectifier is demonstrated in [35] with decent efficiency and small coil area; however, both this efficiency and coil area may be improved with higher frequency operation. A system architecture and design very similar to the goals of this dissertation is presented in [27], however the coil area is very large and not practical for in-

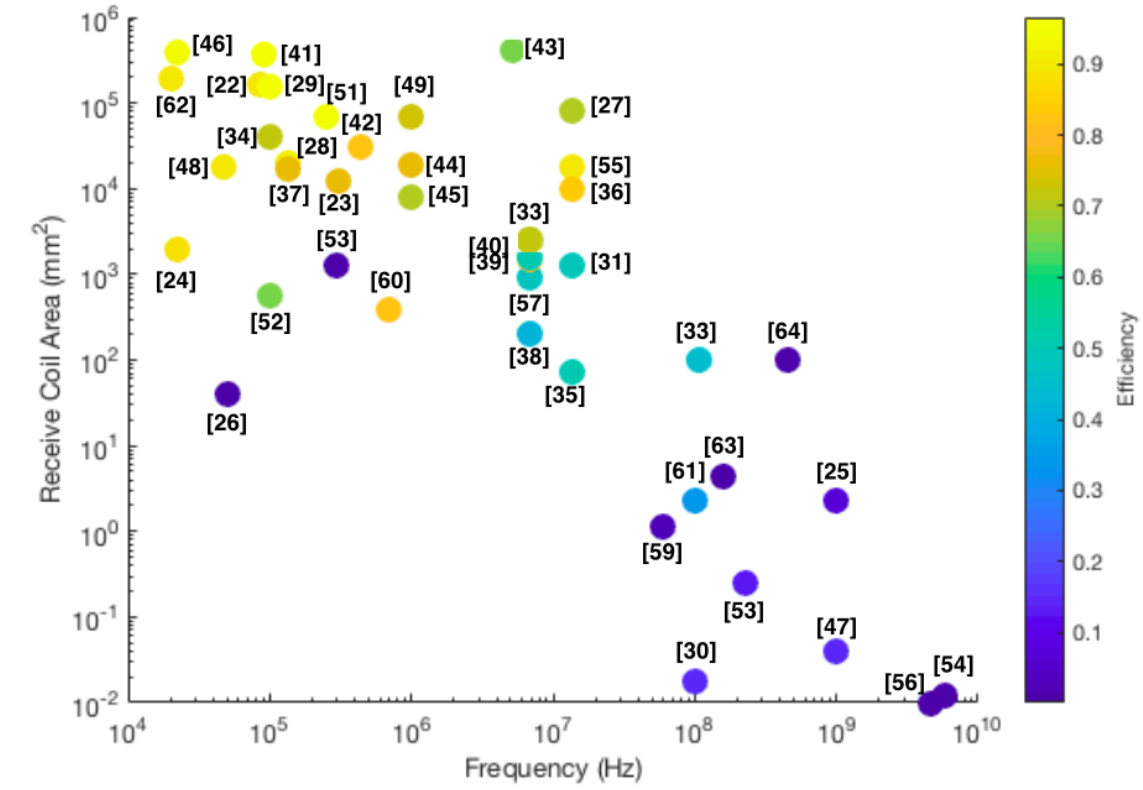

Figure 1.4: Correlation between frequency and coil area in prior literature

Table 1.2: Complete WPT Systems with Regulated Output

Reference	Frequency	Load Power	Transmission Distance	Coil Area	Efficiency	PDU
[23]	305 kHz	7.6 W	55 mm	12272 mm^2	76%	Buck
[35]	13.56 MHz	60 mW	3 mm	71 mm^2	50%	Regulating Rectifier
[27]	13.56 MHz	40 W	150 mm	80425 mm^2	70%	Buck
[30]	13.56 MHz	151 mW	140 μm	0.02 mm^2	15.1%	Buck

tegrated receiver for IoT applications. Finally, [30] demonstrates a complete WPT system with very small coil area but lower efficiency in an interposer level implementation. While higher efficiency is needed for this dissertation, this demonstrates the idea of an integrated WPT receiver similar to this dissertation.

1.4 Integrated Wireless Power Transfer Solutions

A key goal of this dissertation is to not only demonstrate RF near field coupling as an efficient and compact solution, but as an integrated solution as well. A comparison of some integrated near field coupling solutions is shown in Table 1.3. This table shows an ideal integrated solution to support the discussed low power IoT devices has not been previously demonstrated. The system in [40] is a good example of higher power, lower frequency near field coupling. The 5W output power is more than enough to support low power devices, the 51% efficiency is adequate, and the receiver hardware is integrated in a 2.5x2.5 mm^2 chip. The problem is this system is powered through a 1600 mm^2 receiver coil. The advantage of compact receiver for low power IoT applications is lost when the receiver coil area is so large. The works in [63] and [30] show that small area coil near field coupling has been previously demonstrated, but for different applications than the target of this dissertation. Zargham et al demonstrates a very compact and integrated WPT system for biological implants. This coil area (4 mm^2) is smaller than will be demonstrated in this dissertation, thus this work is more suitable for biological implants, as was the goal [63]. For IoT devices with few mW active power consumption, the output power and efficiency in [63] is not suitable. A chip-chip WPT system is demonstrated in [30],

Table 1.3: Integrated WPT Systems in Literature

Reference	Frequency	Load Power	Efficiency	Output Regulation	Coil Area
[40]	6.78 MHz	5 W	51%	Yes	1600 mm^2
[63]	160 MHz	1 mW	1%	Yes	4 mm^2
[33]	100 MHz	741 mW	85.6%	No	100 mm^2
[30]	13.56 MHz	151 mW	15.1%	Yes	0.02 mm^2

with the same efficiency limitation as [63] when applied to low power IoT devices and a transmission distance (140 mum) not practical either for these devices. The work of [33] comes the closest to meeting the design objectives, though the efficiency drops severely (to 44%) when using a 50Ω source as used in this dissertation. This implementation also has no form of output regulation. Thus there exists a gap in the current state of art for an integrated WPT solution for low power IoT applications, one this dissertation proposes to fill through integrated RF near field coupling.

One key contribution of this thesis is integrating embedded inductors into the WPT system with the PDU. By using advanced packaging technologies, embedded passive components may be utilized to decrease the influence of parasitics and to allow for custom design of component electrical parameters for improved utility in the WPT receiver. Also, embedded components increase the reliability of the integrated solution. There is not much prior work on integrating passives in WPT systems. The main work on embedded inductors in this dissertation is for the power inductor for the PDU. While embedded power inductors are rarely integrated in a WPT system, there have been numerous demonstrations of fabrication and design of embedded power inductors in academic literature in general.

The fabrication process should be simple, cheap, and easily integrated with planar PCB process. The most suitable fabrication method for this is to integrate magnetic layers on the power inductor through screen printing. Therefore, a key goal of this dissertation is to introduce a screen printing fabrication for magnetic core planar inductors with similar quality but less steps than previously demonstrated, and not only demonstrate the embedded inductor but integrate it in the complete WPT system for optimal efficiency. Since device size and cost are key design concerns for IoT hardware, the power inductors used

for the regulation become significant. Air core inductors are not area efficient enough for IoT design, and non planar inductor topologies require more complex fabrication than ideal for IoT design. Thus the focus of this review is on planar inductors with magnetic core as is suitable for an IoT architecture and fabrication. Kondo et al [65] demonstrates an in-silicon, packaged power inductor with a screen printed carbonyl-iron composite magnetic layer. The resulting inductor has very low area and DC resistance, but low inductance with corresponding mediocre inductance density. The work of [66] demonstrates another in-silicon spiral power inductor. The magnetic layer was created by manual pressing. The demonstrated inductor has good quality factor (21) and very good inductance density (47.8 nH/mm^2), and comparable efficiency when tested with the commercial converter as compared to the commercial converter with commercial inductor, but still lower efficiency than the compared surface mount technology (SMT) inductor. In fact, this dissertation will make a comparison using the same commercial converter as in this work, but with efficiency improvement. Also, the in-silicon fabrication is inherently more expensive than printed wiring board process, especially when integrating with the remainder of the IoT architecture. An example of PCB compatible inductor with screen printed magnetic layers is seen in [67]. Bang et al demonstrate a high quality factor (45) and high inductance density (33.1 nH/mm^2) packaged spiral inductor on FR4. The inductor was created using basic PCB build up process, with screen printed NiZn magnetic layer on the top and bottom. The fabrication is simple and creates quality packaged power inductors. However, the build up process adds extra fabrication steps over a basic 2 layer design. Furthermore, the double inductor pattern creates a large increase in DC resistance over the two power inductors previously discussed, leading to a potentially significant amount of inductor conduction loss even in a light load IoT application, whereas the previous two would have negligible inductor conduction loss.

Use of integrated inductor with buck converter has been previously demonstrated, but not in a WPT system. The integrated WPT systems in [38],[40], [61], and [75] demon-

strate integrated buck converter, but with SMT inductor. Previous work has demonstrated the design of integrated inductors for buck converters, including magnetic core inductor for GaN-based sychronous buck converter [68], planar air core inductor for 10 MHz buck converter [69], on-chip magnetic core inductor for 4 MHz two-phase converter [70], in-silicon inductor for 6 MHz buck converter IC [66], on-chip spiral inductor for 450 MHz buck converter [71], planar coupled inductor for tapped-inductor buck converter [72], in-package spiral inductor for four-phase buck converter [73], and ferrite-filled PCB inductor [74]. However, only in [68] is a comparison made to commercial inductor with meaningful efficiency improvement, as is the motivation of this work. Previous integrated WPT systems focus on improving the coil system, rectifier, and/or regulation scheme for improved efficiency, such as [25] and [27], but a secondary objective in this dissertation is to demonstrate WPT system efficiency may also be increased through improved power inductor design as well.

1.5 Dissertation Contributions

The main objective of this dissertation is to demonstrate RF near field coupling (RFNFC) is capable of achieving a superior combination of efficiency and receiver coil area compared to other WPT architectures. Specifically, this combination of low coil area and high efficiency is beneficial for light load applications, such as for IoT edge devices. While high efficiency WPT systems and small area RF near field coupling systems have been analyzed before, this combination has never been previously explored. Accordingly, this dissertation presents the design procedure and analysis unique to efficient, regulated, and integrated RF near field coupling systems. The main contributions of the dissertation are:

- The development of a system architecture that focuses on achieving high power transfer efficiency with small coil area for an integrated WPT receiver by using RF source frequency.

- Development of an efficiency analysis for low power, efficient RF near field coupling that demonstrates more robustness than simulation based methods
- Establishing the design process and considerations for a RF near field coupling system with regulated output, specifically identifying the differences in design of a high efficiency RF near field coupling system compared to other WPT systems.
- Identifying detuning high frequency effects and system level integration challenges unique to RF near field coupling, with solutions, most notably through a reverse power distribution network.
- Integration of packaging technology, such as magnetics and screen printing, into the system architecture to demonstrate a fully integrated receiver with embedded power inductor, leading to improved efficiency
- The fabrication and measurement of near field resonant inductive coupling WPT systems with superior combination of coil area and efficiency compared to state of the art.

1.6 Dissertation Organization

Chapter 2 discusses the system architecture developed for the RF near field coupling integrated receiver, and introduces the modeling and efficiency analysis used to guide the design. Chapter 3 presents the modeling and design process for each stage of the developed architecture, focusing specifically on a few designs and key considerations. Chapter 4 investigates layout and component selection challenges for RFNFC that arise from electromagnetic resonant frequency shifting effects, and also demonstrates a reverse power distribution network as a key part of the system for integrating RF-DC conversion with a PDU. Chapter 5 discusses the application of advanced packaging technologies for the receiver, specifically exploring screen printed magnetics in integrated power inductors. Chapter

6 details the complete system measurements, and provides a discussion of the merits of RFNFC as well as a comparison to state of art. Chapter 7 provides discussion on future work, specifically how ML algorithms and flexible hybrid electronics may be used to enhance the current work, as well as the conclusion.

CHAPTER 2
RF NEAR FIELD COUPLING ARCHITECTURE AND EFFICIENCY ANALYSIS

2.1 Introduction

A system architecture must be established to meet the goals of high efficiency, small coil area integrated WPT receiver with regulated output. The only requirements for the system are a single RF input and wireless power transmission via near field coupling to support mW load. This chapter describes the general system architecture used by all demonstrations in this dissertation, highlighting the innovations in system design due to the special needs of a high efficiency, high frequency system.

This chapter also introduces the efficiency analysis and design metrics for the developed architecture. The distribution of power losses in an efficient RFNFC system will be much different than any previously demonstrated WPT system. To design for optimal efficiency, the main sources of loss must be identified and estimated. This chapter discusses why the input voltage to the PDU in the system is dynamic with changing load. An iterative procedure is presented for calculating system efficiency in a RFNFC system, utilizing machine learning models to allow the iterative procedure to run without needing external simulations for each iteration.

2.2 RF WPT System Architecture

Some previously demonstrated WPT system architectures are shown in Fig. 2.1. Of particular note is the initial architecture for the proposed RF near field coupling system for the PDES Consortium at Georgia Tech (the primary source of funding for this dissertation research). In this initial architecture, several chips and power inductors were needed. With such an implementation, the area is increased and more potential for integration issues

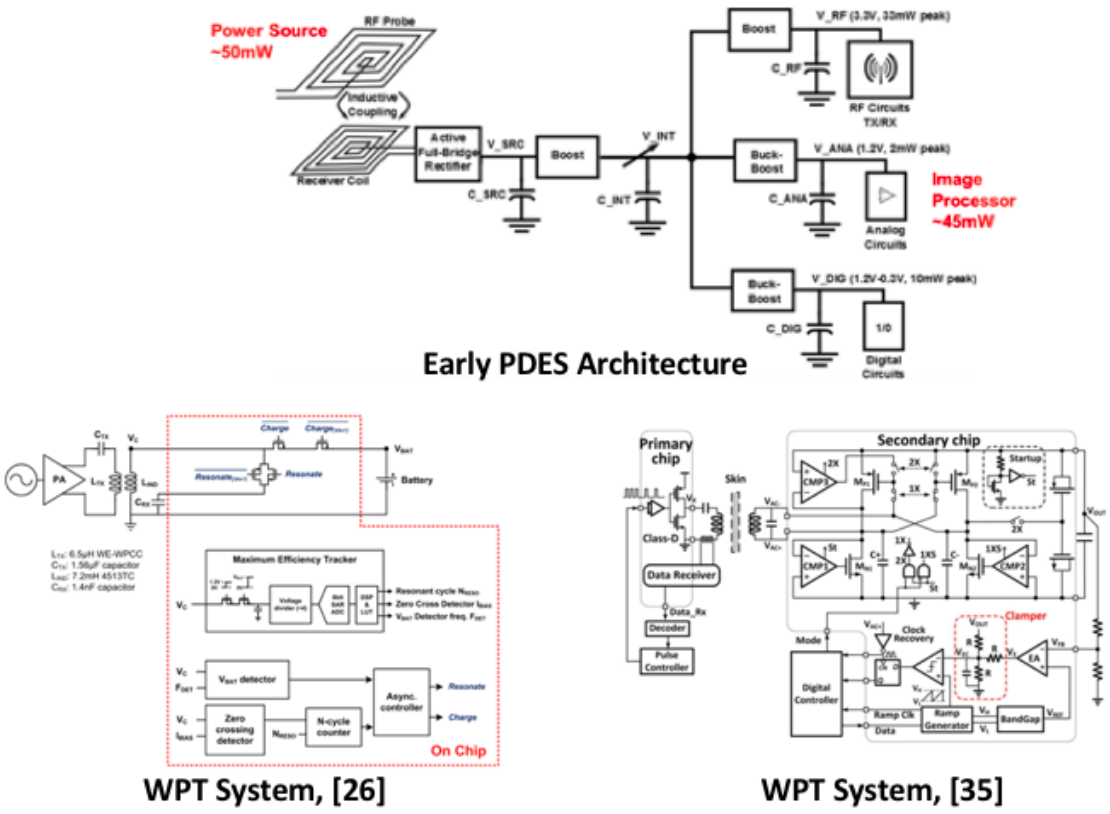

Figure 2.1: Some previous system architectures for inductive wireless power transfer systems

arise.

In response, a simpler system architecture needing only a single chip and single power inductor was developed, leading to decreased complexity and receiver area. The general system architecture developed for all work in this dissertation is shown in Fig. 2.2. A RF signal generator is used for the source in this dissertation, with 14.5 dBm (28.2 mW) maximum power output. This is followed by the near field coupling coil link. Every complete system demonstration consists of a single transmitter board and single receiver. This dissertation mainly examines high efficiency integrated receivers operating with a 2 coil link at transmission distances of 1-3 mm. However, a 4 coil link is also investigated to provide discontinuous power at greater transmission distance. In this instance, the transmitter board and receiver board will have 2 coils each integrated on separate layers, hence still a single transmitter and receiver board.

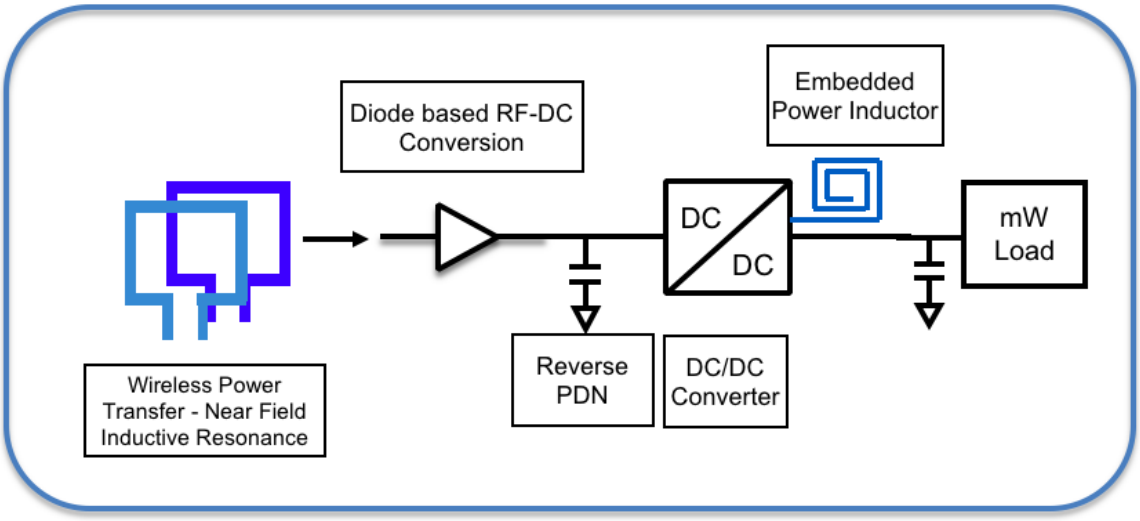

Figure 2.2: System architecture for RF near field coupling WPT system for mW load

A diode rectifier converts the RF power to DC. While other works utilize synchronous rectifiers/on chip rectifiers with optimal efficiency, innovating rectifier topology or process is not part of this dissertation. These works often design these rectifiers for very narrowly defined operating conditions, while this dissertation requires a more general rectifier solution suitable for testing many different designs and systems without having to overhaul the rectifier design in each instance. Standard diode rectifiers utilizing components off the shelf (COTS) are sufficient for the full system design and demonstration.

Because of the voltage smoothing capacitance requirements for the RF-DC conversion (pF scale) and the input capacitance requirements for the PDU (μF scale), a large parallel resonant peak is created between the two capacitors that may result in an unstable voltage supply to the PDU [76]. To solve this integration challenge, a reverse power distribution network (PDN) is designed to deliver a clean voltage supply to the PDU. The reverse PDN design, modeling, and demonstration for a variety of cases is provided in Chapter 4.

A PDU is the final stage in the system architecture. A PDU provides the regulated output necessary for a fully integrated WPT receiver. The PDUs used for measurement demonstrations in this dissertation are all COTS DC-DC converters. DC-DC converters

have been demonstrated in WPT systems previously, generally showing they decrease peak efficiency but maintain efficiency over a wider range of load [58]. While integrating DC-DC converters in a WPT system is common, this is seldom done for low power/high frequency systems, as illustrated by Table 1.1. The type of DC-DC converter depends on the design goals. For optimal efficiency, a switched inductor buck converter is the best option, as discussed later in this chapter. To increase the transmission distance, a boost converter is the best option. With a boost converter, a lower rectifier output voltage is acceptable, with full range of regulated output voltage available after the 'boosting' of this voltage. Accepting a lower rectifier output voltage enables the transmission distance to be increased. The load power range examined for this dissertation is 1-20 mW, mainly due to RF source power available in instrumentation. However, the design process and analysis presented in this dissertation scales to all load power in the mW range. PDU load voltages from 0.5-4V are used in this dissertation, but most of the focus is on output voltage of 1.2V or 3-3.3V, as is typically used for many compact devices.

In a switched inductor buck converter, the power inductor selection is a significant design choice. While not an explicit part of the system architecture, this dissertation will also examine the use of an integrated inductor, as opposed to commercial inductor, as a means to improve the efficiency and packaged reliability of the WPT system. So while using a power inductor is not novel from a system standpoint (every switched inductor regulator must have an inductor obviously), the approach of custom designing this inductor for improved efficiency in light load WPT system does have novelty.

2.3 Power Loss Modeling

The general equivalent circuit for a 2 coil, high efficiency system is shown in Fig. 2.3(a). A L-C matching network with values L_m and C_m match the source resistance R_s to the following circuit. The resonant capacitors C_1 and C_2 are integrated with the coils as SMT components. A series-parallel resonant capacitor network is selected, as has been demon-

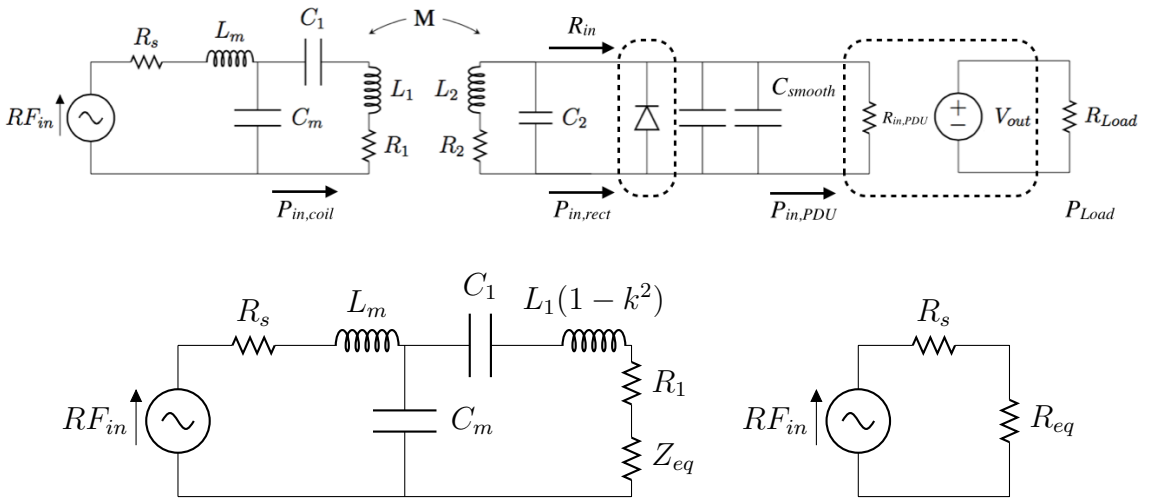

Figure 2.3: (a) WPT system circuit model (b) Equivalent circuit model with reflected impedance from receiver circuit and (c) Equivalent circuit model for source efficiency calculation

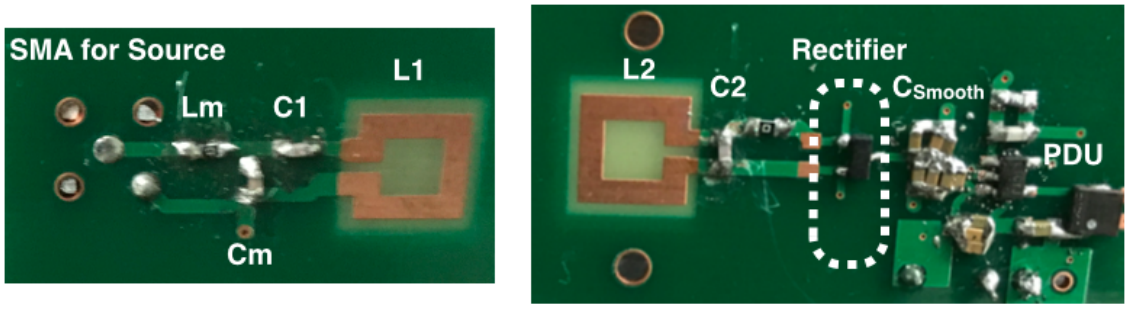

Figure 2.4: Components from circuit model on fabricated circuit

strated ideal for a WPT system with diode rectifier as it operates with high current at the transmit side and high voltage at the secondary side [77]. The coils L_1 and L_2 have resistance R_1 and R_2 with mutual inductance M. The reverse PDN is the network of capacitors labeled C_{smooth}, as voltage smoothing capacitors. A generic model is used for the buck converter, with input resistance $R_{in,PDU}$ and loading conditions of V_{out} and R_{Load}. To give perspective for these values in the actual RFNFC system, Fig. 2.4 shows a fabricated RFNFC system with the equivalent labeling from Fig. 2.3. For additional reference, all variable and component names used in the following analysis are provided in Table 2.1.

To design for optimal efficiency for a given transmission distance and coil size limita-

Table 2.1: Variables used in efficiency analysis

RF_{in}, P_{in}	Input RF Power
$P_{in,coil}$	Input power to transmit coil
$P_{in,rect}$	Input power to diode rectifier
$P_{in,PDU}$	Input power to PDU
P_{Load}	Output power
Z_{eq}, R_{eq}	Reflected impedance from receiver to transmit coil
L_1, L_2	RF coil inductance
L_{sw}	PDU inductor inductance
ω_{phase}	Source frequency (rad/s)
f_{rect}	Source frequency (Hz)
f_{sw}	PDU switching frequency
R_s	Source resistance
R_1, R_2	RF coil resistance
R_{in}	AC resistance seen at rectifier input
$R_{in,PDU}$	DC resistance seen at PDU input
R_{Load}	DC resistance at PDU output
R_{AC}	PDU inductor AC resistance
R_{DC}	PDU inductor DC resistance
R_{diode}	Diode forward resistance
D	PDU duty cycle
$V_{in,PDU}$	PDU input voltage
V_{out}	PDU output voltage
Q_1, Q_2	RF coil quality factors
k	RF coil coupling coefficient
M	Mutual inductance between transmit/receive coil
L_m, C_m	Transmit circuit matching network components
C_1, C_2	RF coil resonant capacitors
C_{smooth}, C_{RPDN}	Voltage smoothing/reverse PDN capacitors
Z_{C2}	Impedance of receiver resonant capacitor
n	Number of conducting diodes
V_f	Diode forward voltage
$\eta_{coil,loaded}$, η_{coil}	Coil efficiency
$\eta_{transmit}$	Efficiency of transmit circuit coil
$\eta_{receive}$	Efficiency of loaded receive coil
η_{source}	Source efficiency
$\eta_{rect,max}$	Max possible rectifier efficiency, after V_f
η_{buck}	PDU efficiency
$\alpha_{conductive}$	Attenuation of microstrip conduction loss per unit length
$\alpha_{dielectric}$	Attenuation of microstrip dielectric loss per unit length
ΔI_{pk-pk}	PDU inductor peak to peak ripple current
$P_{Loss,Vf}$	Diode forward voltage power loss
$P_{Loss,total}$	Sum of all power losses

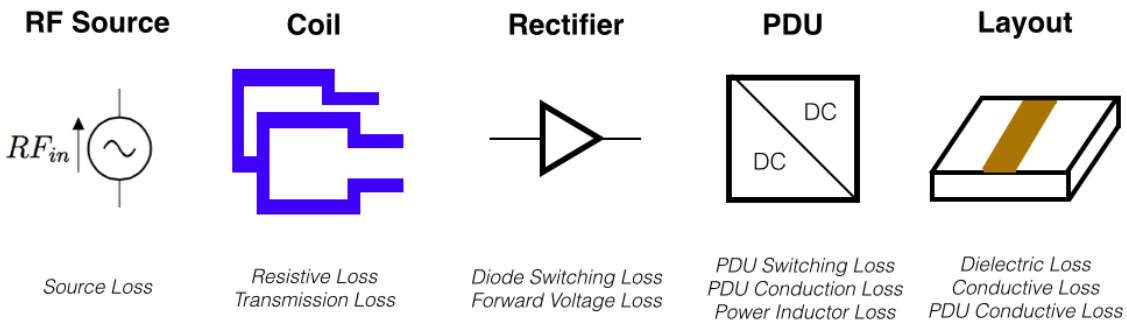

Figure 2.5: Classification of power losses in RF near field coupling system

tion, the sources of power loss in the architecture must be known. Much previous work has been done in this area for inductive WPT. In [78] and [79], robust general equations for determining the efficiency of a near field coupling link are provided, but these papers only focus on the coil link and do not provide the necessary analysis for a full system architecture. In [22], [40], [58], detailed efficiency analyses for full WPT systems with a similar system architecture (coil link, rectifier, PDU) are provided. However, these analyses are not applicable to a low power, RF system, as the distribution of rectifier losses are very different and the influence of the source resistance is more significant in RFNFC systems. This dissertation provides an efficiency analysis in this same spirit as these previous works, but specific to RF and mW load operation. A list of the relevant power losses are provided in Fig. 2.5. The following sections detail each of these losses through equations or simulation, and later chapters use this analysis to guide the design of the coil and to select appropriate components, such as the diodes and PDU.

2.3.1 RFNFC and Coil and Source Efficiency

Most RF near field resonant inductive coupling design primarily uses (1.1), the maximum power transfer efficiency (PTE), to evaluate the effectiveness of the near field coupling coils. Both transmission losses and coil resistive losses are accounted for in this equation. As the coupling coefficient decreases, the transmission loss increases. As the coil resistance increases, the quality factor decreases, also accounted for in (1.1). The maximum PTE

is useful because it simplifies design of the coils into two metrics (Q and k) for quick evaluation of a coil design using an electromagnetic simulator such as HFSS.

However, the maximum PTE assumes perfect matching and optimal loading. Depending on the loading conditions of the PDU, the PTE of the coils in practice will deteriorate. This is shown in the loaded coil efficiency (2.1), where α is the ratio of loading resistance of the coil to the reactance of the secondary resonant capacitor. R_{in} is the AC resistance seen at the input of the rectifier and is related to the input resistance of the PDU (and loading resistance of the rectifier) as given in (2.3), where n is the number of diodes 'on' during AC-DC conversion, V_f is the forward voltage of the diode, and $V_{in,PDU}$ is the PDU input voltage [80].

$$\eta_{coil,loaded} = \frac{k^2 Q_1 Q_2^2}{(1 + \frac{Q_2}{\alpha} + k^2 Q_1 Q_2)(\alpha + Q_2)} \tag{2.1}$$

$$\alpha = \frac{R_{in}}{|Z_{C2}|} \tag{2.2}$$

$$R_{in} = \frac{R_{in,PDU}}{2}(1 + \frac{n * V_f}{V_{in,PDU}}) \tag{2.3}$$

The loaded coil efficiency is the cascaded efficiency of the primary side efficiency and the secondary side efficiency. The primary side efficiency is a measure of how much of the power from the primary may be delivered to the secondary, and is shown in (2.4) [80]. It is simply a voltage divider of the transmit coil resistance and the equivalent (reflected) impedance of the receive coil to the transmit. When operating the receiving coil at the phase resonant frequency, the reflected impedance will be purely real. This is shown in (2.5), where (2.6) gives the phase resonant frequency.

$$\eta_{transmit} = \frac{Z_{eq}}{Z_{eq} + R_1} \tag{2.4}$$

$$Z_{eq} = R_{eq} = k^2 L_1 \omega_{phase} \frac{\alpha Q_2}{\alpha + Q_2} \tag{2.5}$$

$$\omega_{phase} = \sqrt{\frac{1}{L_2 C_2} - \frac{1}{R_{in}^2 C_2^2}} \tag{2.6}$$

The receive link efficiency is a measure of how much of the power received by the secondary coil is delivered to the load. This is shown in (2.7). When the load is fixed, this efficiency may only be improved by increasing the quality factor of the receive coil or by designing the coils to operate with different C_2 to lower α. Else, the optimal efficiency point may be found by changing the load resistance for minimal α.

$$\eta_{receive} = \frac{Q_2}{\alpha + Q_2} \tag{2.7}$$

The system may be designed for maximum power transfer or maximum energy efficiency. For a given source resistance, the maximum power that may be transferred to a load occurs when the load is conjugate matched to the source. All experimental work in this disseration uses a RF signal generator with a 50Ω source, thus to transfer the maximum power, the equivalent impedance of the coiling coils needs to be 50Ω. The equivalent circuit for the transmit circuit with reflected receiver coil impedance at the phase resonant frequency is shown in Fig. 2.3(b). The transmit coil leakage inductance may be negated by the resonant capacitor C_1, resulting in the circuit in Fig. 2.3(c). R_1, the resistance of the transmit coil, should be very small for optimal efficiency (less than 1Ω), thus may be neglected relative to the source impedance and R_{eq}. This gives the efficiency of the source, shown in (2.8), calculated as a voltage divider. That said, none of the designs in this dissertation use maximum power transfer, but rather maximum energy efficiency. If R_{eq} = 50Ω, the maximum power is transferred for a 50Ω source resistance with 50% efficiency. However, if R_{eq} is greatly increased, then the efficiency of the system can increase far beyond 50% [81]. Accordingly, as high efficiency is a key goal, maximum energy efficiency

is chosen as the key metric.

$$\eta_{source} = \frac{R_{eq}}{R_s + R_{eq}} \tag{2.8}$$

2.3.2 RF-DC Conversion

The remainder of the losses in system that operates at RF are either diode losses or microstrip losses. At low power, the forward voltage of the diodes is a significant source of efficiency loss. Even using Schottky diodes with a forward voltage of around 0.3V, the efficiency loss is significant. The maximum rectifier efficiency considering the forward voltage of the diodes is given as,

$$\eta_{rect,max} = \frac{V_{in,PDU}}{V_{in,PDU} + n * V_f} \tag{2.9}$$

where $\eta_{rect,max}$ is the maximum possible efficiency of the RF-DC conversion. The specific power loss from the forward voltage then is given as,

$$P_{Loss,Vf} = P_{in,rect}(1 - \eta_{rect,max}) \tag{2.10}$$

For low power applications, the current through the diodes will be small and the conduction loss can be neglected (very unlike higher power applications as shown in [22]). It should be noted the forward voltage loss is included as conduction loss by some sources. However, at RF the switching loss of the diodes becomes more significant. This can also be referred to as diode reverse recovery loss. The RF-DC conversion efficiency of a half-wave rectifier as a function of frequency is shown in Fig. 2.6. Each simulation was completed in Keysight ADS with the SPICE parameters for HSMS 282x series Schottky diodes, lossless traces, 500Ω load, and a LC matching network reoptimized for each frequency. Setup this way, the switching loss is the only variable loss in the simulation. Clearly, the efficiency drops by a few percent as the frequency increases, showing the switching loss is not negligible at RF operation.

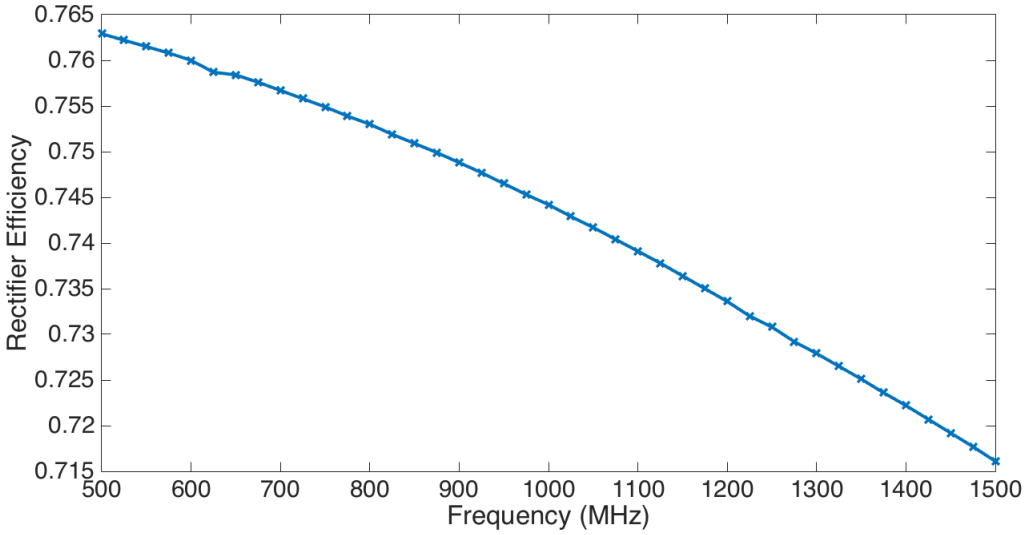

Figure 2.6: Efficiency of a half wave rectifier as a function of frequency

Most calculations of diode switching loss require transient waveforms of the diode current and voltage, and these measurements and calculations are very difficult to perform at RF [82]. To compare diode components more easily and re-evaluate the switching loss at different frequency, a way to estimate the switching loss as a function of the diode SPICE parameters is needed. The main contributor to switching loss is the diode junction capacitance C_j. This is confirmed by a series of ADS simulations as shown in Fig. 2.7, where the junction capacitance is varied for a 1 GHz half wave rectifier with 500Ω load. Again, the matching network is optimized for each simulation. As the junction capacitance increases, the switching loss increases.

In addition, the system parameters of input power P_{in} and rectifier load resistance $R_{in,PDU}$ affect the switching loss. These parameters affect the amount of voltage across the diode when it is 'off', thus increasing the switching loss at higher voltage as it becomes more difficult for the diode to reverse/recover. A series of ADS simulations was run for both a bridge and half wave rectifier in ADS, to generate data for efficiency as a function of these parameters. Each time, the circuit matching network was reoptimized. Then, each simulated efficiency was compared to the efficiency of the optimized circuit with the same

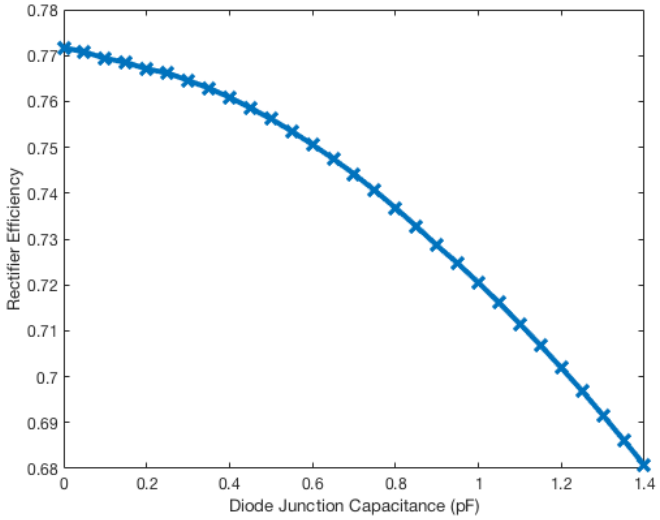

Figure 2.7: Efficiency of a half wave rectifier as a function of diode junction capacitance

parameters except with C_j = 0pF (no switching loss), to determine the amount of switching power loss. Different data must be generated for the bridge and half wave rectifiers, as the amount of voltage across the diode in the off state is different in each case, affecting the switching loss.

This data was used to develop machine learning model for the diode switching loss. This was accomplished in Matlab using a neural net, using a Bayesian regularization algorithm with the help of Ph.D. student Huan Yu. A comparison between the ADS simulated switching loss and the neural net predicted switching loss is provided in Fig. 2.8 for a bridge rectifier, for C_j = 0.7 pF, 1000Ω load, and P_{in} = 14.5 dBm. While the accuracy is not perfect, there is less than 0.1 mW difference, which translates to less than 0.5% efficiency difference. This demonstrates a simple and novel approach for estimating the diode switching loss in a RF WPT system without need for extra simulation.

The other losses are microstrip losses. This is exhibited with the microstrip lines in the both the transmitter circuit and the receiver circuit at the receiver coil and rectifier. These losses are either conduction or dielectric loss and shown respectively in (2.11) and (2.12), where σ is the conductivity of the microstrip line, Z_0 is the characteristic impedance of

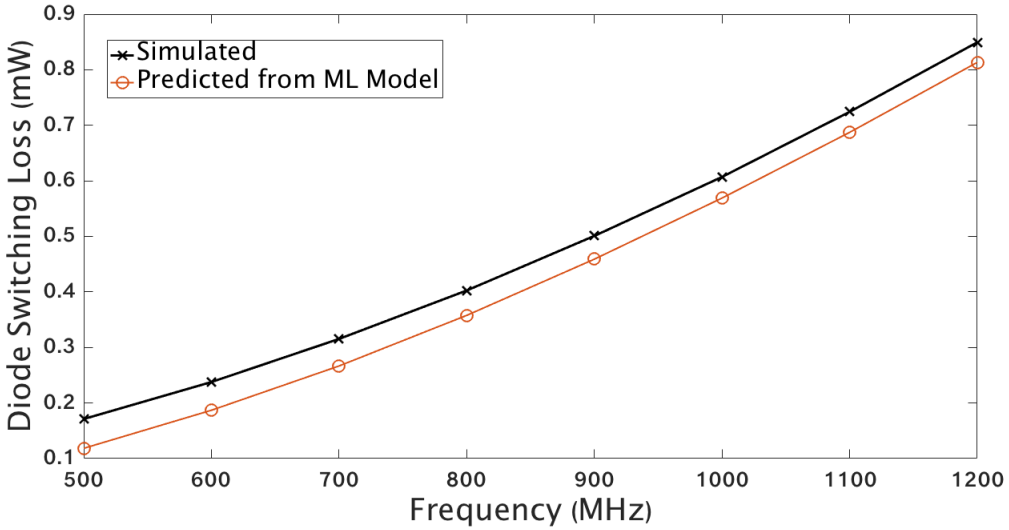

Figure 2.8: Comparison of diode switching loss from ADS simulation and machine learning model for HSMS 2820 diodes in RF near field coupling system

the line, W is the width of the microstrip line, ϵ_e is the effective dielectric constant, ϵ_r is the relative dielectric constant, and $tan(\delta)$ is the loss tangent of the substrate [81]. If the substrate parameters and dimensions of the microstrip lines are known, these losses may be calculated.

$$\alpha_c = \frac{\sqrt{\omega\mu_0/2\sigma}}{Z_0 W} \tag{2.11}$$

$$\alpha_d = \frac{k_0\epsilon_r(\epsilon_e - 1)tan(\delta)}{2\sqrt{\epsilon_e}(\epsilon_r - 1)} \tag{2.12}$$

2.3.3 PDU Input Voltage and System Efficiency Analysis Procedure

A key reason for using a buck converter as the PDU for high efficiency is it allows the rectifier to be operated at a higher intermediate load voltage, and then 'bucked' to the desired output voltage. This improves the efficiency from (2.9), especially for output voltages of PDU 1.2V or less. At small output voltage (such as 1.2V), the efficiency with rectifier alone is lower compared to using a PDU (small efficiency loss) and rectifier output operated at

3V, for instance. However, to properly design the coils the resistance seen at the load of the rectifier must be known, as this will affect the loaded coil efficiency from (2.1) and the source efficiency from (2.8). The relationship between the input resistance of the buck converter and the load resistance of teh buck converter is given in (2.13), where D is the duty cycle of the buck converter [83].

$$R_{in,PDU,lossless} = \frac{R_{Load}}{D^2} \tag{2.13}$$

However, this assumes a lossless converter. To account for the losses in the converter, (2.14) should be used. This adjusts the input power to the PDU to give the necessary output power, accounting for the buck converter efficiency. For a given range of converter output voltage and resistance combinations, the load resistance range of the rectifier (and thereby the coils) may be known.

$$R_{in,PDU} = \frac{R_{Load}}{D^2 \eta_{buck}} \tag{2.14}$$

The input voltage to the PDU is similarly increased by the efficiency of the buck converter, shown in (2.15).

$$V_{in,PDU} = \frac{V_{out}}{D \eta_{buck}} \tag{2.15}$$

The efficiency of the buck converter is degraded by inductor losses and conduction and switching losses in the converter. The inductor losses will be explored in greater detail in chapter V, but the general calculation of inductor DC ($P_{Ind(DC)}$) and AC ($P_{Ind(AC)}$) power losses for the buck converter can be estimated using,

$$P_{Ind(DC)} = R_{DC} * I_{Load}^2 \tag{2.16}$$

$$P_{Ind(AC)} \approx \frac{R_{AC} \Delta I_{pk-pk}^2}{12} \tag{2.17}$$

$$\Delta I_{pk-pk} = \frac{(V_{in,PDU} - V_{out})D}{f_{sw}L_{sw}} \tag{2.18}$$

where R_{DC} is the DC resistance of the inductor, I_{Load} is the load current, R_{AC} is the AC resistance of the inductor, f_{sw} is the switching frequency, ΔI_{pk-pk} is the maximum ripple current, $V_{in,PDU}$ and V_{out} are the input and output voltages for the converter, L_{sw} is the inductance of the power inductor and D is the duty cycle. While analytical forms of the calculation of the buck converter switching and conduction losses exist, device specific capacitances are not known for the devices used in this thesis, so simulators will be relied on instead to determine the contribution of these losses. Similar to the diode switching loss, a ML model is developed for the losses. The PDU efficiency was simulated in Linear Techonology LTSpice as a function of $V_{in,PDU}$, V_{out} and load power P_{Load}. A machine learning model was trained with the data with a gaussian process regression algorithm with the help of Ph.D. student Hakki Torun. A comparison of the PDU efficiency (just considering conduction/switching loss, no inductor loss) from LTSpice simulation and the ML model based on simulated data is shown in Fig. 2.9. At different operating points, the ML modeled loss is within 2%, and typically within 1%, of the LTSpice efficiency. This is tolerable error for the PDU switching/conduction losses, as these losses comprise only a small portion of the overall loss in the entire system. In contrast, like the diode switching loss an extra simulation is not needed when a new load/circuit is considered, and all losses may be evaluated concurrently, representing a key benefit from using the ML model.

The remaining missing link is that the input voltage to the PDU is not actually known from the above equations. From (2.14) and (2.15), for a given load and converter efficiency, $R_{in,PDU}$ and $V_{in,PDU}$ may take an infinite amount of values (along a line) to satisfy these equations. This leads to one of the quirks with using a PDU in a power driven (opposed to voltage driven) WPT system - the input voltage to the PDU will regulate to the minimum necessary voltage to supply the load, when the PDU output voltage is less than the input voltage. The voltage will be the minimum necessary to supply a given load, as this will be

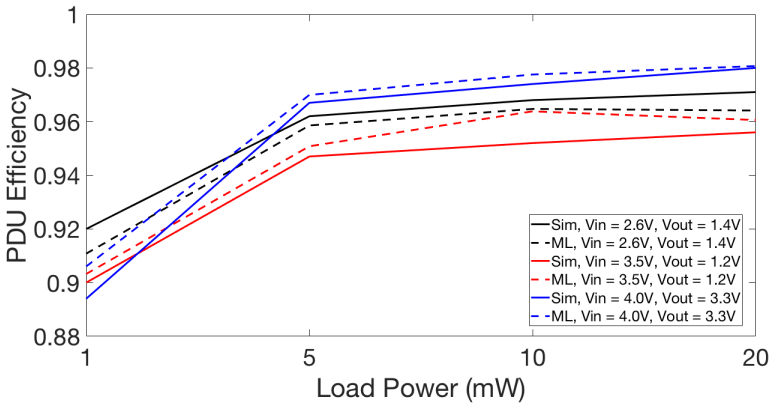

Figure 2.9: Comparison of PDU efficiency from LTSpice simulation and ML model

the highest efficiency point for the buck regulator (as opposed to increased voltage input, as increasing the conversion ratio will lower the efficiency). However, the input voltage and corresponding input resistance will increase to whatever point necessary to improve the WPT system efficiency to supply the load. As the values of the input voltage to the PDU and $R_{in,PDU}$ change, the source, coil, and rectifier efficiencies will be altered as shown in earlier equations. For a given input power, the PDU will set $V_{in,PDU}$ to the value which matches the output power of the rectifier to the input power necessary at the PDU to supply a given load. Essentially, the converter nautrally adjusts the input voltage to match the PDU input power times the converter efficiency to the load power. If no value of $V_{in,PDU}$ accomplishes this, insufficient power is provided and the input power needs to be increased or the load power decreased. Since the circuit is powered with a controlled power source, and not a controlled voltage source, it is possible more power is available to the input of the PDU than is necessary. What happens in this case? The input voltage to the PDU will rise, as the PDU will attempt to dissipate this power by increasing the voltage conversion ratio and thereby decrease its efficiency. It also happens that if the voltage is increased beyond the optimal efficiency point, the input resistance to the PDU will also increase and start to decrease the efficiency of the WPT system, helping to match the power in the case when the efficiency is too high for a given load. If the input power continues to increase, the input voltage will continue to increase until it exceeds the maximum operating input voltage for

the PDU. At this point, the PDU responds by releasing the magic smoke. This has been confirmed multiple times with different PDU chips over the course of experimental work for this thesis, never intentionally.

As an example of this power matching, if 10 mW power is necessary at the buck input to power a certain load, the input voltage could be 2.5V and the load resistance 625Ω to satisfy this. However, the corresponding calculated efficiency for the source, coil, and rectifier might be too low to supply 10 mW at this rectifier loading conditions. Instead, the converter input could be 4V with 1600Ω load resistance. At these rectifier loading conditions, the WPT system efficiency might be sufficient to supply 10 mW at the converter input. If the input power at the PDU is increased to 15mW, 5 mW of power needs to be dissipated. The PDU responds by increasing the input voltage until the power is matched. And if it can't be matched, the PDU will be overloaded and stop working. For this dissertation, the only power of interest is the minimum input power necessary to power a given load, as this will be the maximum efficiency point for that load.

Therefore for a given PDU output, the efficiency analysis procedure must determine when there is a combination of $V_{in,PDU}$ and $R_{in,PDU}$ that can supply enough power to the input of the PDU for a given RF input power. This procedure is shown in Fig. 2.10. This procedure determines the minimum P_{in} necessary to supply a given load V_{out}, R_{Load}, which is by definition the optimal efficiency point. This process starts at the minimum possible P_{in} (assuming 100% efficiency), then incrementally increases $V_{in,PDU}$ to determine if there is sufficient power available at the input to the PDU to power the specified load, using the aforementioned analysis. If not, P_{in} is also incrementally increased until a minimum combination of P_{in} and $V_{in,PDU}$ is found that can power the load, from which the efficiency can be calculated as P_{Load}/P_{in}. There is some error due to the discrete nature of the iterative process, but this procedure appropriately accounts for the dynamic nature of the PDU input voltage to calculate the system efficiency.

This is also why a model for the diode switching loss and PDU losses is vital - it

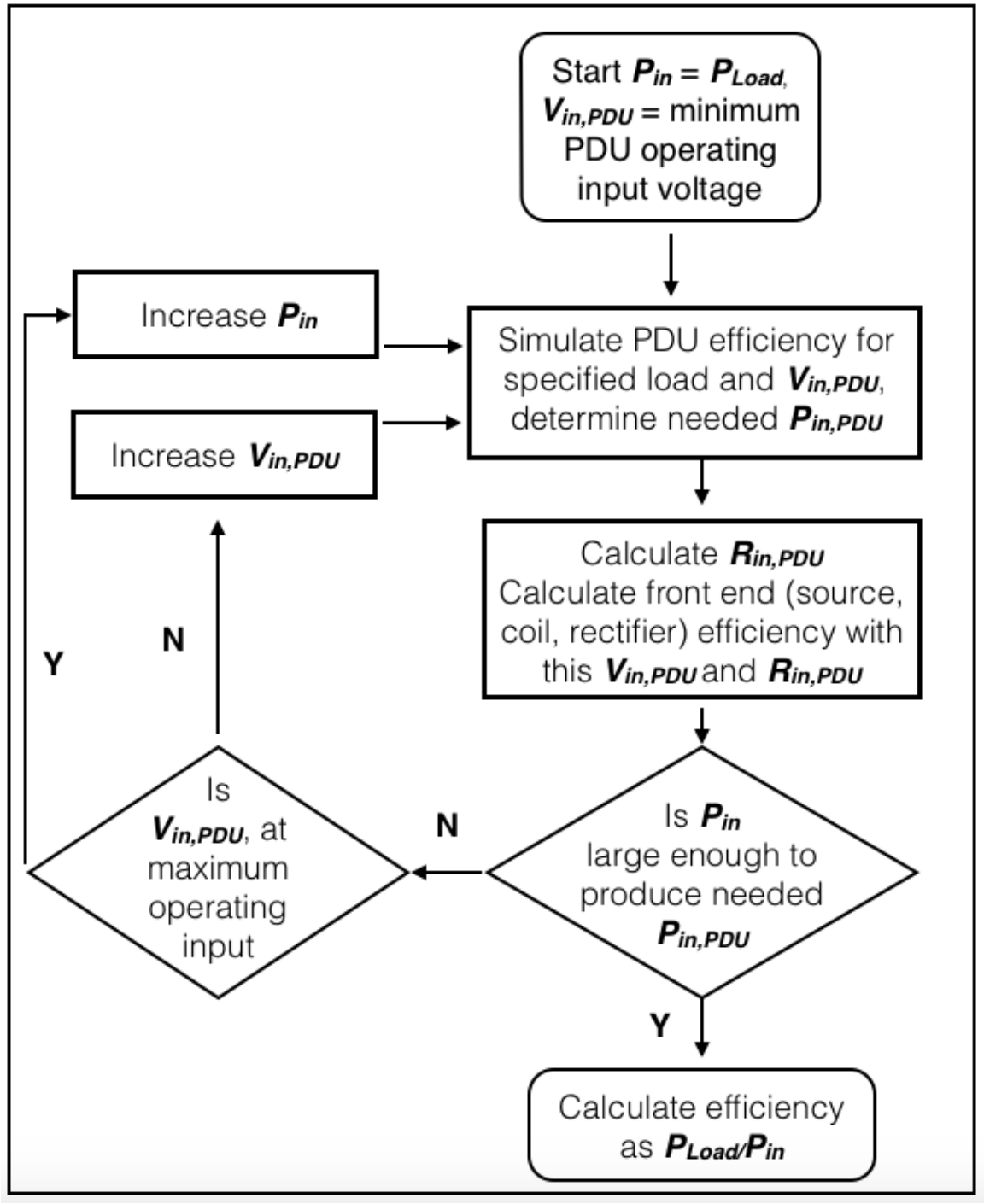

Figure 2.10: Procedure for determining efficiency for regulated RFNFC system

eliminates the need to run numerous extra simulations for each iteration of this procedure. Each iteration of the procedure uses a new combination of $V_{in,PDU}$ and P_{in}. As $V_{in,PDU}$ changes, so will $R_{in,PDU}$. As each iteration has a unique combination of P_{in} and $R_{in,PDU}$, the diode switching losses will change for each calculation. In addition, the PDU losses vary considerably with each new $V_{in,PDU}$. Thus, by not needing a new simulation to find a new value of these losses for each iteration, the machine learning model enables much faster efficiency analysis.

In this thesis, often just the coil plus rectifier circuit will be examined, without the PDU. The individual sources of loss are calculated the same, but in this case the efficiency is determined by solving a quadratic equation of the rectifier output voltage to determine what value matches the input power minus the calculation of losses to the rectifier load power.

Because the system operates with a controlled power source, when the PDU output voltage is above the minimum input operating voltage for the PDU (2.5V for the LTC3564 for example), the PDU powers itself from its output. Using a form of bootstrapping, in this mode of operation the PDU input voltage and the output voltage are equal. In this state, continuing to increase the input power will not change the input voltage, unlike the previously discussed situation when V_{out} is less than $V_{in,PDU}$. While the losses of the coil + rectifier front end are calculated the same, the PDU losses change. First, because no 'bucking' is actually needed the inductor switching is much less, approximated using ripple current with input voltage 50-100 mV greater than the output. Second, the PDU losses are harder to estimate, through simulation or measurement. The LTC3564 does not provide a way to externally bias the bootstrap circuit, so the losses from the self-powering cannot be calculated through measurement. Thus simulated losses must be relied upon, with efficiency around 99% in this mode of operation typically simulated. While this is certainly greater efficiency than received in practice, the PDU losses are a small portion of the overall system losses thus the error will not affect the design of the system front end. As

discussed in Chapter 6, by assuming variable $V_{in,PDU}$ and using the efficiency analysis as normal (with revised inductor loss), better correlation to the system efficiency is achieved compared to calculating the losses with fixed $V_{in,PDU} = V_{out}$.

This efficiency analysis is meant to be used as a tool guiding the design than a perfect predictor of the system efficiency. Standard simulation based methods, using ADS, HFSS, LTSpice, etc., to design separate subsystems does not properly account for the interdependence of each subsystem on various other subsystem parameters. One good example of this is the expanded form of the source efficiency, given as

$$\eta_{source} = \frac{k^2 L_1 \omega_{phase} \frac{\frac{V_{in,PDU}^2 R_{Load}}{\frac{V_{out,PDU}^2 \eta_{buck}}{2}(1+\frac{n*V_f}{V_{in,PDU}})}}{|Z_{C2}|} Q_2}{R_s + k^2 L_1 \omega_{phase} \frac{\frac{V_{in,PDU}^2 R_{Load}}{\frac{V_{out,PDU}^2 \eta_{buck}}{2}(1+\frac{n*V_f}{V_{in,PDU}})}}{|Z_{C2}|} Q_2} \quad (2.19)$$

This equation illustrates that the source efficiency is dependent on several characteristics that aren't intuitive, such as the buck converter efficiency, the diode forward voltage, and the receiver resonant capacitance value. Capturing these complex relationships between the subsystems is very difficult, if not impossible, with simulation based methods. Thus the design of the complete system, specifically with component selection and coil design, uses the developed efficiency analysis to better understand and consider the effects of the various system parameters on system efficiency.

However, while this efficiency analysis captures how the system efficiency trends with different design parameters, the use of several approximations prevents it from being an extremely precise system efficiency predictor in all cases. Some design variables may be tuned to help model to measured correlation as noted. Some of these approximations and

limitations are listed below.

- Matching losses are unaccounted for. The matching network is utilized to improve efficiency, while the efficiency analysis assumes there are no matching losses. Many measurements in this dissertation occur over a large resistance range with the same matching network, where a perfect match across all these loads is impossible. As such, part of the load resistance range will have a lower efficiency than predicted, especially at larger values of R_{Load}. This effect is more pronounced with PDU absent, as the PDU functions to keep a more stable value of $R_{in,PDU}$ to the rectifier.

- In addition, the impedance matching will lead to much improved efficiency in cases where R_{eq} is very small, such as at increased transmission distance and/or small load resistance. When R_{eq} is below 50Ω, even by using maximum power transfer matching, the efficiency will be much improved over what the efficiency analysis predicts. The efficiency analysis still functions as a better design guide, but must be used in conjuction with other design processes and tools for matching the design to achieve optimal efficiency.

- The inductor losses must be mitigated, especially at low load power. As the selected PDUs operate with complex operation at the load power examined, they are designed specifically to diminish inductor losses compared to what would typically be predicted. Based on LTSpice simulations, when the inductor loss from (2.17) is halved, the resultant calculated PDU efficiency much more closely matches the LTSpice simulated efficiency, thus that adaptation is made for the calculated efficiency. As the best resistance value is difficult to estimate exactly, it may be tuned to help modeled to measured efficiency correlation within reasonable values.

- $V_{in,PDU}$ functions much more complexly than assumed. While the predicted PDU input voltage closely matches the measured for some load power, at other times the input voltage behaves very strangely, especially under 5 mW. This will be shown in

a couple of measurements in later chapters, but in one instance a PDU settles at 1.9V PDU input across a range of 3-4 mW, though the minimum operating input voltage is 2.4V for this PDU. Interestingly, the measured efficiency in these cases still trends very similarly with the calculated efficiency, though the actual input voltage behaves strangely in what is attributed to device specific peculiarities.

- The analysis assumes the PDU operates in pulse frequency modulation 'burst' mode, as is the mode of operation for the LTC3564 at light load. While the TPS62615 may use single or multi pulse, the converter switching and conduction losses are not a major portion of the power losses. In addition, there is not much control over these in the design (as off the shelf components are used), thus the use of simulated losses offer an acceptable approximation.

- The efficiency analysis is very sensitive to the coil characteristics, such as L_1, k, and Q_2, so any discrepancies between simulation and the fabricated coils hurts accuracy

- P_{in} is discretely increased in analysis and measurement, with corresponding loss in accuracy

- Diode switching loss and PDU losses are calculated with a ML model, based off simulated data. This results in sufficient accuracy to understand how these losses affect trends in subsystem efficiency, but will not result in a perfect estimation of these losses.

2.4 Summary

This chapter examined the development of a system architecture for a RF WPT system with regulated output, detailing the improvements over previous examples. In addition, this chapter discussed the efficiency metrics developed to guide the design of the RFNFC systems discussed in later chapters of this dissertation. The efficiency analysis improves

upon previous work by classifying and quantifying losses tailored specifically to low power, high frequency WPT systems, utilizing machine learning models for certain power losses to decrease the number of external simulations needed to calculate efficiency, and using an iterative system efficiency analysis procedure to model the dynamic nature of the input voltage to the PDU.

CHAPTER 3
SUBSYSTEM DESIGN

3.1 Introduction

The previous chapter introduced the system architecture and the modeling of the power losses relevant to a low power, RFNFC system. The system architecture consists of a mW RF source, near field coupling coil link with matching network, diode rectifier, reverse power distribution network, and DC-DC converter. Equations for the various power losses and efficiency analysis procedure were provided. The importance of system level design was also discussed.

This chapter presents specific design examples. All modeling and simulation work for each of the subsystems are included here. This chapter uses the modeling and power loss equations introduced in the prior chapter to dictate design choices such as component selection, rectifier topology, and coil geometry. Various pieces of the system architecture are demonstrated through simulation and measurement through several designs, focused on low power applications. The design process is described, explaining how the design approach for RF near field coupling systems varies compared to other WPT systems. The designs developed in this chapter will be further evaluated in chapter 6 as complete system demonstrations.

3.2 Design Identification

Because of the scope of this dissertation, different designs are examined to demonstrate different aspects of the approach, modeling, or dissertation objectives. Each system uses one of four different coil designs, in varying combinations. The geometry parameters for each of these coils are given in Table 3.1, and the design process to choose this geometry

Table 3.1: Coil Geometry and Parameters

	l (mm)	w (mm)	g (mm)	L (nH) @ 1 GHz	C_{par} (pF)
$coil_1$	5.75	1.31	0.58	6.06	0.484
$coil_2$	7.25	1.65	0.73	7.95	0.563
$coil_3$	7.5	1.5	2.0	9.72	0.452
$coil_4$	8	1.1	0.80	14.19	0.534

is provided in the following section. For systems, either a half wave or bridge rectifier is used. Systems are designated by the rectifier type and coils used. $Half_{2,2}$ for instance uses a half wave rectifier and $coil_2$ for both the transmit and receive. $Bridge_{4,1}$ would use a bridge rectifier with $coil_4$ for the transmit and $coil_1$ for the receive.

In addition, providing full simulation and design details for each of these designs would make the body of this dissertation needlessly long. Significant design approaches, design decisions, subsystem measurements, and simulation details only are included in this chapter.

3.3 Coil Design

3.3.1 Selection of Coil Geometry

To demonstrate an integrated solution, the RF coils for this design are integrated on the same substrate as the rest of the transmitter or receiver circuit (instead of off board coils often seen in WPT demonstrations). Various coil implementations have been previously demonstrated, including wirewound [58], planar spirals [33], and planar rings [25]. For RF operation, single turn rings give the best maximum PTE, as shown in Fig. 3.1. The coil geometry for all designs in the dissertation has the parameters shown in Fig. 3.2. In the Fig. 3.1 HFSS simulation comparison, 1, 2, and 3 turn planar inductors on FR4 are compared, with l = 7.5mm, w = 1mm for the 1 turn coil, l = 5mm, w = 0.5mm for the 2 turn coil, and l = 4.5mm, w = 0.25mm for the 3 turn coil. The Q and k are significantly degraded when more than one turn is simulated. Because the parasitic capacitance is much greater in the multiple turn coils (from the interwinding coupling), the self resonant frequency is much lower. This causes an artificial increase in k as frequency increases as shown in Fig. 3.1.

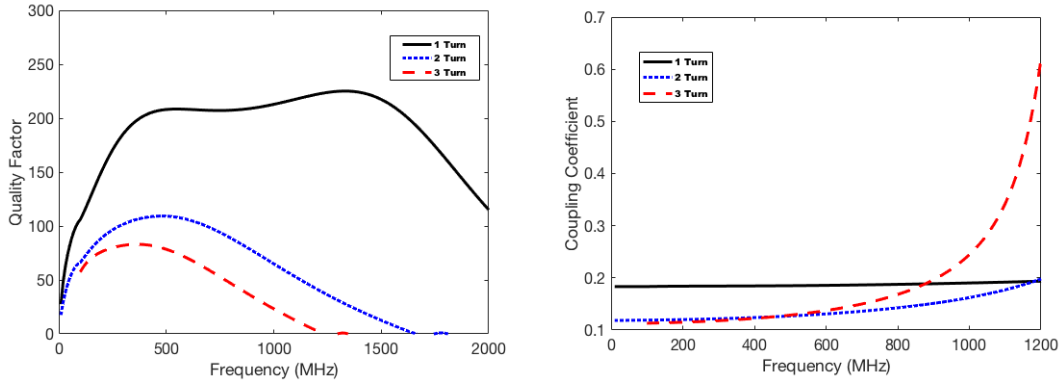

Figure 3.1: Comparison of Q and k for 1, 2, and 3 turn RF coils

To keep coil area small and prevent the inductance from increasing and further lowering the self-resonant frequency, smaller line width must be used when more turns are added. This greatly increases the resistance and decreases the quality factor at RF. Because of this, single turn rings are used for all designed coils.

Both the transmit and receiver coils are designed with the same geometry. However, area is only a consideration for the receiver coil. An HFSS model for the coils is shown in Fig. 3.3, with 1 oz copper on FR4 substrate. One important geometry and modeling note for the coils is a void is added in the ground plane directly beneath the coil (with slightly larger area). This leads to increased inductance, and therefore greater efficiency, for the coils. The simulated magnetic fields, viewed from the side, for the $coil_{2,2}$ link is shown in Fig. 3.4. HFSS is used for all full wave 3D electromagnetic simulations in this dissertation.

3.3.2 Coil Parameter Modeling

Before introducing the coil design, a couple of notes should be made about the parameters used in the calculated efficiency analysis from Chapter 2. First, the HFSS simulated quality factors change greatly with the transmission distance, shown in Fig. 3.5. This simulation sweep shows $coil_4$ simulated Q at 1 GHz as a function of transmission distance. One reason for this variation is the capacitive coupling between the coils increases as transmission distance decreases, decreasing the self-resonant frequency and artificially increasing the

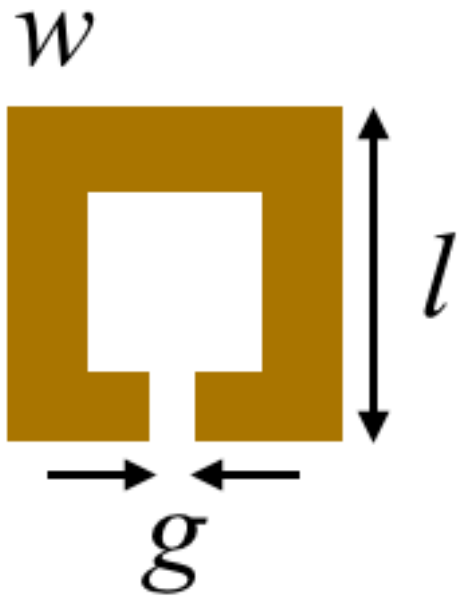

Figure 3.2: Coil geometry for this dissertation, with side length l, line width w, and gap distance g

resistance of the coil. The reason it is artificial is that the coils are designed to operate at resonance, thus operating closer to the self-resonant frequency does not degrade efficiency as much the HFSS simulation would suggest but rather lessens the extra capacitance needed from the resonant capacitor. While the Q does degrade some in practice as distance shortens, using this simulated value results in large efficiency underestimation when compared to measurement. The most accurate calculated efficiency, compared to measurements, occurs when using the quality factor of the coils when not closely coupled to the other coil. Therefore, the quality factor of each coil is simulated alone, with this value used in all efficiency calculations, with some slight tuning allowed.

Second, the microstrip feedline on the transmitter side needs to be modeled to calculate the source efficiency. The extra inductance from the microstrip feed line also adds to the reflected impedance to the transmit coil and correspondingly increases the source efficiency. Microstrip line length is appoximated and simulated in HFSS for each transmit coil used, and this value added to L_1 for use in efficiency calculation. By doing this, much better

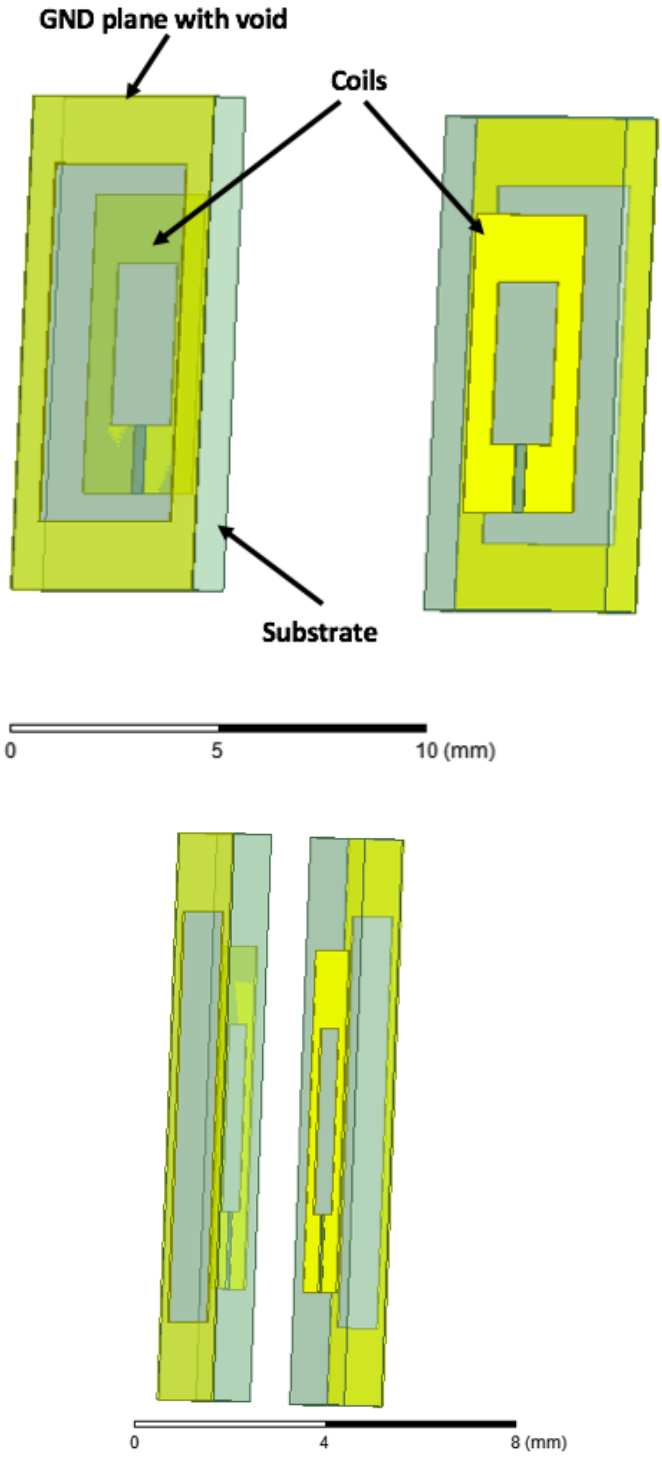

Figure 3.3: HFSS model of coils ($coil_2$) at (a) 10 mm transmission distance and (b) 2 mm transmission distance

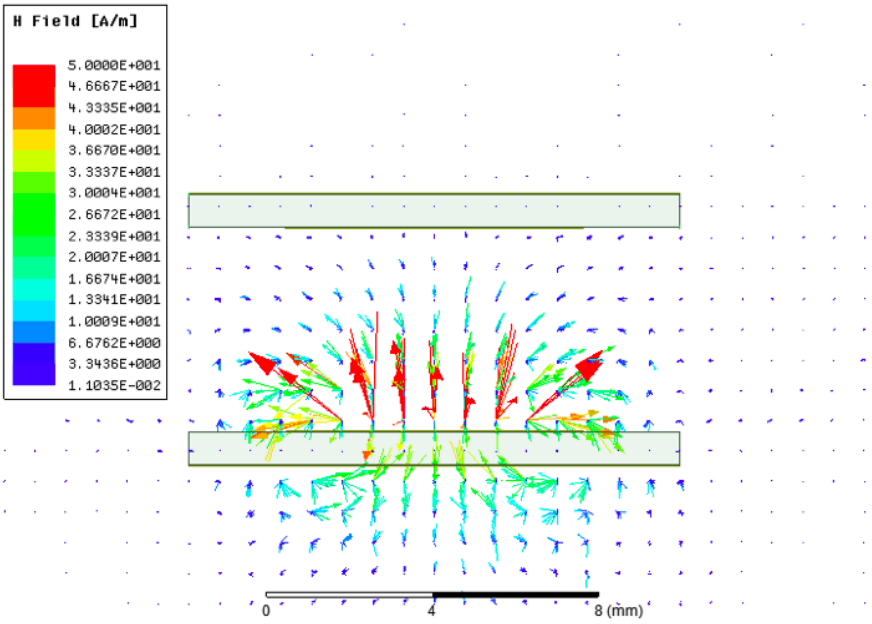

Figure 3.4: Simulated H-field of $coil_{2-2}$ at 5 mm transmission distance

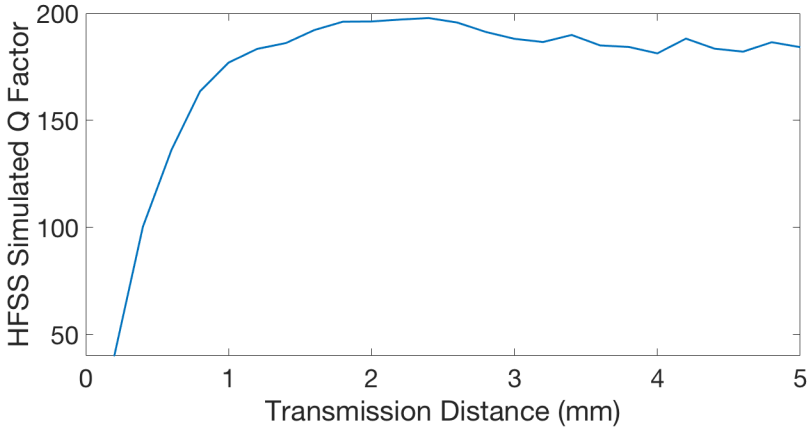

Figure 3.5: Effect of the transmission distance on the simulated Q factor for $coil_4$ geometry

agreement between the calculated and measured efficiency is achieved.

3.3.3 Coil Design and Efficiency

There are three metrics to analyze the effectiveness of the coils: the maximum PTE (1.1), the loaded coil efficiency (2.1), and the source efficiency (2.8). The maximum PTE is the least effective method, as it is system agnostic, but it allows for the quickest evaluation of a design. The loaded coil efficiency (referred to as just the coil efficiency going forward) and the source efficiency are the more accurate metrics for evaluating the coils for use in a specific system.

The maximum PTE is used first to quickly evaluate a wide range of coil geometry to narrow the focus of the design. For example, if a coil geometry only has 60% max PTE, then there is no need to further consider that geometry. An HFSS simulation sweep was performed for various square coil geometry at 2mm transmission distance, with the same geometry for both coils. The k, Q, and maximum PTE as a function l and the ratio of w/l at 868 MHz is shown in Fig. 3.6. For this sweep, g is set to l/10. The coupling coefficient is increased at larger l, and for intermediate line width. For all l, the coupling coefficient is largest when the line width is one quarter of l (2*w/l = 0.5). In contrast, Q is the largest at smaller l and thicker line width. With very small coil size and thick lines, the resistance is very small even at RF operation. Using these values to calculate the maximum PTE, Fig. 3.6 shows the design of the coils should avoid using very small line width (less the 10% of l). For the receiver coil, the maximum l considered is 10mm. While good maximum PTE can be achieved with larger l as well, a key design goal is to minimize receive coil area. If the same efficiency can be achieved with smaller coils, then no reason exists for considering l above 10mm.

While the maximum PTE suggested the best efficiency could be obtained with large w coils, when factoring in the load resistance the optimal geometry changes. Smaller w may demonstrate better coil efficiency, shown in Fig. 3.7. This is because smaller w increases

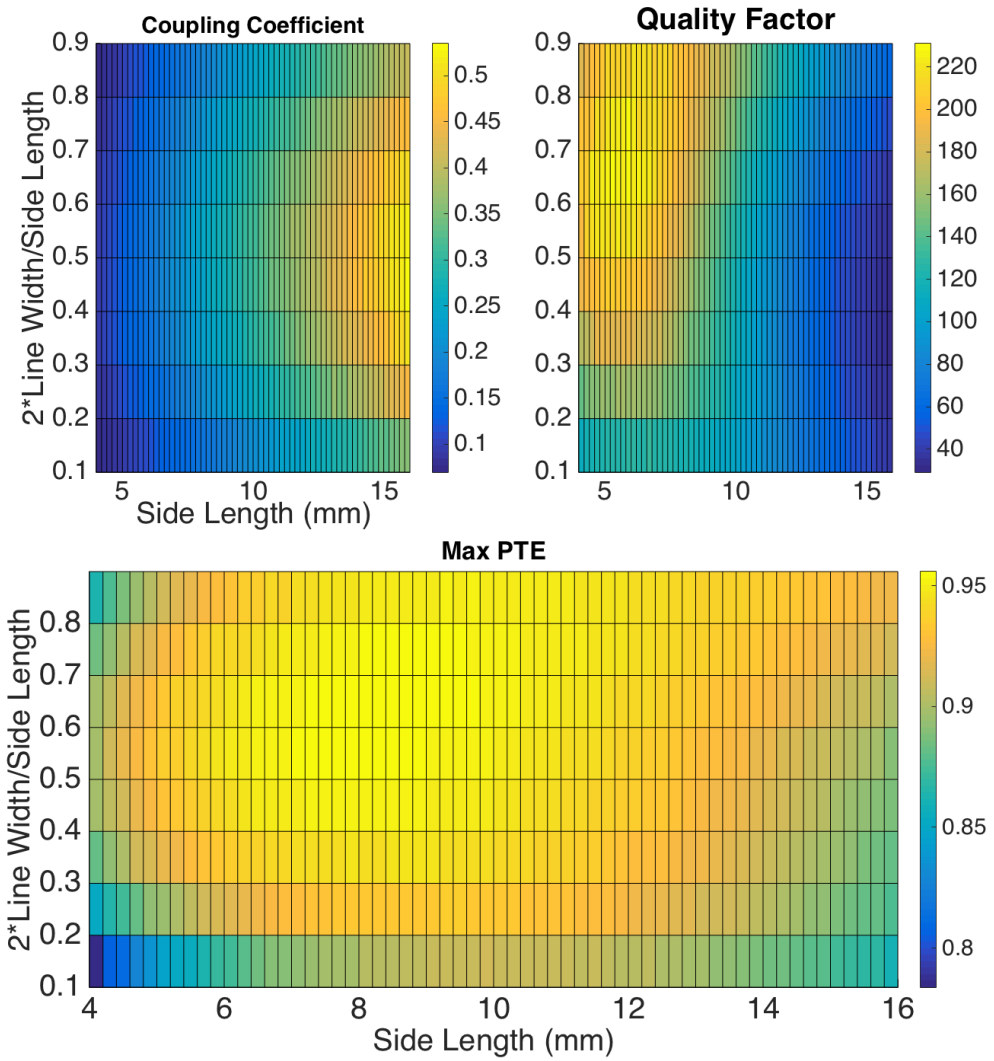

Figure 3.6: (a) Plot of how k and Q vary with coil geometry and (b) plot of how the maximum PTE varies with coil geometry

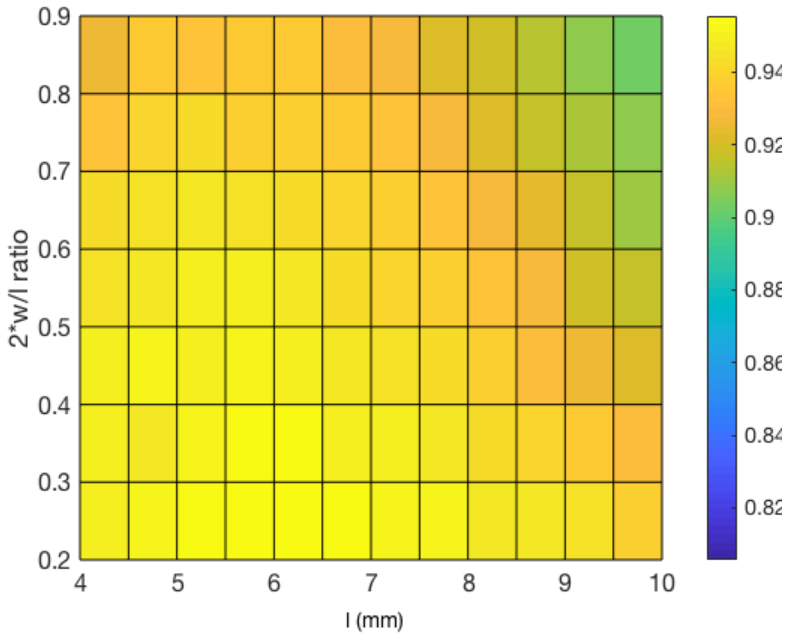

Figure 3.7: The coil efficiency for $coil_{3-3}$ link with R_{in} = 1000Ω at 1 GHz

the inductance. While the quality factor decreases, a smaller value for C_2 is used for the same 1 GHz resonant frequency, decreasing α and thereby increasing the coil efficiency from (2.1). A similar effect is seen on the source efficiency. In Fig. 3.8, the effect of the geometry on the source efficiency is shown for 850 MHz frequency and varying R_{in} for the $coil_3$ geometry at 1mm transmission distance. The geometry for both coils is the same. The source efficiency increases with R_{in} and may be very high at thousands of Ω R_{in} despite the low transmit inductance compared to lower frequency WPT systems. This is a reason why low power, mW applications are ideal for RFNFC - large load resistance is necessary for 1-20 mW output power. With large load resistance, the high source efficiency is possible despite the 5-15 nH L_1. Increasing the load power would decrease the load resistance (for the same output voltage), and accordingly the source efficiency would suffer greatly and result in a need to increase the coil area and decrease the frequency for adequate efficiency.

The optimal source efficiency occurs for larger area coils, with intermediate ratio of w/l. Similar to before, smaller w leads to increased inductance, thus smaller C_2 and α. More significantly, smaller w and greater l lead to increased L_1, increasing the reflected

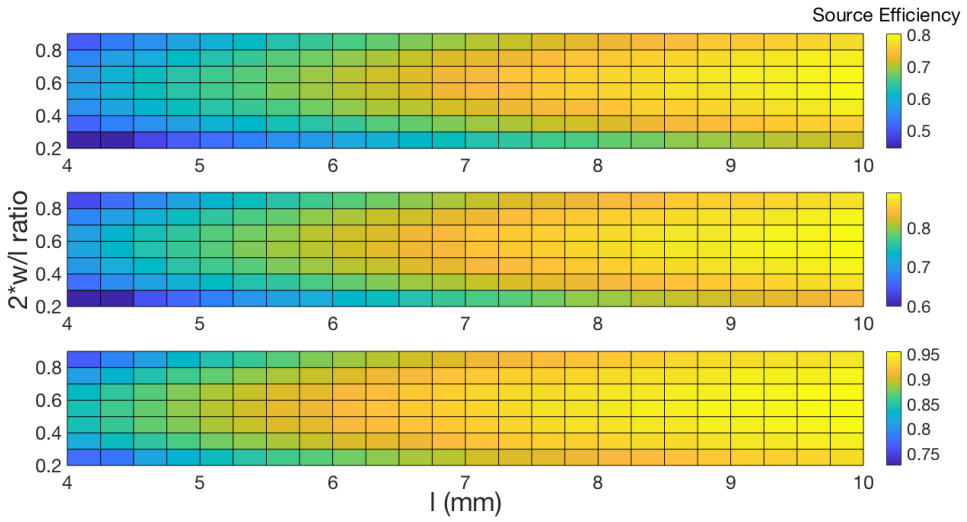

Figure 3.8: Geometry effect on source efficiency at 850 MHz with R_{in} = (a) 500Ω (b) 1000Ω and (b) 3000Ω

resistance R_{eq} and thus source efficiency. Too small w and the quality factor decreases. Too large w and the inductance decreases, thus the ideal value of w is an intermediate value. This consideration is unique to high efficiency, RF near field coupling. Lower frequency systems have greatly increased L_1, thus the source efficiency will be guaranteed large without having to consider this as a factor.

This also highlights part of the design choice. While larger l, especially for the transmit coil, leads to increased source efficiency, it also increases the area. Hypothetically, it is worth 5% source efficiency decrease to decrease the area by 36%, moving from l = 10mm to l = 8mm. But why not just use a very large inductance transmit coil and very small area receive coil? This can be done to an extent (as will be demonstrated), but very large inductance mismatch will not necessarily lead to better efficiency. When using very large area, large inductance transmit coil, the receiver coil should not be drastically different in area lest the k will suffer. From (2.5), R_{eq} improves linearly with the inductance L_1 but with the square of k, so if an increase in L_1 is met with a similar decrease in k, source efficiency will suffer. Further, the coil efficiency is dependent on k and not L_1, so any difference in the coil geometry to operate with large L_1 and Q_2 need not have a meaningful reduction in

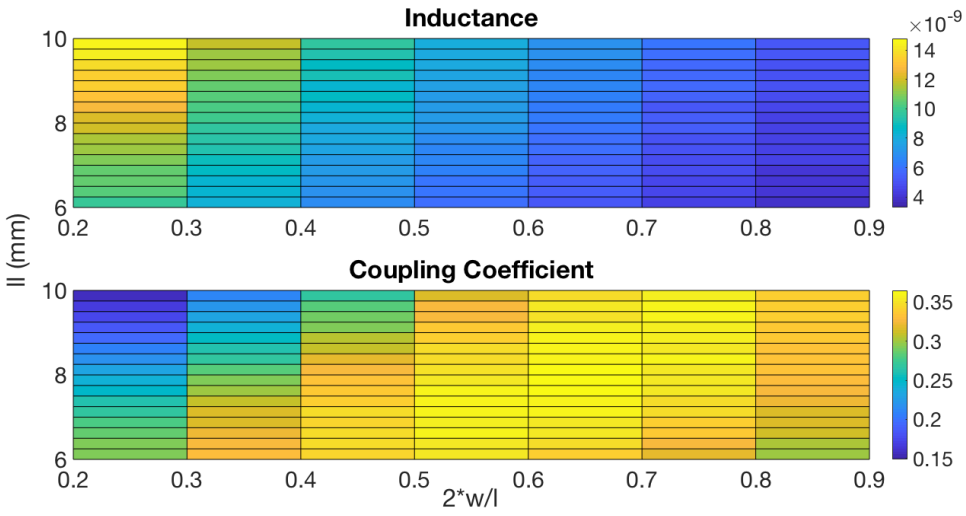

Figure 3.9: HFSS simulation with receiver coil l = 6mm, w = 1.5mm, and varying geometry for transmit coil at 800 MHz

k. A HFSS simulation demonstrating this is shown in Fig. 3.9, for fixed small area receiver coil and varying the size of the transmit coil. Using the same coil geometry for the transmit and receiver coils (l = 6mm, 2* w/l = 0.5) has the largest k, but small L_1. Similar k can be achieved by increasing both transmit l and w, but this leads to equal or lesser transmit inductance, thus no benefit. Changing the coil geometry to get improved L_1 decreases k. Since the receiver coil inductance is small (around 6 nH), L_1 should be improved. The peak efficiencies in this dissertation occur at the greatest load power, thus lowest $R_{in,PDU}$, so the source efficiency cannot rely on huge $R_{in,PDU}$ for acceptable efficiency even after accounting for matching. Thus for very small inductance receiver coils, a balancing of the decrease in k and increase in L_1 should occur.

Considering all these factors, 4 different coils were selected for full system design. These designs were selected for best combination of receiver coil area and coil+source efficiency. The quality factor and inductance of each coil is shown in Fig. 3.10. One may refer back to Table 3.1 for the geometry parameters. $Coil_4$ has the largest inductance because it was chosen to have the lowest ratio of w/l, sacrificing quality factor at higher frequency for increased inductance. $Coil_4$ was designed and intended to operate as the

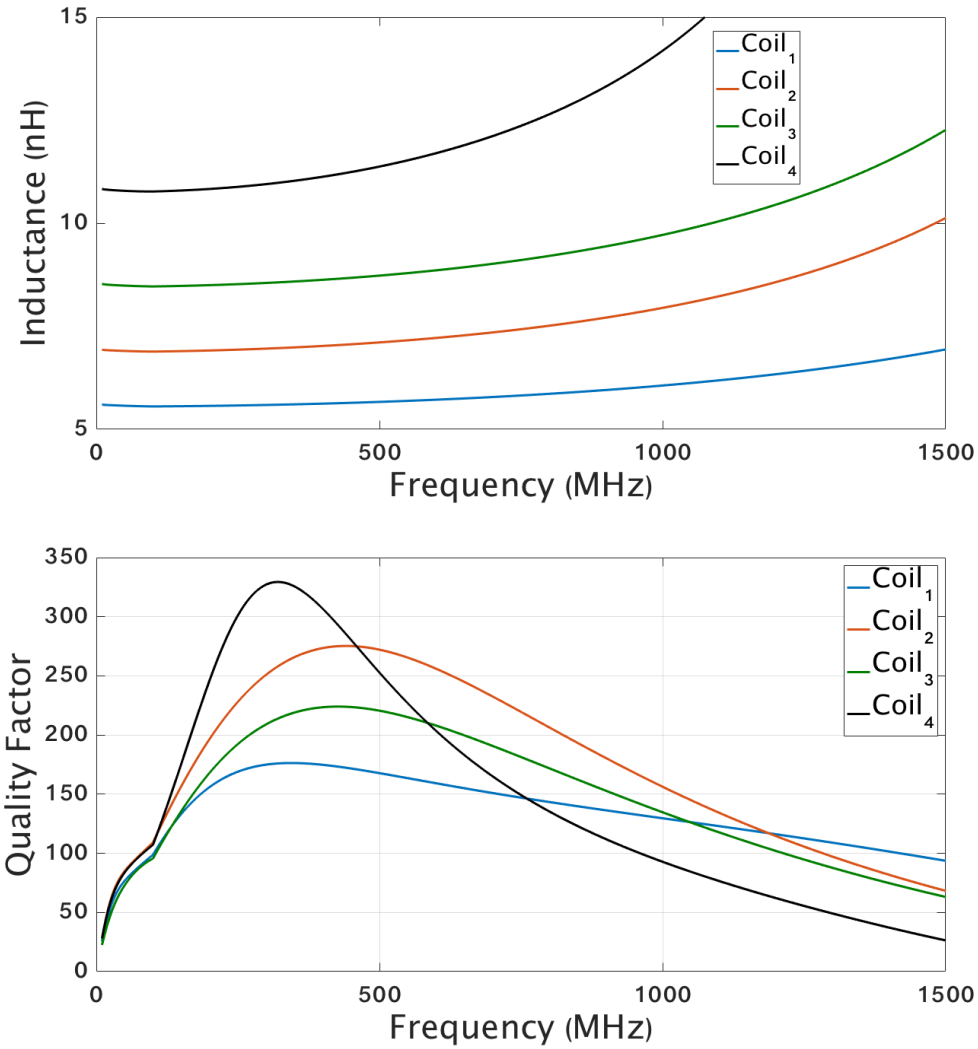

Figure 3.10: Simulated inductance and quality factor of each coil

highest efficiency transmit coil. The smallest area coil is $coil_1$ (33 mm^2), but has the lowest quality factor. This demonstrates the tradeoff between area and efficiency inherent to the design. $Coil_1$ has similar geometry to the receiver coil examined in Fig. 3.9, and a similar balancing of k and L_1 shows both $coil_4$ and $coil_2$ are suitable for use as transmit coils for $coil_1$. $Coil_2$ has the best overall Q across different frequency, and is selected as the coils for demonstrations of the reverse PDN in Chapter 4 and the integrated inductor in Chapter 5 to give operating frequency flexibility. The HFSS simulated coupling coefficient variation with distance for different coil combinations used in the full system is shown in Fig. 3.11.

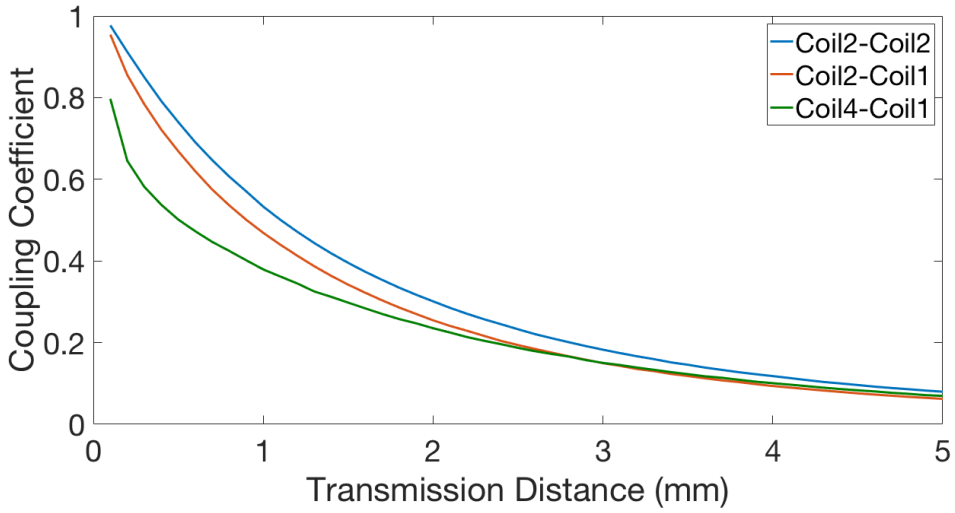

Figure 3.11: Transmission distance vs k for different coil links, at 900 MHz

For each combination the system efficiency can be estimated by using the k for a given transmission distance with the Q and L from Fig. 3.10. Note that the larger line width $coil_2$ has higher k as the transmission distance increases, as the metal area of the coil is greater. As the mismatch in geometry to $coil_1$ is greater for $coil_4$ than $coil_2$, the k is notably smaller in this case. However, when using $coil_2$ for both coils, the best k is achieved due to the fact the coil geometry is the same and the line width (and metal area) of the coils is larger. This makes a $coil_{2,2}$ system optimal for operating at increased transmission distance.

The coil and source efficiency as a function of frequency for various coil links is shown in Fig. 3.12 at 1mm and 2mm transmission distance and varying R_{in}. This graphic captures most of the previous discussion, while showing how the selected designs balance the various constraints. For the coil efficiency, all the designs have very high quality factor such that increasing the transmission distance has minimal effect on the coil efficiency. The coil efficiency can operate with lower k without a large decrease in the efficiency. However, the coil efficiency sharply decreases when R_{in} increases from 500Ω to 5000Ω. A system with $coil_1$ receive is most susceptible, as the small L_2 causes α to be larger. This receiver coil is not a good fit for the smallest load power (less than 5 mW). While the other systems have efficiency decrease, they are still suited for the lowest load power. In addition, the

$half_{4,1}$ link shows the most variation in coil efficiency with frequency, as the Q of $coil_4$ varies most with frequency. Thus systems with a transmit $coil_4$ are chosen to have lower source frequency in experimental work.

The source efficiency shows the opposite trend to the coil efficiency: the efficiency is greatly improved by increasing R_{in}. This is by design, as the coil geometry was selected to balance the decrease in coil efficiency with increasing load resistance with substantial gain in source efficiency. When R_{in} is 500 Ω, the increase in transmission distance has a larger effect on the source efficiency. Unlike the coil efficiency, the source efficiency is very susceptible to decrease in k. When the load resistance is greatly increased, the source efficiency shows much less decrease with transmission distance. While the efficiency is still slightly better at 1mm, the transmission distance can be increased by 100% with only slight efficiency decrease as the coil efficiency remains largely constant at smaller k and the source efficiency remains largely constant at large R_{in}. When operating at increased transmission distance (2-3mm), it should be expected then that the peak efficiency will occur at larger load resistance than for 1mm transmission distance.

3.3.4 Effect of Misalignment

To demonstrate the effect of misalignment of the coils, a link with $coil_{2,2}$ was simulated at 2mm distance with varying lateral misalignment, up to half of the length of $coil_2$. The effects of misalignment on k, the coil efficiency, the source efficiency, and the combined source+coil efficiency is shown in Fig. 3.13. Up to 1 mm misalignment, k and the efficiency of the system is not noticably changed. This is expected, as near field coupling is less suspectible to misalignement, compared to inductive power transfer for instance. As the misalignment increases, the k starts to fall off but the coil efficiency stays high. Again, this is as expected because near field coupling can operate with high coil efficiency at lower k if the Q is high. The source efficiency suffers greatly, however, as k starts to decrease. Thus, while the coils still transfer the power with high efficiency with large misalignment, much

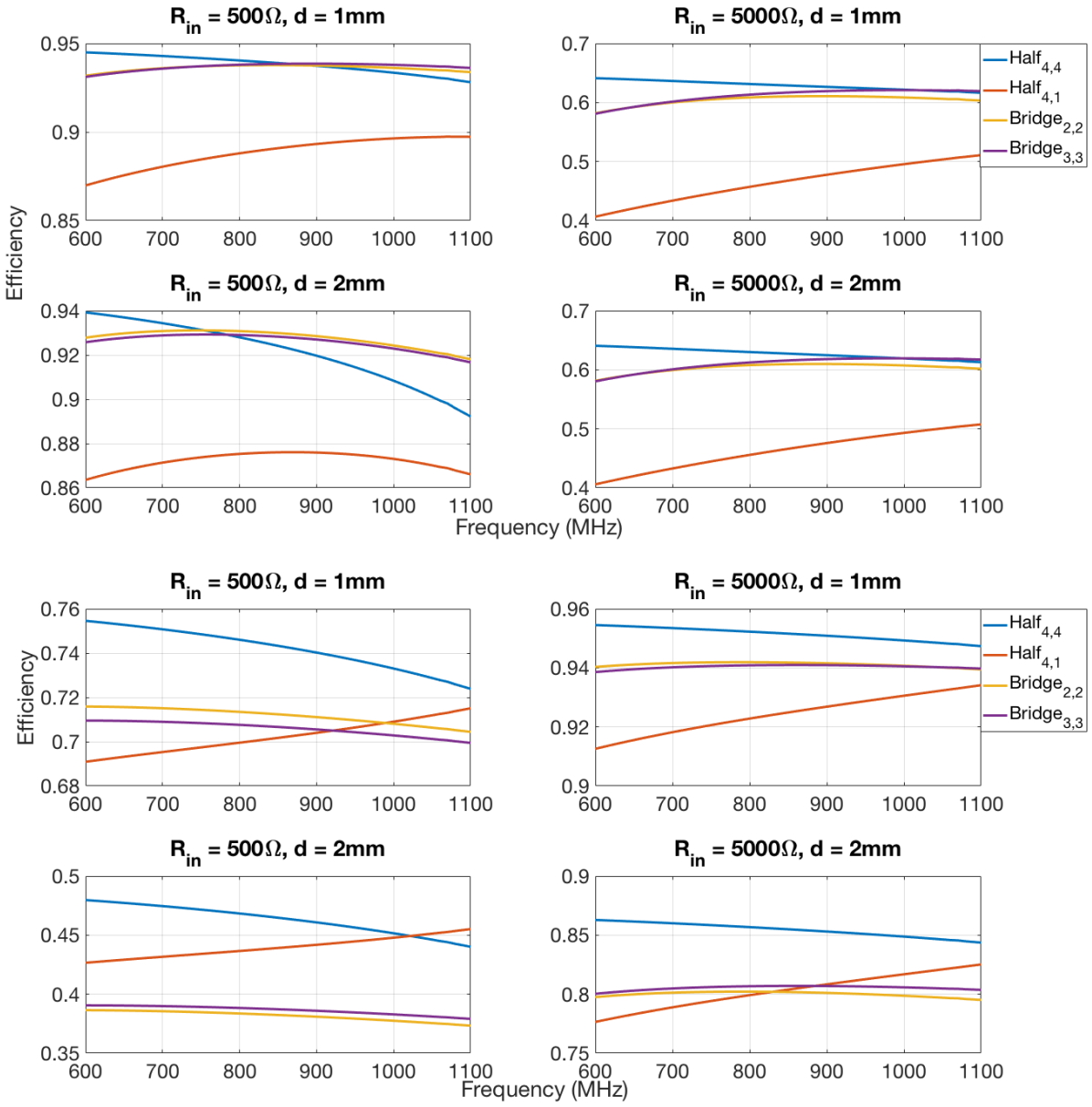

Figure 3.12: Coil (top) and source (bottom) efficiency for different transmission distance d and R_{in}

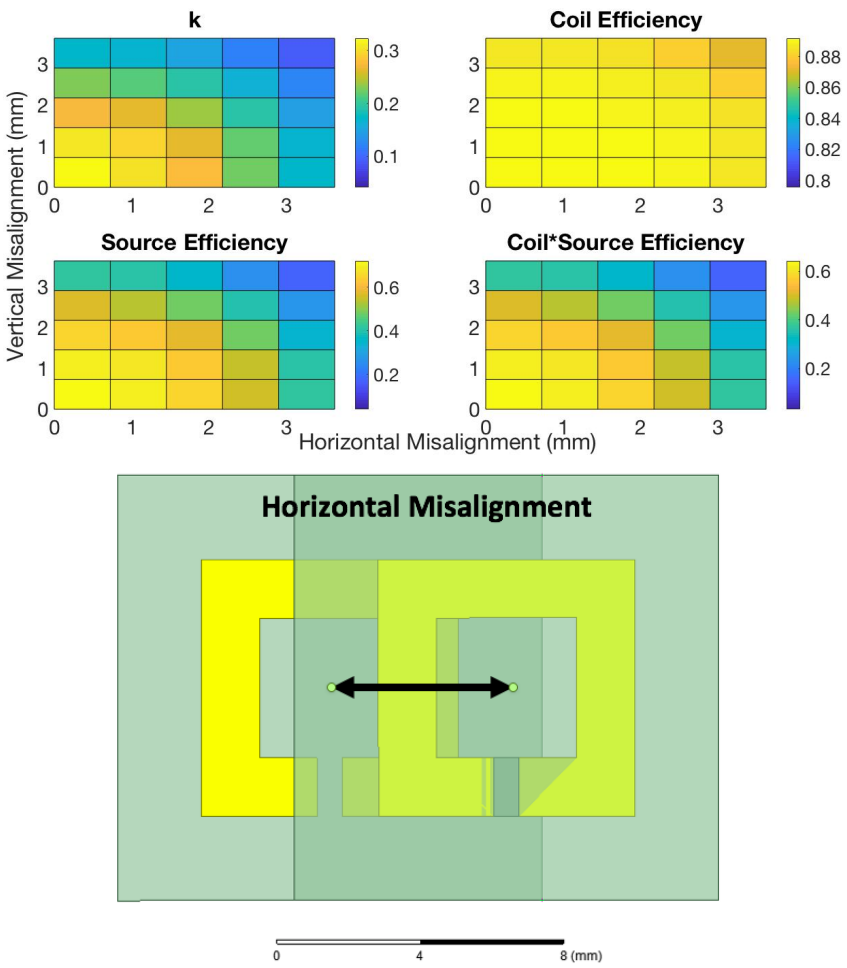

Figure 3.13: (a) HFSS simulated k on $coil_2$ change with lateral misalignment, and the corresponding effect on the coil and source efficiency and (b) Picture of the HFSS simulation model for this setup

power is lost in the source such that low power, RF near field coupling can only tolerate around 1mm misalignment in either direction without compromising efficiency.

3.4 Rectifier Topology and Diode Selection

3.4.1 Diode Selection

The selection of an appropriate diode is crucial for efficiency. Three factors are important in a RF near field coupling system: the junction capacitance C_j, the forward voltage V_f, and the breakdown voltage. C_j and V_f relate to the switching and forward voltage

Table 3.2: Comparison of RF Diodes

Diode Model	C_j	V_f	Breakdown Voltage	Loss from (2.10)	Switching loss	Efficiency Decrease
HSMS-2820	0.7 pF	0.34V	15V	3.4 mW	0.34 mW	13.3%
SMS-7630	0.14 pF	0.26V	2V	2.6 mW	0.04 mW	N/A
BAR64	0.17 pF	1.1V	150V	11 mW	0.05 mW	39.2%
HSMS-2860	0.18 pF	0.25V	4V	2.5 mW	0.05 mW	N/A
SMS3922	0.7 pF	0.34V	8V	3.4 mW	0.34 mW	N/A
SMS3923	0.9 pF	0.37V	20V	3.7 mW	0.58 mW	15.2%

loss, respectively, and the breakdown voltage limits the maximum rectifier output voltage, decreasing the efficiency at larger load power. Table 3.2 shows a comparison of several diodes used in RF design. The two sources of power loss are determined from (2.10) and the neural net switching model for a bridge rectifier with 1000Ω load and 14.5 dBm, 800 MHz source. Note that while V_f is not constant, the diode current change is small over all loads considered such that the value of V_f is assumed not to change significantly.

An ADS simulation of a half-wave rectifier with 14.5 dBm source, optimized for efficiency, shows reverse voltage in excess of 5V across the diode. Accordingly, the SMS-7630, HSMS-2860, and SMS3922 diodes all have insufficient breakdown voltage. At increased power load, the rectifier output voltage will be limited and the efficiency will decrease. Among the rest of the diodes, the Avago HSMS-2820 series diodes have the lowest loss, and as they have the best combination of breakdown voltage and low loss, they are selected for this work. The forward voltage loss is dominant over the switching loss, such that even though the BAR64 diode has much smaller switching loss, the large increase in forward voltage loss leads to the greatest efficiency drop in the given system. If very light loads were considered (less than 1 mW) such that the voltages are less, the SMS-7630 series diodes would be the optimal choice. If higher power and voltage were considered, the BAR64 diode would be the superior option. The efficiency decrease from the diode is 13% even with HSMS-2820 diodes in this example. Even though the diode selection is much less interesting from a design standpoint compared to the rest of this thesis, this highlights the importance of proper diode selection to achieve the best efficiency.

3.4.2 Rectifier Topology

Three different rectifiers were considered for RF-DC conversion: half-wave, bridge (full-wave), and Class E. A Class E rectifier is a modified version of the half-wave rectifier. A class E rectifier is a resonant rectifier that seems ideal for low power, RF operation because it uses only a single diode (only one forward voltage loss) and because it uses zero-voltage switching to mitigate switching loss in the diode. Using the equations from [85] for a 1000Ω rectifier load at 868 MHz, the calculated class E filter inductance value is 472 nH and filter capacitance value is 0.07 pF. For RF design, this is very, very difficult to achieve in practice. Moreover, the class E rectifier has its own resonant frequency which needs to be perfectly matched to the coils to have optimal efficiency - adding extra design complexity. A RF near field coupling system designing a custom chip rectifier might be able to use the class E rectifier, but it is unsuitable for the work in this dissertation using components off the shelf.

Full systems using both the half-wave rectifier and the bridge are designed to compare the two rectifier topologies. Both the calculated efficiency and the ADS optimized, simulated efficiency for the $coil_{4,4}$ link with both a half-wave and bridge rectifier are shown in Fig. 3.14 for 14.5 dBm, 700 MHz source. The ADS simulation used the same HFSS simulated coil data as the calculated efficiency, with microstrip line components added. The values of C_m, L_m, C_1, and C_2 were optimized for best efficiency. The correlation of efficiency to load resistance in the two cases is very different. In fact, the ADS simulation suggests the bridge rectifier should have the best efficiency. This cannot possibly be true, as the only major difference with respect to efficiency is that the bridge rectifier has an extra forward voltage loss such that, if both rectifiers are optimally matched, the half wave should have higher efficiency. This represents a key finding of this dissertation - simulation based techniques are less accurate for efficiency analysis than the demonstrated analysis. While this example was chosen specifically to make this point, other ADS comparisons between the bridge and half wave rectifiers have shown both the half wave and bridge as

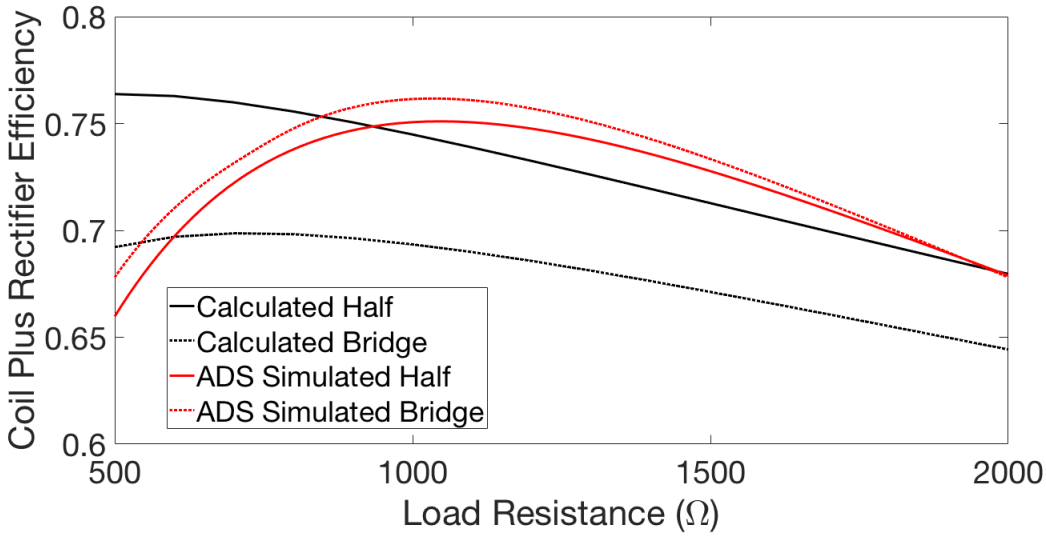

Figure 3.14: Comparison of analysis techniques for half and bridge rectifier with $coil_{4,4}$ with 14.5 dBm, 700 MHz source, 1mm transmission distance

superior for different designs. Again, this defies reason as one of the two should be superior to the other more generally, as will be shown in measurement results. ADS simulation does have value for RF near field coupling systems, as will be discussed in the next chapter, but not for efficiency analysis. Bridge rectifiers will still be used in full system measurements for analysis purposes, as the bridge rectifier is less susceptible to dynamic effects with a RFNFC system for better correlation with modeling, as will also be discussed in the following chapter.

3.5 Coil + Rectifier Experimental Work

Various aspects of the coil design were validated through measurement. Without the PDU, isolating the influence of various parameters is more easily demonstrated. In addition, most of these measurements will not be repeated in Chapter 6 measurements of full systems, as the purpose (validating design considerations) is already completed. The measurements were performed with a HP 8648D RF signal generator and an oscilloscope, with variable resistor rectifier load. Chapter 6 gives more complete details on the measurement setup and procedure.

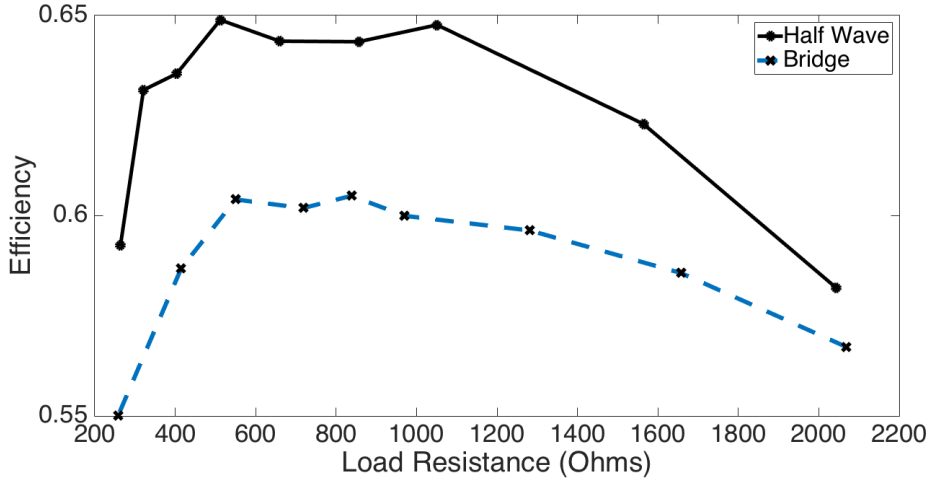

Figure 3.15: Comparison of the bridge and half-wave rectifier with $coil_{2,2}$.

3.5.1 Bridge vs Half Wave Rectifier

A comparison of a half-wave and bridge rectifier with $coil_{2,2}$ for both RF coils is shown in Fig. 3.15. The measurement is completed at 1mm transmission distance with 14.5 dBm, 868 MHz source. The half wave rectifier has a higher efficiency across all load. In addition, the efficiency difference is largest at low load resistance, as this is the lowest output voltage. Accordingly, the bridge rectifier is more affected by the forward voltage, while at large load resistance the output voltage is larger and diminishes the efficiency decrease from forward voltage loss.

3.5.2 Rectifier Efficiency with Increasing Input Power

The effect of the input power on the efficiency of $bridge_{2,2}$ is shown in Fig. 3.16. The measurement was completed at 1mm transmission distance with 1000Ω load resistance and 780 MHz source frequency. As the input power increases, the efficiency improves. With constant resistance load, the coil efficiency and source efficiency is mostly unchanged as the input power increases. Only slight variation in R_{in} with rectifier output voltage leads to changes in these values, and their changes mostly cancel each other out as the input power increases. Thus the efficiency increase comes via the rectifier, because the rectifier

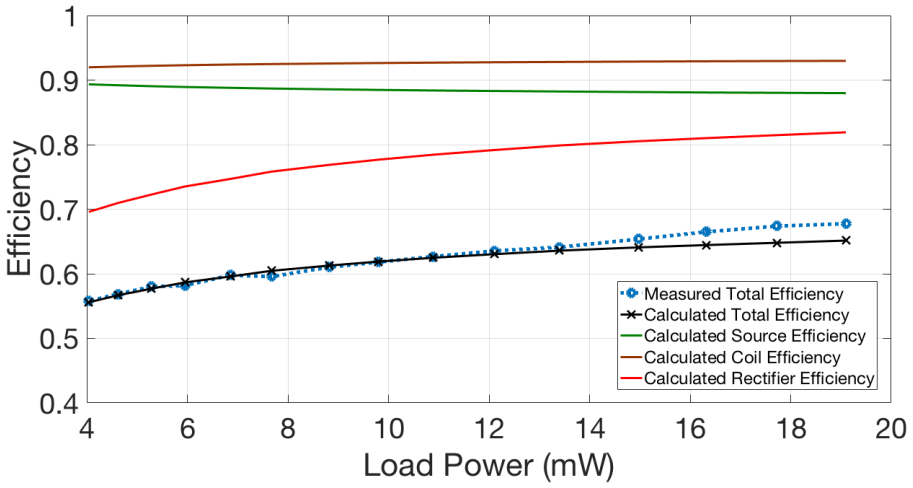

Figure 3.16: Effect of the input power on efficiency for $bridge_{2,2}$. L_m = 0.3 nH, C_m = 0.2 pF, C_1 = 3.5 pF, C_2 = 3.5 pF

output voltage increases with input power. This leads to improved efficiency from (2.9) as previously discussed.

3.5.3 Rectifier Efficiency with Increasing Resistance

Figure 3.17 shows the effect of increasing resistance on the efficiency of the $bridge_{3,3}$ design. This measurement is completed at 1mm transmission distance with 14.5 dBm, 1040 MHz source. The rectifier efficiency is improved in a similar way to increasing the input power - by increasing the output resistance the output voltage is increased, for improved efficiency. Unlike the input power variation measurement, the load resistance is not fixed. The coil efficiency decreases and matching loss increases as the load resistance increases. This leads to an intermediate voltage having the highest efficiency. At smaller load resistance the loss is dominated by the rectifier efficiency, but as the load resistance increases the coil efficiency decrease outpaces the rectifier efficiency increase.

The largest limitation with the calculated efficiency is it assumes an optimally matched system. Over a wide range of resistance, this is not necessarily the case. In this instance, there is disagreement between the calculated and measured efficiency at the large load resistance, because the same matching circuit was used for all load resistance in measurement.

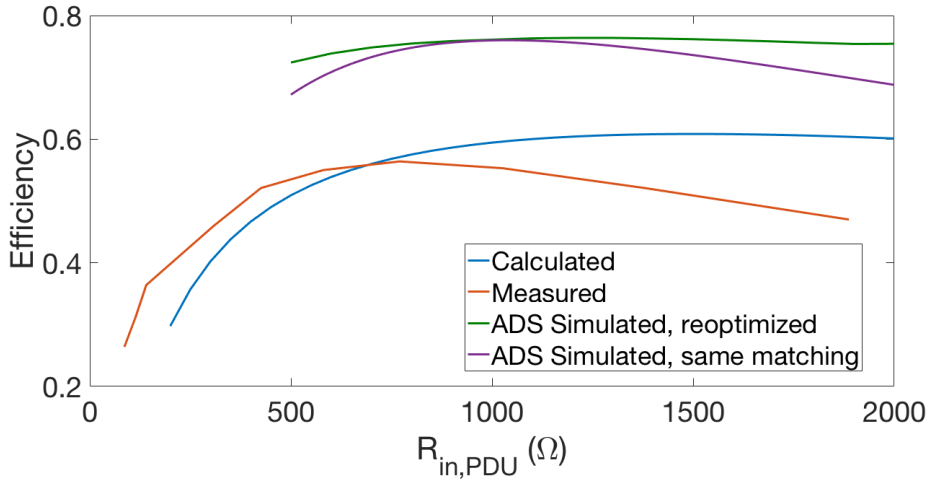

Figure 3.17: (a) Effect of changing load resistance on bridge rectifier efficiency

While the calculated efficiency expects that the efficiency will still be large, the measured efficiency shows a sharper decrease as the matching loss increases. If this circuit were matched for a 2000Ω load instead, the agreement would be much better at the higher load resistance, but worse at the lower load resistance. This is shown from the ADS simulation. Ignoring the fact the ADS simulation grossly overestimates the efficiency (count this as more evidence of the calculated efficiency superiority to simulated), the general shape of the ADS simulation using the same matching network more closely resembles the shape of the measured curve. This shows that a portion of the loss at the upper end of the load resistance is matching loss - not captured by the proposed analysis. When the matching network is reoptimized for each resistance point in ADS, a curve more like the calculated efficiency results. The calculated efficiency analysis should then just be used to predict the best possible efficiency for a single point, and not used to determine the efficiency over a wide range of load.

3.5.4 Different Frequencies

A comparison for the rectifier efficiencies of $half_{2,1}$ and $half_{1,1}$ at 600 MHz and 1000 MHz is shown in Fig. 3.18. At load resistance less than 1000Ω, the efficiency of all systems is

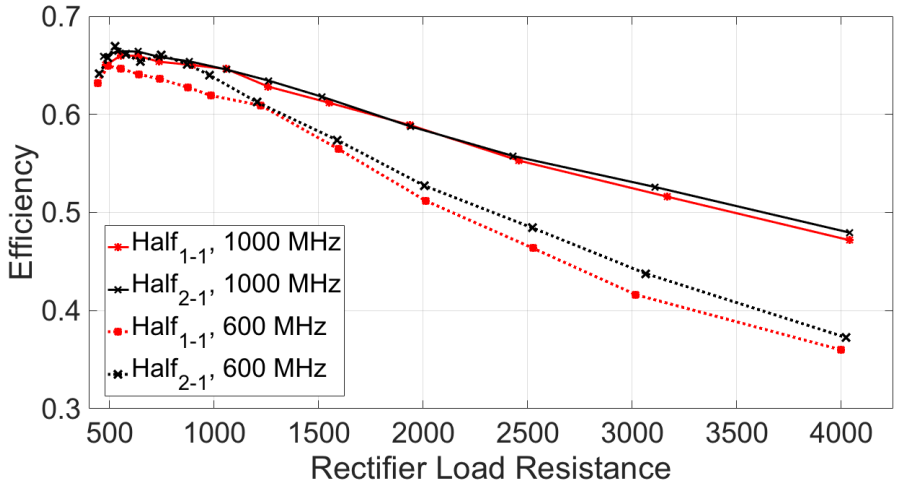

Figure 3.18: Efficiency at 600 MHz and 1000 MHz for $half_{2,1}$ and $half_{1,1}$

similar. In general, using $coil_2$ as the transmit has slightly higher efficiency as the quality factor of this coil is much improved over $coil_1$ and has slightly higher L_1, while the k is very similar. However, as the load resistance increases, the 600 MHz design efficiency decreases much faster. This is not intuitive, as at higher frequency it would be expected there are greater diode switching and microstrip losses. However, a larger value of C_2 is needed to resonate at 600 MHz (C_2 = 7pF was used) than 1000 MHz (C_2 = 0.2pF). This leads to a corresponding larger value of α, which leads to a greater decrease in the coil efficiency. If larger load resistance is needed for a system, it is beneficial to increase the frequency of the system to limit the value of C_2 necessary for resonance.

3.5.5 Different Transmission Distance

A comparison of $half_{2,2}$ and $half_{2,1}$ with 14.5 dBm, 850 MHz source is shown in Fig. 3.19 at both 1mm and 2.5mm transmission distance. At 1 mm transmission distance, the efficiency peaks in the 500-1000Ω load range. While $half_{2,2}$ has slightly higher efficiency, the $half_{2,1}$ design has smaller receiver coil area, again showing the tradeoff between receiver coil area and efficiency inherent to the design. When the transmission distance is increased to 2.5mm, it can be seen the efficiency now peaks in the 1500-2500Ω load range. As dis-

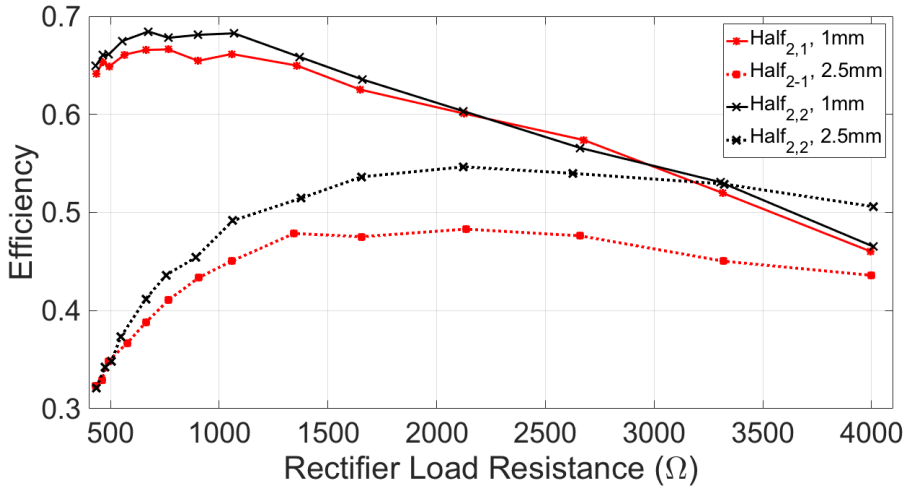

Figure 3.19: Measured efficiency of rectifier for $half_{2,2}$ and $half_{2,1}$ at 1mm and 2.5mm transmission distance

cussed in an earlier section, a large value of $R_{in,PDU}$ is needed for high source efficiency to compensate for smaller k ($\sim$0.2 at 2.5mm distance compared to $\sim$0.5 at 1mm distance). This is why the efficiency peaks for a different load resistance range. Also, using $coil_2$ here as the receive coil leads to much greater efficiency improvement. While at 1mm the marginal gain in k did not lead to large efficiency increase, at 2.5mm transmission distance this increase in k is much more significant. The effect of matching loss may also be seen when $R_{in,PDU}$ = 4000Ω. At 2.5mm transmission distance, the $half_{2,2}$ circuit shows higher measured efficiency than at 1mm. This is not actually possible from the efficiency analysis, or logically as the circuit has the same parameters except smaller k, which will only decrease efficiency. As the circuits are matched optimally for their peak efficiency (and this occurs at smaller load resistance for 1mm transmission distance), more matching loss is present at 4000Ω at 1mm transmission distance.

3.6 4 Coil Circuit Design

While most of the designs examined in this dissertation are very similar, one unique 4 coil network will be examined. In this design, the goal is very different. The objective

is to increase the transmission distance and provide similar power output discontinuously without increasing the source power or significantly increasing coil area. Accordingly, efficiency is not a large concern compared to the transmission distance and coil area (for discontinuous use, it is assumed adequate time is given to 'charge' the rectifier output to provide increased output power). For this demonstration, large storage capacitance is located at the output of the rectifier, to power a boost converter. The integration challenges for this are discussed in the following chapter. To store as much energy as possible at the output of the rectifier, the voltage should be as high as possible from $1/2CV^2$. The rectifier is charged with open circuit load, such that with infinite resistance load, a 'loaded coil' efficiency metric is not valid. Efficiency should not be completely ignored, lest the rectifier output voltage will suffer, and the efficiency metric used is given as [60],

$$\eta_{4coil} = \frac{(k_{12}^2 Q_1 Q_2)(k_{23}^2 Q_2 Q_3)(k_{34}^2 Q_3 Q_4)}{[(1 + k_{12}^2 Q_1 Q_2)(1 + k_{34}^2 Q_3 Q_4) + k_{23}^2 Q_2 Q_3][1 + k_{23}^2 Q_2 Q_3 + k_{34}^2 Q_3 Q_4]} \tag{3.1}$$

The geometry of the 4 coil system is shown in Fig. 3.20. The coil1 is supplied by the RF source through a matching network, and coil2 is on the opposite layer of the board, center aligned. Coil3, on the receiver board, faces coil2. Coil4 is on the other layer of the receiver board, center aligned, and connects to a half wave rectifier. The same single turn ring geometry is used, though with the increased number of coils the number of variables rises. To limit the HFSS simulations, coil1 and coil4 were picked to have the same geometry, and coil2 and coil3 were picked to have the same geometry. In addition, this system operates at 30mm transmission distance with 14.5 dBm, 960 MHz source. As k_{23} quickly falls with the increase in transmission distance, coils2/3 were designed to have much larger area to have adequate k_{23}. The maximum area at 960 MHz is restricted though, as the self-resonant frequency will be exceeded if the coil is too large. Restricting the area to 400 mm^2, the optimal efficiency was reached with the geometry shown in Table 3.3 at 0.2% At this geometry, k_{23} = 0.0072, which while small, is sufficient to store enough energy to

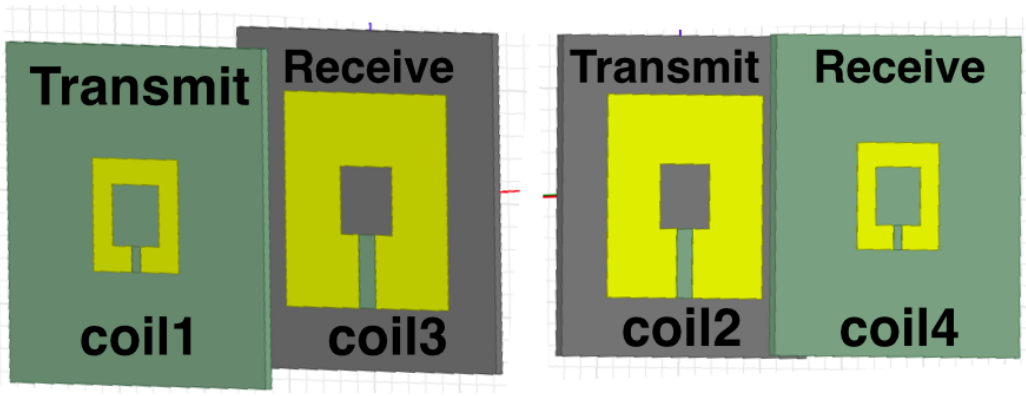

Figure 3.20: (Left) 4 coil system when viewed from left and (right) 4 coil system when viewed from right

Table 3.3: Four Coil Parameters

	Coil 1, 4	Coil 2, 3
l	10 mm	19 mm
w	2.3 mm	6.5 mm
L	10.2 nH	10.4 nH
Q	188	131

power milliwatt-scale loads.

3.7 PDU Selection and Circuit Design

This dissertation uses COTS converters for the PDU. Accordingly, the 'design' aspect for the PDU circuit is not in PDU design but selecting the appropriate PDU and modeling the PDU in the entire system. While the main weakness of the efficiency analysis is that it loses accuracy over a wide range of load, the PDU helps rectify this (no pun intended). A PDU is shown to help maintain the efficiency over a wide range of load [58]. Because the input resistance to the PDU is a function of the duty cycle and the change in $V_{in,PDU}$, $R_{in,PDU}$ will not change as much as the corresponding change in R_{Load}, opposed to using a rectifier alone. This leads to improved efficiency over a wider range of load, using the same component values for the matching network, though the peak efficiency is sacrificed. As the designed system operates with maximum 28 mW input, the optimal PDU will have high efficiency at this loading range. In the two coil system targeting high efficiency, the buck regulator needs to be able to convert down to at least 1V. Similar to the diodes, the

Table 3.4: Comparison of MHz switching PDU

PDU Model	Switching Frequency	Eff @ 1V, 10 mW	V_{in} range	V_{out} range
LTC3564	2.25 MHz	85%	2.5-5.5V	0.6-5.5V
LTC3600	4 MHz	70%	4-15V	0-14.5V
TPS54A20	4-10 MHz	50%	8-14V	.5-2V
TPS62088	4 MHz	87%	2.4-5.5V	0.6-4.0V
TPS62650	6 MHz	89%	2.3-5.5V	.75-1.44V

selection of PDU is less interesting from a design standpoint but crucial for achieving optimal efficiency. The input voltage needs to work in the range of the rectifier output voltage measurements completed earlier (up to around 5V). In addition, the switching frequency is desired to be as high as possible. This enables a much smaller power inductor to be used for smaller overall system size. Few commercially available buck converters operate at MHz frequency, and a few are shown in Table 3.4. The LTC3600 and TPS54A20 are suited for higher voltage/power output than examined in this dissertation. The TPS62650 has the best combination of efficiency and switching frequency, but the output voltage range is very low. However, the TPS62615 (fixed 1.2V output, else the same as the TPS62650) will be used for demonstration of the integrated inductor in Chapter 5 due to the 6 MHz switching frequency. This dissertation needs to examine a wider range of output voltage to comprehensively explore and validate the efficiency model and calculations, but for a fixed voltage output this PDU would be superior. Among the other two, the LTC3564 has more output voltage range and the TPS62088 has slightly higher efficiency and frequency. Either could be used with equal effectiveness. To break dissertation formality briefly, all fabricated designs in this thesis are hand-soldered by myself. The TPS62088 is only available in wafer chip-scale package and the LTC3564 is available in SMT SOT package, such that the LTC3564 is significantly easier to hand solder for experimental work and is selected as the PDU for this dissertation.

No innovation in PDU circuit design is presented in this dissertation, as the circuit design simply follows the datasheet for the DC-DC converter, just changing the feedback resistors to give different output voltage. The guidelines for the layout were to minimize the amount of resistance on the output, input, and inductor traces, as this can lead to significant

power loss in the conductive losses of the PDN.

3.8 Summary

This chapter discussed the main design considerations for the coils for RFNFC systems. The modeling approaches and design tradeoffs, using the previous chapter analysis as a guide, were explained in this chapter. In particular, the transmit inductance, the effect of load resistance on the coils, and implications of source efficiency were examined both through calculation and measurements. The justification of the selection of diode and PDU components was also given in this chapter.

CHAPTER 4
RF NFC INTEGRATION CHALLENGES

4.1 Introduction

The previous chapter discussed the design, simulation, and modeling of the subsystems and complete system architecture. However, further integration challenges still remain. Merely piecing together and connecting the previously designed subsystems leads to an ineffective complete system. Various high frequency effects affect the selection of component values in RF near field coupling circuits. The conventional equations and analysis used to select these values do not necessarily hold at RF operation. It was previously shown the developed efficiency analysis is better suited for designing the system than simulators, but for component value selection the use of simulators greatly improves accuracy. This chapter discusses how to model microstrip line effects and parasitic capacitance, and investigates further adjustment of the resonant capacitance value in the case of the half wave rectifier.

This chapter also discusses the design of a reverse power distribution network (PDN). The reverse PDN is necessary for system integration to deliver a stable voltage supply to the PDU. Layout considerations, capacitance selection, and experimental validation of the reverse PDN is provided in this chapter for two coil, continuous power output systems and four coil, discontinuous power output systems to integrate large storage capacitance.

4.2 Component Value Selection for RF Inductive WPT

4.2.1 Purpose of External Components

This chapter discusses, in part, the selection of component values in RFNFC systems. For this dissertation, this pertains to the matching network values L_m and C_m and the resonant capacitor values C_1 and C_2. The value of C_2 is the most influential on the resonant

frequency and should be determined first. L_m, C_m, and C_1 are then selected to provide optimal efficiency at the resonant frequency with the selected value of C_2. Even without L_m, C_m, and C_1, over 50% efficiency of the coil + rectifier system is possible, as the purpose of these values is just impedance matching. This includes C_1, whose purpose is to cancel the leakage inductance from the transmit coil L_1 at the resonant frequency. While poorly chosen values for these components can increase matching loss, and even change the optimal resonant frequency if the circuit is optimally matched for a different frequency close to the resonant value with C_2, there is much greater margin for error on the selection of these values than the selection of resonant capacitor C_2, which will greatly change the resonant frequency of the system depending on its value.

4.2.2 Parasitic Capacitance Adjustment

Another effect of operating with higher frequency, lower inductance coils is that the parasitic capacitance, C_{par}, becomes a more influential factor. This effect has been previously examined in [86], but in near field coupling circuits at short transmission distance the parasitic coupling between the coils themselves must also be accounted for. The parasitic capacitance restricts the amount of inductance that can be designed in a RF near field coupling system. However, unlike other inductors (such as power inductors discussed in the next chapter), the near field coupling coils may be operated up to their self-resonant frequency with no disadvantages. To determine the value of C_{par}, the 2-port S-Parameters of each individual coil are simulated in HFSS. Then, the parasitic capacitance C_{par} is extracted from the self-resonant frequency and the inductance of each coil at 1 GHz. The simulated values of C_{par} are given in Table 3.1.

As parasitic capacitance is traditionally modeled in parallel with the inductor, this value of C_{par} should be subtracted from the value of C_2 as C_2 is in parallel with L_2 and thereby with the parasitic capacitance as well. If not, the resonant frequency will be downshifted from the desired resonant frequency. Take for example $coil_4$. For a phase resonant fre-

quency of 1 GHz with 1000Ω load, the value of C_2 should be 4.1 pF. However, when the value of the parasitic capacitance of $coil_4$, 0.484 pF, is added to this value, the phase resonant frequency becomes 954 MHz = more than 4% frequency shift. In practice, this modeling may be accomplished through a combination of HFSS and ADS simulation. The value of C_{par} determined from HFSS simulation can be used in subsequent ADS simulation to determine the appropriate value of C_2.

4.2.3 Significance of Microstrip Lines

The coil inductance and resonant capacitance values demonstrated in the previous chapter are in the range of 5-20 nH and 0.2-10 pF. Because these values are smaller than observed for lower frequency systems and the source frequency is at RF, the microstrip lines in the design have a considerable effect on the resonant frequency of the system. HFSS exported S-Parameters of $half_{4,1}$ were simulated in ADS, shown Fig. 4.1(a), with different lengths of microstrip line between the receive coil and receive resonant capacitor. With just 2 mm of microstrip line added, the resonant frequency is shifted by over 20%. The receive coil has only 6 nH inductance, thus it is more susceptible to this frequency variation. When $half_{4,4}$ is simulated, the effect is less pronounced as the inductance of $coil_4$ in the $half_{4,4}$ receiver is larger than $coil_1$, though almost 100 MHz shift is still observed.

The influence of microstrip lines is verified through measurement of the $half_{4,1}$ system at 0.5mm transmission distance and 14.5 dBm source and 1000Ω load, shown in Fig. 4.2. The rectifier output voltage was measured with C_2 and a 100 pF voltage smoothing capacitor in different locations (shown in Fig. 4.2(b)) for three cases as follows: i) C_2 at position 1 and the smoothing capacitor at position 3, ii) C_2 at position 2 and the smoothing capacitor at position 3, and iii) C_2 at position 1 and the smoothing capacitor at position 2. The circuit was measured with no matching circuit (short L_m and C_1, open C_m) and C_2 = 3.5 pF. Even though the circuit/schematic is the exact same in each case, the amount of microstrip line between various points is not. Accordingly, the rectifier output voltage fre-

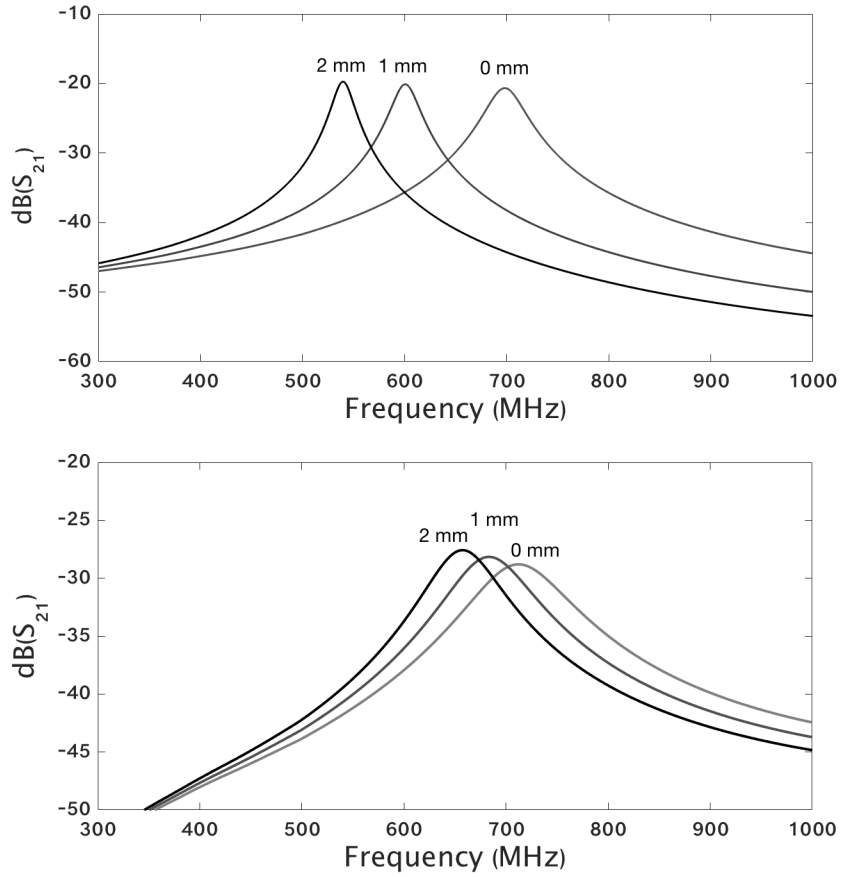

Figure 4.1: Effect of the transmission line length between L_2 and C_2 on the resonant frequency for (a) $half_{4,1}$ and (b) $half_{4,4}$

quency response greatly changes in each of the cases. It should be noted that the efficiency with 1000Ω load peaks around 60% (4.1V output) without matching network, emphasizing the significance of determining C_2 first and then selecting the transmit circuit values to further increase efficiency. The circuit was operated in very close proximity (0.5mm), but this highlights the significance of determining C_2 primarily, and then selecting the other values to squeeze extra efficiency out of the system. In particular, the value of C_2 must be adjusted to account for transmission lines in the receiver for operation at the desired frequency. The influence of microstrip lines and vias are modeled directly in ADS through MLine and via components, to help select the optimal values of C_2 and transmit impedance matching values.

The microstrip lines in the receiver are modeled in ADS using the equivalent WPT circuit shown in Fig. 4.3, using equivalent circuit values for the coils and equivalent modeled microstrip line geometry. Note that in this simulation, no transmit circuit values are used as they are not needed to determine the receiver resonant frequency. A generic diode component is shown as the rectifier, to be replaced with the appropriate rectifier topology being simulated. The simulated S_{21} parameter can determine the needed down adjustment of C_2 to resonate at a specific frequency. If a bridge rectifier is selected for the design, this is the final adjustment of C_2 to account for the detuning of the resonant frequency.

4.2.4 The Dynamic Behavior of Half Wave Rectifiers in RF Near Field Coupling

As discussed in the previous chapter, to achieve high source efficiency, large k is necessary. However, operating the coils with large k has an unusual effect on the half-wave rectifier: it shifts the resonant frequency lower. This is shown by a measurement of $half_{4,4}$ for two cases with no PDU. First, at 1mm transmission distance with C_1 = 5 pF, C_2 = 3.5 pF, and no matching network, both a bridge and half-wave rectifier were measured with 14.5 dBm source and 1000Ω load, shown in Fig. 4.4(a). There is more than 100 MHz difference in source frequency giving the best output voltage despite the same circuit. This is not

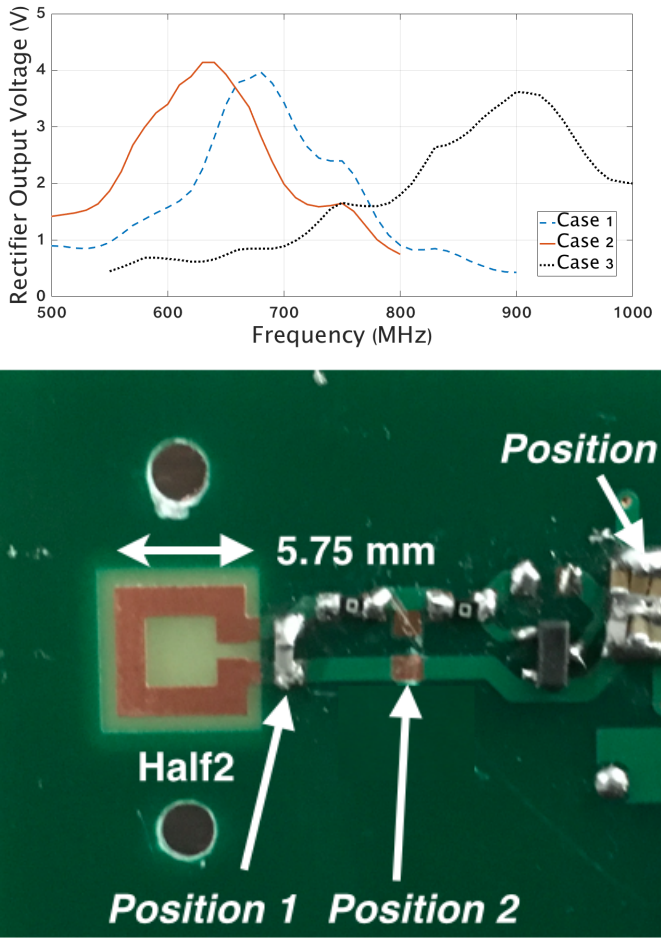

Figure 4.2: (a) Measured rectifier output voltage of $half_{4,1}$ coil+rectifier system with different positions of C_2 and the smoothing capacitor as classified in (b) photo of circuit used in testing

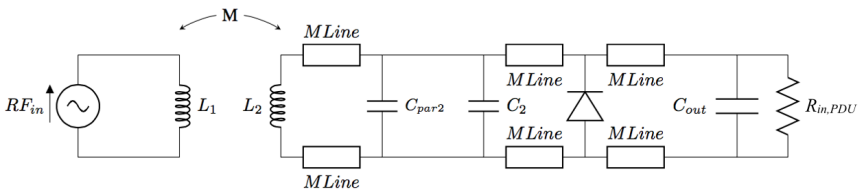

Figure 4.3: Circuit model for determining resonant frequency detuning from microstrip lines

just the influence of the microstrip line, because the current path in the bridge rectifier is more inductive than the half-wave rectifier. Next, the circuit was operated in very close proximity - 0.5mm - with a completely identical comparison. There was no matching network or C_1, C_2 = 2.4 pF, and the exact same board was used in the comparison. This was accomplished by using a diode where appropriate for a half-wave rectifier, using a shorting resistor at the other diode location for the positive half-cycle for the bridge rectifier, and keeping the locations for the diode in the bridge negative half-cycle open. This way, the half-wave circuit has a completely identical current path to the bridge rectifier in the positive half-cycle, with only an extra shorting resistor added in the current path for the half-wave rectifier. The rectifier output voltage comparison for these two cases is shown in Fig. 4.4(b). There is over 300 MHz shift - over 25% resonant frequency shift - between the two rectifiers. Even accounting for possible minor variations in the measurement, diode impedance, shorting resistor, etc, there has to be a fundamental difference in how the RF coil link interacts with the two rectifier types to account for such a drastic shift.

When using a half-wave rectifier, the effective inductance of the coil increases and downshifts the resonant frequency. A half-wave rectifier is the superior choice for high efficiency in a light load system. The forward voltage of the diode has a significant factor on the efficiency at the voltages examined in this paper, and having only one forward voltage drop in the half-wave rectifier leads to notable efficiency improvement. This differs from conventional wisdom though as the half-wave rectifier in theory only rectifies half the signal and wastes the other half, such that greater than 50% efficiency should be impossible. In a resonant WPT system, this is not the case as energy is stored in the reactive components in the negative half cycle. This is evidenced in a comparison of the half and bridge rectifiers in an ADS transient simulation of the WPT circuit in Fig. 4.5, with equivalent inductance and k to the $half_{4,1}$ link. Here, microstrip lines are not included in simulation as they disturb the transient waveforms, and the value of C_1 is adjusted for similar output power across different simulations.

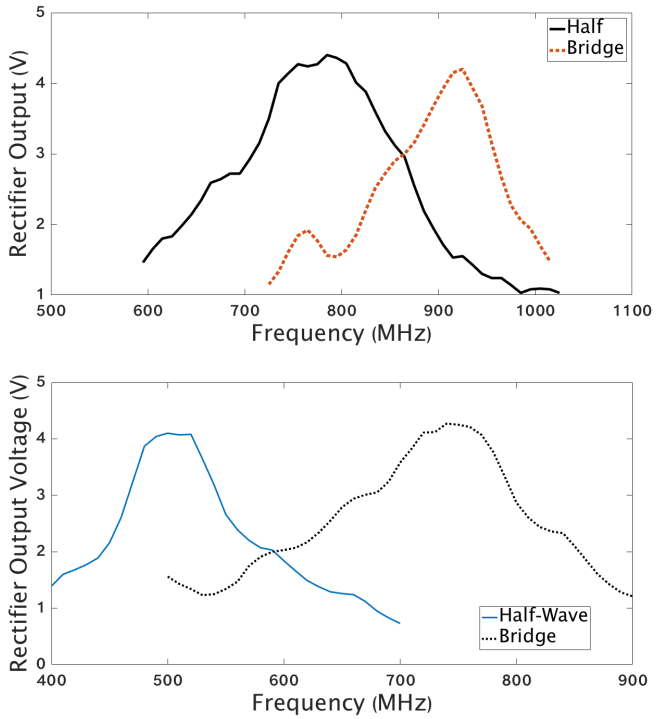

Figure 4.4: Comparison of the measured output voltage of a RF half wave rectifier and bridge rectifier with identical near field coupling circuit at (a) 1mm transmission distance and (b) 0.5mm transmission distance

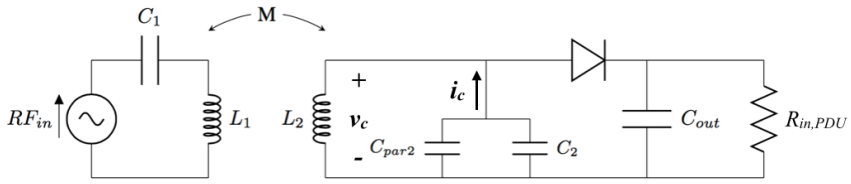

Figure 4.5: Circuit model for determining L_{half}

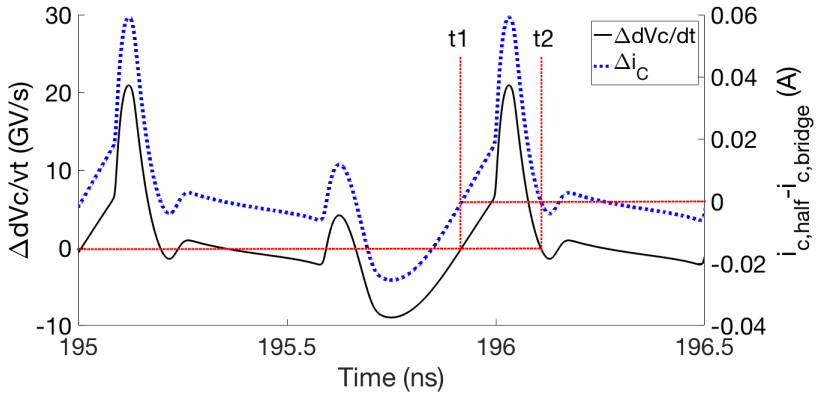

Figure 4.6: Difference in the simulated i_c current and $\frac{dVc}{dt}$ between the half-wave and bridge rectifier

For the half-wave rectifier, the stored energy is released in the positive half cycle, leading to a different i_c C_2 current in comparison of the bridge and half-wave rectifier as shown in Fig. 4.6. In the half-wave rectifier, there is an extra 'burst' of current as the capacitor releases stored energy. The value of the C_2 capacitance calculated from $i_C = C\frac{dVc}{dt}$ is the same as the given value for $C_2 + C_{par}$ in simulation for both rectifiers, thus the capacitor voltage adjusts as expected with the current. This difference in capacitor current leads to a similar difference in dVc/dt between the rectifiers, shown in Fig. 4.6.

If only considering the difference in the half-wave and bridge rectifier between the time points $t1$ and $t2$, where the half-wave current is greater than the bridge current in the positive half cycle, the difference in C_2 capacitor voltage ΔVc can be calculated from the difference in $\frac{dVc}{dt}$ as shown in Fig. 4.7. As the receive capacitor and inductor are in parallel, this difference in capacitor voltage is matched with an equivalent change in L_2 inductor voltage. From $V_L = L\frac{diL}{dt}$, this change in inductor voltage is matched by either a change in inductance or current derivative. The simulation shows negligible difference in receiver coil current in the bridge and half-wave rectifiers, thus there is effectively extra inductance L_{half} in the receiver coil during this time when integrated with a half-wave rectifier. This creates the downshift in resonant frequency when using a half-wave rectifier.

L_{half} may be calculated as shown in (4.1), where ΔV_c is the additional voltage in the

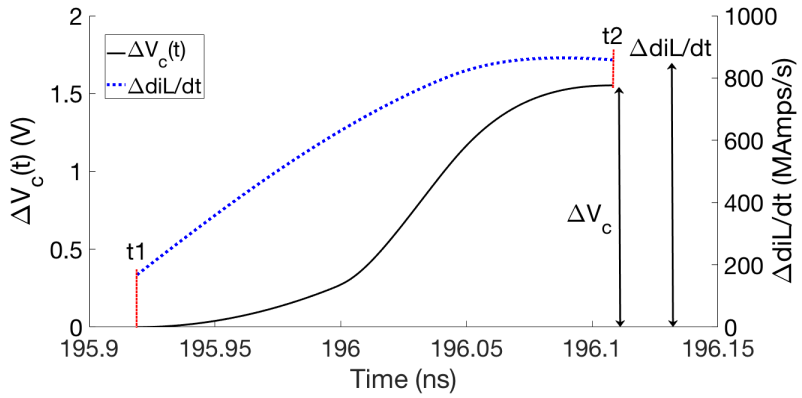

Figure 4.7: Change in V_c and $\frac{diL}{dt}$ between half and bridge rectifier between time $t1 : t2$

half-wave rectifier during time $t1 : t2$ and $\Delta\frac{diL}{dt}$ is the change in inductor current derivative over the same time frame, calculated from transient ADS simulation with either a bridge or half wave rectifier. ΔV_c is a difference from simulation of both the bridge and half wave circuits, while $\Delta\frac{diL}{dt}$ is a difference in just one of the circuits (either), calculated from the same time period. This leads to a new formulation of the phase resonant frequency, given in (4.2), where $C_{sum} = C_2 + C_{par}$.

$$L_{half} = \frac{\Delta V_c}{\Delta\frac{diL}{dt}} \tag{4.1}$$

$$\omega_{phase,half} = \sqrt{\frac{1}{(L_2 + L_{half})(C_{sum})} - \frac{1}{R_{in}^2(C_{sum})^2}} \tag{4.2}$$

4.2.5 Component Selection Process

To select the appropriate values of the circuit components L_m, C_m, C_1, and C_2, first the correct value of C_2 must be selected. The value of C_2 is the dominant value on the resonant frequency. The other values, including C_1, function mainly as impedance matching components and are selected to increase efficiency. This selection process is accomplished through the following procedure:

- In HFSS, simulate C_{par} for the designed coil link at the selected transmission distance
- In ADS simulation, adjust value of C_2 to resonate at the desired source frequency, from the simulated S-Parameters of circuit shown in Fig. 4.3
- (Only with half-wave rectifier) Calculate the value of L_{half} from ADS transient simulation of circuit shown in Fig. 4.5 and (4.1). Adjust value of C_2 to resonate at same frequency using (4.2)
- Select the values of L_m, C_m, and C_1 to optimally match source to following RF near field coupling circuit, with microstrip components added at transmit circuit, using simulated S-Parameters in ADS circuit. It should be noted this is the trickiest portion of the component selection process, as the matching is highly sensitive to the microstrip line geometry and needs to be precisely modeled for appropriate transmit circuit values in simulation.

As an example, the following describes this process for $half_{4,4}$ and $half_{4,1}$ at 1mm transmission distance and 700 MHz source frequency. The calculated values for C_2 are 4.4 pF for $half_{4,4}$ and 8.6 pF for $half_{4,1}$, from (2.6), for 700 MHz resonance. The simulated value of C_{par} from HFSS at 1mm distance was 0.48 pF for $half_{4,4}$ and 0.43 pF for $half_{4,1}$. After modeling the microstrip lines in ADS simulation, the adjusted values of C_2 were 2.0 pF (C_{sum} = 2.5 pF) for $half_{4,4}$ and 5.9 pF (C_{sum} = 6.3 pF) for $half_{4,1}$ for 700 MHz resonance. The calculated values of L_{half} from (4.1) were 6.0 nH for $half_{4,4}$ and 1.2 nH for $half_{4,1}$. Thus, to maintain 700 MHz resonance frequency with a half-wave rectifier with this extra inductance, the final selected value for the C_2 component was 1.2 pF for $half_{4,4}$ and 5.0 pF for $half_{4,1}$. Note that these values of C_2 are significantly smaller than the calculated value without compensation. Finally, values of L_m, C_m, and C_1 were chosen for optimal matching as listed in Table 4.1 for a sample of different designs to be examined in full system measurements.

Table 4.1: Component Values for Full System Measurement

	Freq	L_m	C_m	C_1	C_2
$half_{4,4}$	700 MHz	1.2 nH	0.2 pF	3 pF	1.2 pF
$half_{4,1}$	700 MHz	1.0 nH	0.2 pF	5 pF	5 pF
$bridge_{2,2}$	780 MHz	0.3 nH	0.2 pF	3.5 pF	3.5 pF
$bridge_{3,3}$	1000 MHz	1.5 nH	0.2 pF	5.1 pF	2.4 pF

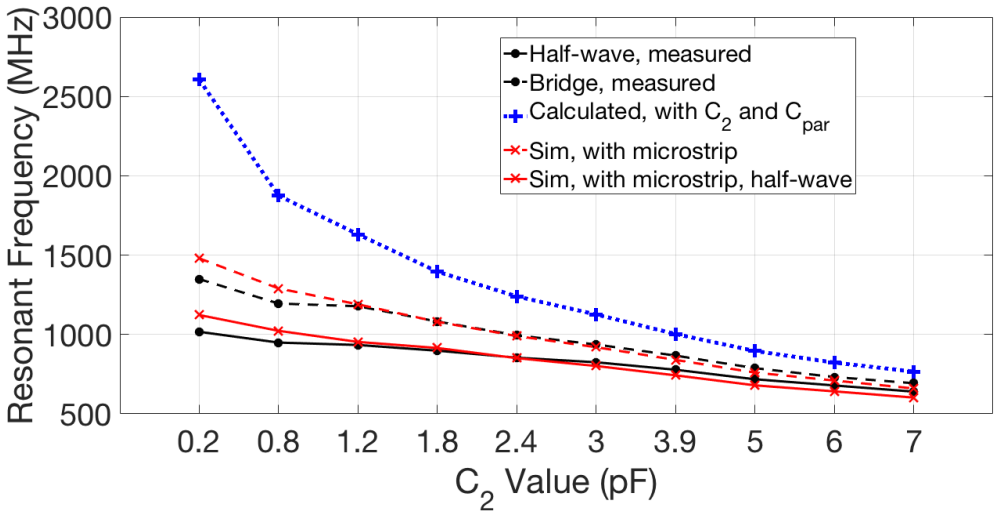

Figure 4.8: Comparison of the receiver resonant frequency with varying C_2 values for various measured and calculated data

To demonstrate the effectiveness of the modeling of the microstrip lines and L_{half} on the resonant frequency, a $bridge_{4,1}$ and $half_{4,1}$ link were measured with 14.5 dBm source and 1000Ω rectifier load and different values for C_2. For the transmit circuit, L_m and C_1 were short circuits and C_m was an open circuit. The source frequency was swept and the resonant frequency was determined from the source frequency giving the largest rectifier output voltage. The measured resonant frequency of these half-wave and bridge rectifiers is shown in Fig. 4.8. It can be seen that the calculation of the phase resonant frequency from (2.6), even including C_{par}, is much higher than the measured resonant frequencies. It can also be seen that the measured half-wave rectifier resonant frequency is lower than the measured bridge rectifier resonant frequency despite the identical circuits (aside from the rectifier topology), validating a downshift in frequency when utilizing a half-wave rectifier.

When modeling the resonant frequency from simulation with microstrip lines added,

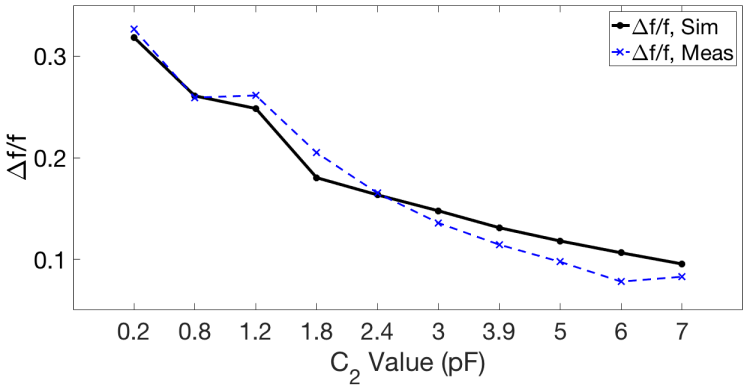

Figure 4.9: Change in measured and simulated resonant frequency between half-wave and bridge rectifier with different C_2

the simulated resonant frequency closely matches with the measured bridge resonant frequency. This is expected, as the bridge rectifier only needs to account for the effects of the parasitic capacitance and microstrip lines to determine the shift in resonant frequency. When adding the simulated value of L_{half} for each C_2 case, the simulated resonant frequency closely matches the half-wave measured resonant frequency. The simulated and measured frequency shift between the half-wave and bridge rectifier is shown in Fig. 4.9, where $\Delta f/f = \frac{f_{bridge} - f_{half}}{f_{half}}$. This shows that the extra inductance L_{half} appropriately models the frequency shift between the half-wave and bridge rectifier. The simulated resonant frequency is slightly higher than the measured data for the smallest values of C_2, likely due to the effect of capacitor mounting parasitics not included in the modeling. The error from mounting parasitics will be larger at higher frequency, with smaller C_2.

4.3 Reverse Power Distribution Network

4.3.1 Reverse PDN for Continuous Power Demand

In the designed system architecture, the RF diode rectifier is directly followed by a PDU. Lower frequency systems may use similar capacitance values for the voltage smoothing capacitor for the rectifier and the input capacitor for the PDU. For the LTC3564, an input capacitance of 4.7-22 μF is recommended. The self resonant frequency of any version of

this capacitor will occur far before the operating frequency of the rectifier. A capacitor on the pF scale is needed for the rectifier. However, when putting a pF capacitor and a μF capacitor in parallel, a very large parallel resonant peak will occur [87]. This leads to large voltage variation in the supply to the PDU.

To solve this issue, a reverse power distribution network is designed to successfully integrate the RF rectifier and PDU. The reverse PDN is a network of parallel capacitors designed to mitigate the parallel resonance between the smoothing capacitor and PDU input capacitor. The reverse PDN name arises from the fact a small value capacitor at the supply side is integrated with a large value capacitor at the chip, the reverse of what is seen in a digital PDN [88]. This name and development of the original idea of the reverse PDN was accomplished with postdoctoral researcher Dr. Anto K. Davis. First, the design of a reverse PDN for continuous power demand is presented. For continuous power output, both the PDU and rectifier create voltage ripple. Establishing a target impedance is a useful design metric, in the same way as conventional PDN design. The general form for the target impedance is defined in (4.3), where ΔV is the allowable voltage ripple and ΔI is the maximum transient current ripple.

$$Z_t = \frac{\Delta V}{\Delta I} \tag{4.3}$$

From the PDU perspective, the current ripple arises from the switching power inductor. The current ripple for a buck converter is given in (4.4), where D is the duty cycle, $V_{in,PDU}$ is the input voltage to the PDU, V_{out} is the output voltage of the PDU, D is the duty cycle, f_{sw} is the PDU switching frequency, and L_{SW} is the inductance (note that this was the same ripple current used to estimate the inductance AC loss in chapter 2). The reverse PDN is designed for the LTC3564 buck converter, which operates with a 'burst' mode. This means the converter delivers more energy to the load in shorter bursts and then shuts off circuitry until the output voltage falls below a specified value, at light loads. It is essentially a variant of discontinuous conduction mode (DCM), where the load is regulated in bursts as opposed

to typical DCM, and as such the current ripple will exceed the values typical for a given inductance and load. For the reverse PDN the max current ripple is set to the limit allowed by the LTC3564 - 360 mA. From this, the target impedance for the reverse PDN for the worst case scenario from the PDU side is given in (4.5).

$$\Delta I_{buck} = \frac{D(V_{in,PDU} - V_{out})}{f_{SW} L_{SW}} \tag{4.4}$$

$$Z_{t,PDU} = 2.78 \Delta V \tag{4.5}$$

A rectifier has guaranteed voltage ripple from the output voltage smoothing. The voltage smoothing ripple for a half rectifier is shown in (4.6), where $I_{load,rect}$ is the output current of the rectifier (and input current of the PDU), f_{rect} is the near field coupling and rectifier frequency, and C_s is the smoothing capacitance value of the rectifier. The total voltage ripple arising from the rectifier cannot be less than this value, irrespective of the target impedance. From this voltage ripple, the current ripple $I_{rip,rect}$ is calculated as shown in (4.7). Finally, the target impedance for the reverse PDN from the rectifier perspective is shown in (4.8), where $V_{in,PDU} = I_{load,rect} R_{in,PDU}$.

$$V_{ripple,half} = \frac{I_{load,rect}}{f_{rect} C_s} \tag{4.6}$$

$$I_{rip,rect} = \frac{V_{ripple,half}}{R_{in,PDU}} \tag{4.7}$$

$$Z_{t,rect} = \frac{\Delta V_{allowable,rect}}{\Delta I_{rip,rect}} = \frac{\Delta V_{allowable,rect}}{\frac{V_{in,PDU}}{R^2_{in,PDU} f_{rect} C_s}} \tag{4.8}$$

The total voltage ripple arising from the rectifier is the sum of (4.6) and (4.8), shown in (4.9). It can be seen that even if a large target impedance is set, the voltage ripple will not

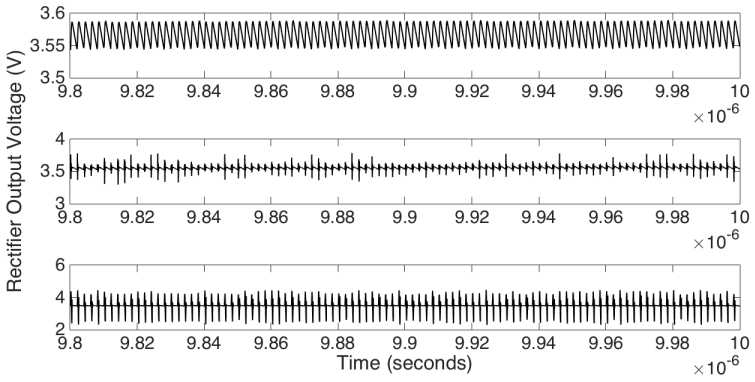

Figure 4.10: Simulated rectifier output voltage with 500 MHz rectifier with 100 pF smoothing capacitor with (a) ESL = ESR = 0 (b) ESL = 0.3 nH, ESR = 0.1Ω and (c) ESL = 5 nH, ESR = 0.3Ω

be largely affected as the input resistance of the PDU for this system will be at least a few hundred Ω. The more significant factor is the ripple from the rectifier voltage smoothing. Because of this, the reverse PDN phase is also an important consideration, as shown in Fig. 4.10. For the same value smoothing capacitor, the equivalent series resistance (ESR) and equivalent series inductance (ESL) are changed in a series of 3 simulations in Keysight ADS. When the ESR = ESL = 0 (ideal capacitor), the voltage ripple equates with (4.6). As the ESR and ESL increase (the phase becomes less ideal), the voltage ripple increases.

$$V_{rect,allowable} = (1 + \frac{Z_{t,rect}}{R_{in,PDU}})V_{ripple,half} \tag{4.9}$$

The voltage ripple may be split into two parts: the consistent voltage ripple and peroidic voltage spikes. The periodic voltage spikes arise from the impedance of the reverse PDN, and will be controlled so long as a reasonable target impedance is set. The consistent voltage ripple comes from (4.6), and as the phase becomes less ideal, the equivalent capacitance of the reverse PDN will decrease and lead to increased voltage ripple. To better approximate the smoothing voltage ripple, the simulated Z-Parameters of the reverse PDN capacitor network are converted to an equivalent T-circuit model, shown in Fig. 4.11. A T-circuit model is chosen because an admittance based model (such as a Pi-circuit model)

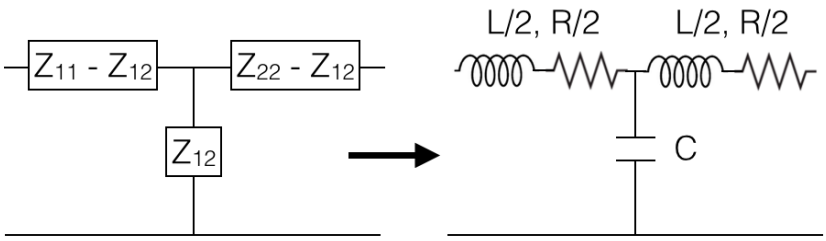

Figure 4.11: Equivalent T-circuit model for the reverse PDN capacitor network

is not accurate at high frequency. Also, the T-circuit model, with a capacitor as the only shunt component, is an intuitive model to use for a network of parallel capacitors.

As an example, a reverse PDN with 6 capacitors was simulated as the smoothing capacitance for a 700 MHz half wave rectifier with 14.5 dBm power source and 1000 Ω load. Each capacitor had ESL = 0.3 nH, ESR = 0.5 Ω, and 0.5 mm of microstrip line between each parallel capacitor (the approximate the effects on a fabricated system). The first five capacitor values were 30 pF//100 pF//600 pF//2 nF//2 nF, and two cases were simulated for the final capacitor C_6: 2nF and 20 nF. From (4.6), the voltage ripple should be around 4x less with a 20 nF capacitor, as the total parallel capacitance is 6.7 nF when C_6 = 2 nF and 24.7 nF when C_6 = 20 nF. Figure 4.12(a) shows the smoothing voltage ripple is the same for both cases. While the capacitance in the extracted T-circuit model is equal to the total capacitance at low frequency, it is approximately the same at 700 MHz as shown by Fig. 4.12(b). Using this value in (4.6) gives a smoothing voltage ripple of 3 mV, approximately the same value as in the ADS simulation. The design of the reverse PDN needs to both limit the impedance to prevent large voltage spikes and control the phase to have enough effective smoothing capacitance at the near field coupling frequency to limit the smoothing voltage ripple.

A simple demonstration of the reverse PDN was designed for the $half_{2,2}$ system at 820 MHz with the LTC3564, first just considering the contribution of the PDU on the voltage ripple. For a voltage ripple specification of 150 mV, the target impedance is 417mΩ. For this demonstration, the voltage smoothing capacitor has value 330 pF, and the PDU input

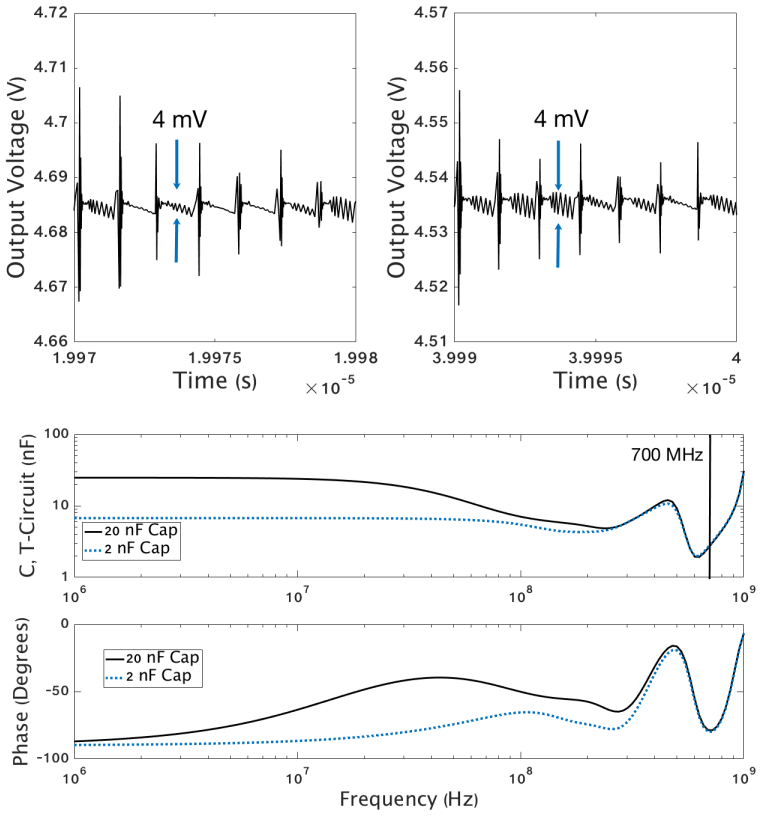

Figure 4.12: (a) Comparison of the simulated rectifier output voltage when C_6 = 2 nF (left) and 20 nF (right) (b) Capacitance in the equivalent T-circuit model for both simulated reverse PDN cases and (c) Phase of each reverse PDN case

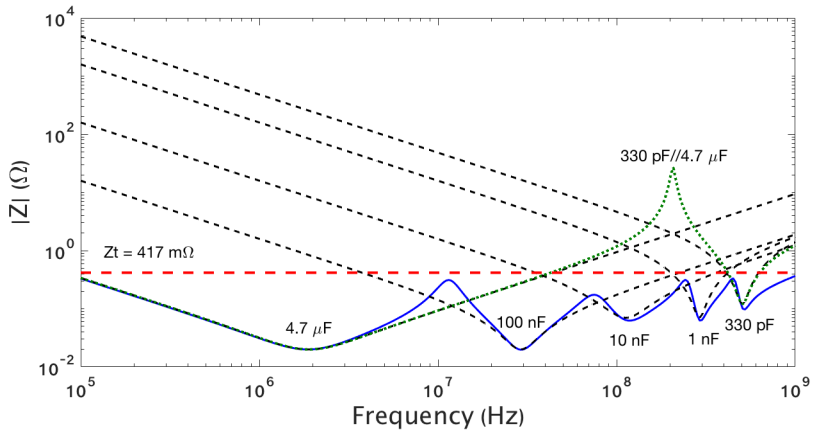

Figure 4.13: Impedance profile of each individual capacitor and the total parallel combination for 5 capacitor reverse PDN demonstration

capacitor has value 4.7 μF. The Z-Parameters of different value capacitors were calculated with manufacturer provided ESR and ESL for each capacitance value. When just the 330 pF and 4.7 μF capacitor are in parallel, a large parallel resonance occurs at 200 MHz, such that the target impedance is exceeded between 40 and 400 MHz as shown in Fig 4.13. From interposing the impedance profile of different capacitor combinations, it was determined that adding three capacitors -1nF, 10nF, and 100nF-between the 330 pF and 4.7 μF was sufficient to meet the target impedance as shown in Fig. 4.13. The capacitance values were chosen closer together at the low end because lower value capacitors have higher ESR [87], increasing the impedance minimum of these capacitors. The crossing of individual capacitor impedance profiles for larger valued capacitors needs to have a comfortable margin under the target impedance, as the low ESR of these capacitors leads to an increased parallel resonant peak, while the opposite is true for the smaller valued capacitors, as seen in Fig. 4.13.

The reverse PDN capacitor selection was verified with a subsequent Keysight ADS simulation of these five capacitors in parallel, with 0.5mm of microstrip line between them to model the design in the fabricated system. The simulated impedance of this network is shown in Fig. 4.14. This impedance profile is compared to a capacitor network with 4x330pF in parallel with the 4.7 μF PDU input capacitor such that the number of capacitors

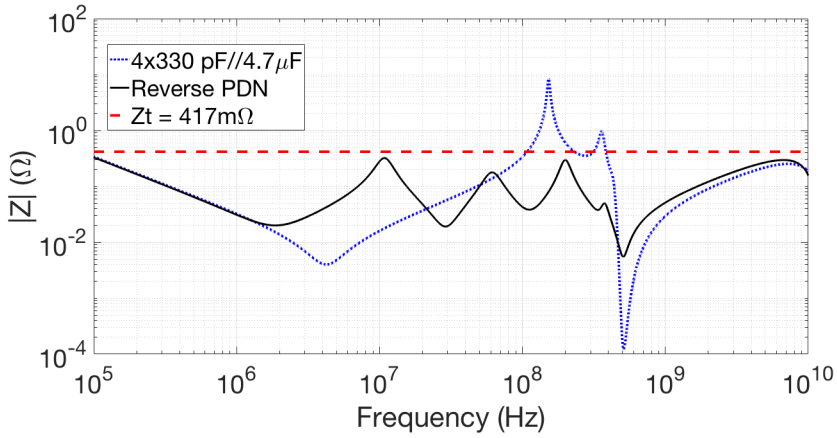

Figure 4.14: Comparison of the simulated impedance profile for the 5 cap reverse PDN and cases without the reverse PDN

in each case is the same, as will be compared in measurement. The reverse PDN meets the target impedance specification, while the case without the reverse PDN has a large parallel resonant peak impedance (9Ω). This large parallel resonant peak destabilizes the PDU input voltage and can lead to significant loss in the system.

The two cases were measured with a 1 mm separation with the $half_{2,2}$ system and LTC3564 with 1 μH SMT inductor, with the tested receiver board shown in Fig. 4.15. The output voltage was fixed at 1.2V and measured with 138Ω resistor load (10 mW). The system was measured with a 820 MHz source from a HP 8648D signal generator. The same receiver board is used in both cases. The reverse PDN uses 0603 package X7R surface mount capacitors of values 330 pF//1 nF//10 nF//100 nF at the reverse PDN area in Fig. 5, and the second case uses 4x330 pF capacitors in the same location.

For the reverse PDN case, the PDU was able to regulate the 1.2V, 10 mW output with 13.1 dBm input power. At this same input power, the case without the reverse PDN is unable to regulate the output. When the input power was increased to 13.7 dBm, the second case was able to regulate the output successfully. The large parallel resonance in the case without the reverse PDN introduces an additional source of power loss to the system. Without the reverse PDN, the system efficiency was 44.6%, while the system efficiency with the reverse PDN was 51.2%. This 6.6% system efficiency difference is solely accounted for by

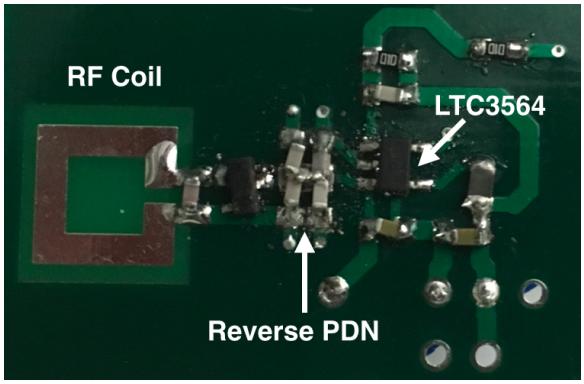

Figure 4.15: Fabricated receiver circuit with 5 cap reverse PDN for $half_{2,2}$

the capacitor selection and reverse PDN design, as the same circuit was used in both measurements, identical in every other way. This demonstrates the importance of the reverse PDN in RF WPT to link RF-DC conversion with a PDU.

For more through demonstration of the necessity of the reverse PDN and design process, a reverse PDN was designed for the $half_{2,2}$ system at 860 MHz, this time accounting for the rectifier ripple and more thorough consideration of layout effects. For this example, the buck converter output is 1.2V with 200Ω load with a 1 μH power inductor. From (4.5), for 50 mV allowable voltage ripple specification, the target impedance is 0.14Ω. From the rectifier side, the input resistance to the buck converter is determined from R_{Load}/D^2, and is calculated as 868Ω. From (4.9), even if the target impedance is set to 0.14Ω, the contribution of the PDN impedance from the rectifier current ripple to the overall voltage ripple is very small. The effective smoothing capacitance is the more significant factor. For this demonstration the system operates at 860 MHz. Assuming 10 mV allowable voltage ripple specification from the rectifier, the effective smoothing capacitance needed from (4.6) is 335 pF.

All capacitors used are SMT ceramic in 0603 package of 3 types: (i) C0G capacitors for small pF capacitance, (ii) X7R for intermediate value (100 pF-100nF) capacitance and (iii) X7R for large (100 nF and greater) capacitance. To simplify design, the ESL values and ESR values are modeled from manufacturer supplied data for a capacitor of each type.

These values are then used in the design as the default values for each of the three categories. The ESL was modeled as a single value inductance. The ESR of the capacitors is much more frequency dependent, especially over the range considered. Manufacturer supplied 2 port series S-parameters were converted to the equivalent 1 port S-Parameter with just the resistance characteristic. This data was then used as a frequency dependent resistor in ADS, with a separate characteristic for each capacitor category as the ESR varies considerably with capacitance value for ceramic capacitors [87].

In the fabricated structure, two parallel lines are used to conserve area, with the ground of both capacitor lines connected to the ground plane shared with the PDU through vias. The transmission lines and vias are modeled directly through ADS components, while the spreading inductance in the ground plane is approximated as seen in [[87], eq. (6.72)]. The capacitor value selection followed using the impedance sculpting method for decoupling capacitor selection in a conventional PDN [87], in a similar process as Fig. 4.13. The designed reverse PDN uses 13 capacitors (6 pF//20 pF//47 pF//100 pF//220 pF//470 pF//1000 pF//22 nF//47 nF//100 nF//330 nF//1μF//4.7μF) to meet the target impedance for the PDU, the smoothing capacitance for the rectifier, and with at least 5 μF capacitance at the input of the PDU. In practice, fewer capacitors may be used with no noticeable drop in efficiency, as the LTC3564 can tolerate a fairly large amount of voltage ripple. However, for the purpose of examining general integrated solutions for all RFNFC systems in this dissertation, the methodology for a reverse PDN for any RFNFC system needs to be demonstrated. The impedance profile of the designed reverse PDN is shown in Fig. 4.16. The target impedance requirement for the PDU is met, while the effective capacitance is 700 nF at 860 MHz and 5 μF at 2.25 MHz, meeting the capacitance requirements for both the PDU and the rectifier. The reverse PDN does not become inductive until after 1 GHz, despite the large amount of capacitance in the circuit.

The $half_{2,2}$ system was measured at a transmission distance of 1mm with a 14.5 dBm, 860 MHz source to power a 200 Ω resistor with 1.2V regulated output. The system was

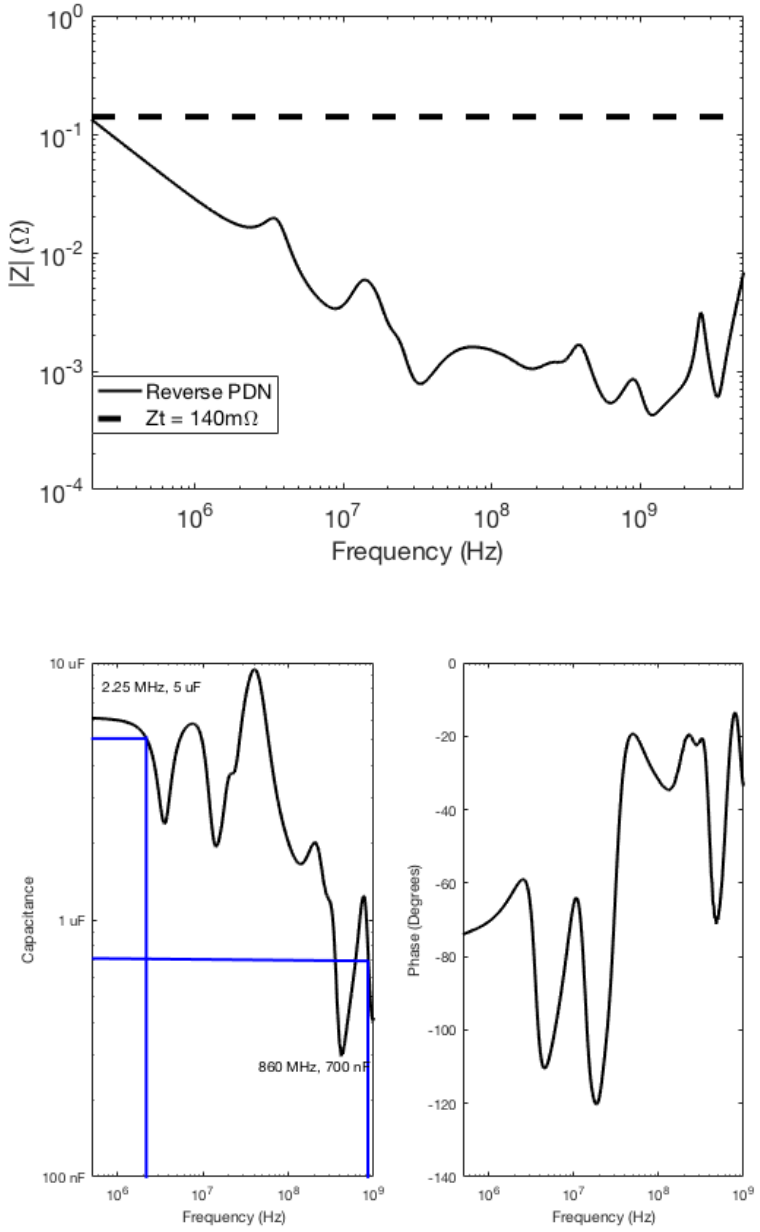

Figure 4.16: Designed reverse PDN (top) impedance magnitude and (bottom) effective capacitance and phase

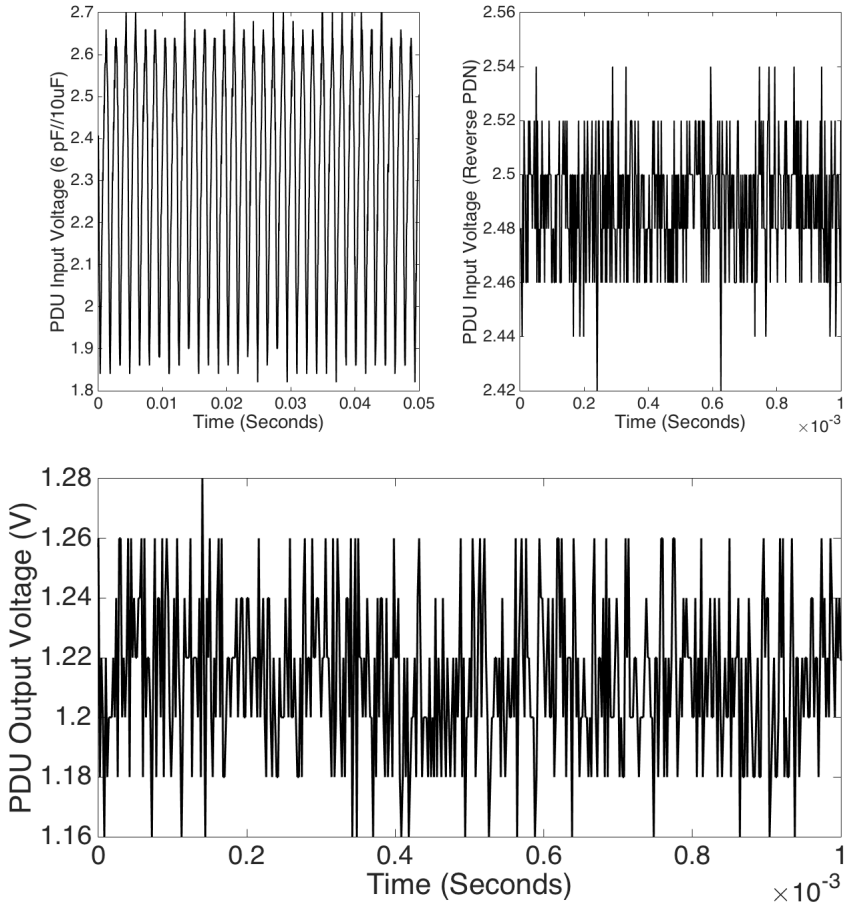

Figure 4.17: (Top) Measured PDU input voltage for both capacitance cases and (bottom) measured PDU output voltage for system with the reverse PDN

measured for two capacitor combinations between the rectifier and PDU: (i) a 6 pF capacitor and 10 μF capacitor in parallel and (ii) the designed reverse PDN capacitor network (starting with 6 pF and ending with 4.7 μF). When just the two capacitors were used, the system was unable to supply and regulate the needed 1.2V output. As expected, the strong parallel resonance between the two capacitors leads to unmanageable PDU input voltage ripple, shown in Fig. 4.17. In contrast, the system with the reverse PDN integrated shows much lower PDU input voltage ripple and successfully regulates the output as designed.

A reverse PDN is designed for all two coil systems using the same impedance sculpting method for the capacitors. 50 mV of allowable ripple is set for the allowable voltage ripple from the PDU, giving a target impedance of 114 mΩ from (4.5). This same target

impedance is set for the rectifier, and from (4.8) if this target impedance is met at higher frequency there will be negligible ripple contribution from the voltage spikes as $R_{in,PDU}$ will be at least 500 Ω. Second, the effective smoothing capacitance needs to meet the standard from 500 MHz to 1100 MHz (the span of frequency examined for the near field coupling system in this dissertation). The maximum value of $I_{Load,rect}$ occurs at the minimum LTC3564 operating voltage (2.5V) and maximum power output (around 20 mW), for maximum 10 mA rectifier output current. From this, the effective smoothing capacitance needed in this frequency range is 2000 pF for a half wave rectifier. For the systems with a bridge rectifier, the ripple will be half, thus if the half-wave rectifier smoothing capacitance specification is met, then the bridge must be as well. The total voltage ripple should be less than the sum of these two, or 60 mV.

The reverse PDN was designed with the same process as before. The designed reverse PDN has the simulated impedance profile shown in Fig. 4.18, consisting of 11 capacitors in parallel (100 pF//220 pF//470 pF//1 nF//3.3 nF//10 nF//33 nF//100 nF//330 nF//1 μF//4.7 μF). The reverse PDN impedance does not become inductive (positive phase) until after 1.1 GHz, despite 6.2μF total capacitance in the circuit. Both the target impedance and effective smoothing capacitance specifications are met, and at 2.25 MHz (the switching frequency for the buck converter) there is 6.2 μF capacitance, meeting the input capacitance requirement for the regulator. This reverse PDN is applicable to all measured full systems, though the full systems in chapter 6 might use a few less capacitors, as allowable, for systems operating at lower power (less $I_{Load,rect}$ or higher frequency).

4.3.2 Reverse PDN for Discontinuous Power Demand

The design of the reverse PDN to integrate large storage capacitance is different than the continuous power system. With mF capacitance at the rectifier output, the smoothing voltage ripple will not be an issue, even at 1 GHz. The issue is the rectifier DC output voltage can decrease without the reverse PDN. This is shown through the T-circuit model. If the

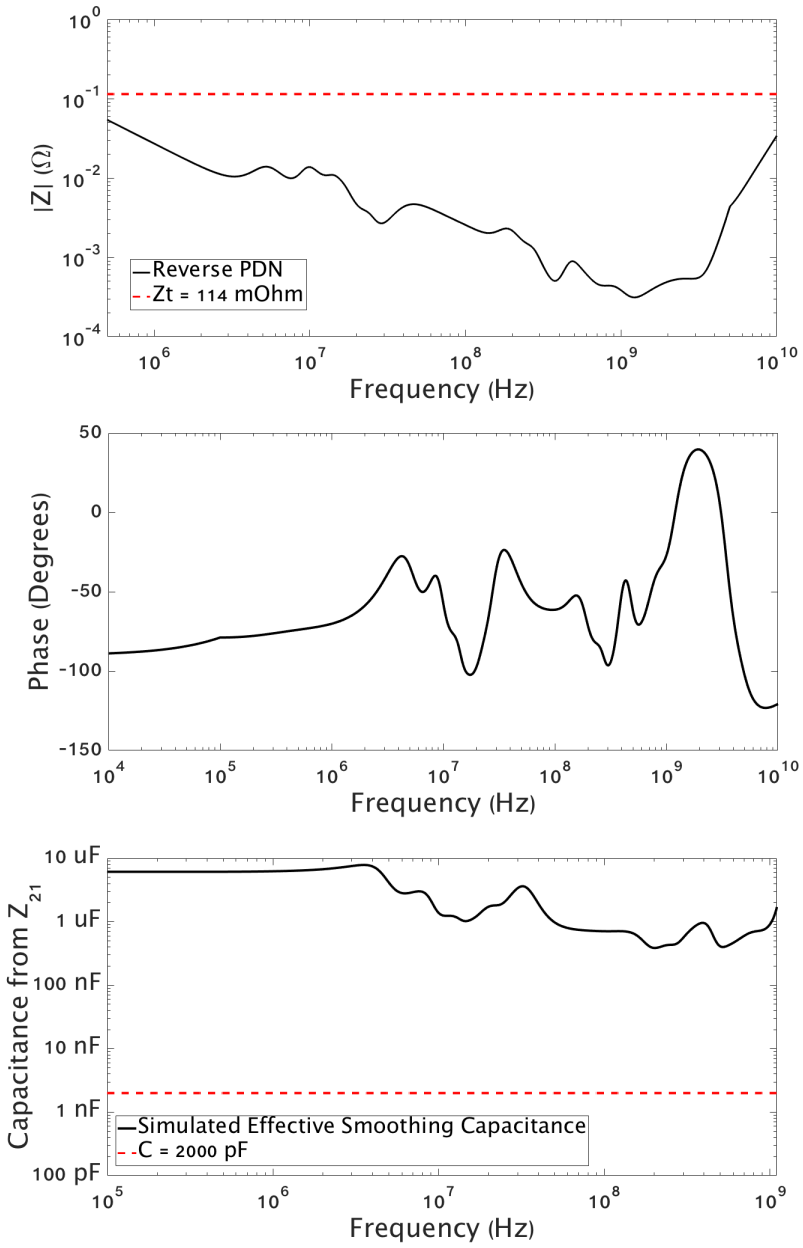

Figure 4.18: (a) Impedance of the designed reverse PDN and (b) Phase of the designed reverse PDN and (c) Effective smoothing capacitance value extracted from T-circuit model

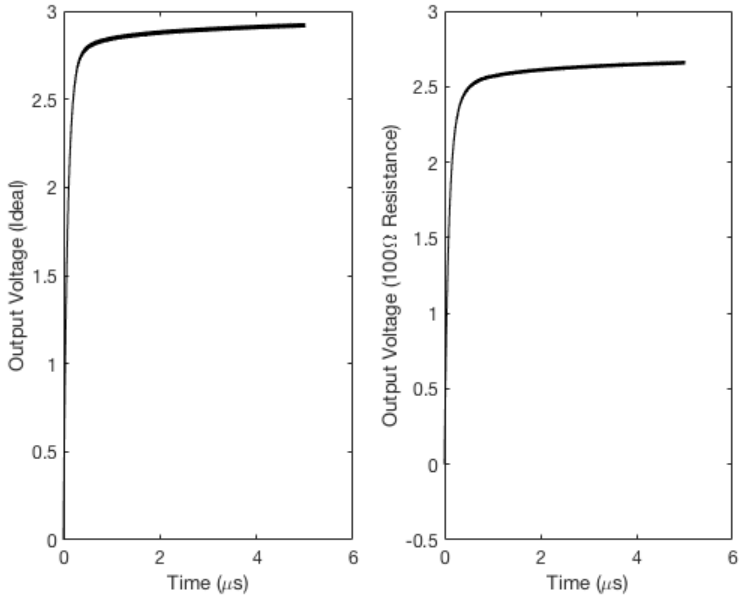

Figure 4.19: (Left) Simulated rectifier open circuit voltage with C = 100 pF (right) with 100Ω equivalent PDN resistance with C = 100 pF

T-model equivalent resistance of the capacitor network is large, the rectifier open circuit voltage decreases. In Fig. 4.19, a half wave rectifier operating at 1 GHz is simulated in ADS with open circuit load and T-circuit model output capacitor for two cases: i) C = 100 pF and L = 0 nH, R = 0Ω and ii) C = 100 pF, R = 100Ω, and L = 0 nH. The DC voltage is decreased in the latter case, though minimal voltage ripple is observed in both cases. To prevent drop in rectifier DC output, the reverse PDN target impedance in the equivalent T-circuit model is set at 1Ω.

Lead based aluminum electrolytic capacitors are selected for the mF capacitance in the reverse PDN. Even though electrolytic capacitors are polarity dependent, using them in the rectifier output ensures the voltage across the capacitor terminals will never be negative. Lead based are preferred over SMT because SMT electrolytic capacitors would need increased length of transmission line, leading to a larger shift in resonant frequency as shown earlier. A reverse PDN was designed with 4 ceramic capacitors (100 pF, 10 nF, 1 μF, and 100 μF) and 4 electrolytic capacitors (1 mF, 2x4.7 mF, 10 mF), using the same design

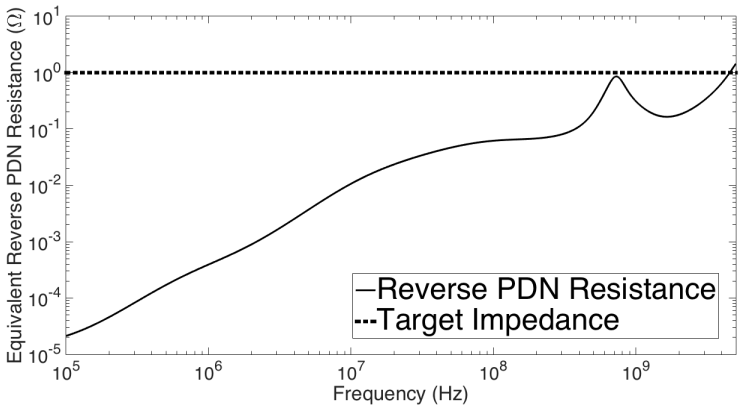

Figure 4.20: Extracted T-circuit model resistance of the simulated 4 coil system reverse PDN

process as for the two coil system. The T-circuit model was extracted from the simulated reverse PDN. The extracted resistance is shown in Fig. 4.20, and is less than the 1Ω target impedance set for the design.

A measurement of the designed 4 coil system with a half-wave rectifier was completed with 967 MHz source frequency at a 30 mm transmission distance. The measurement was completed with both the designed reverse PDN as the rectifier output capacitor network and a 100 pF capacitor in parallel with a 22 mF electrolytic capacitor as the rectifier output capacitor network. A comparison of the output voltage for the two cases is shown in Fig. 4.21. The output voltage with the reverse PDN is 1.5V compared to 0.8V for the two capacitor case. This is almost a 4x increase in the energy stored when integrating the reverse PDN. This demonstrates the suitability of the reverse PDN for integrating large storage capacitance with a RF rectifier in addition to successfully integrating a RF rectifier and PDU.

4.4 Summary

This chapter examined the integration challenges following the design of the subsystems. When integrating the complete RFNFC system, various issues arises that must be remedied through modeling and design. One of these issues are various resonant frequency detuning

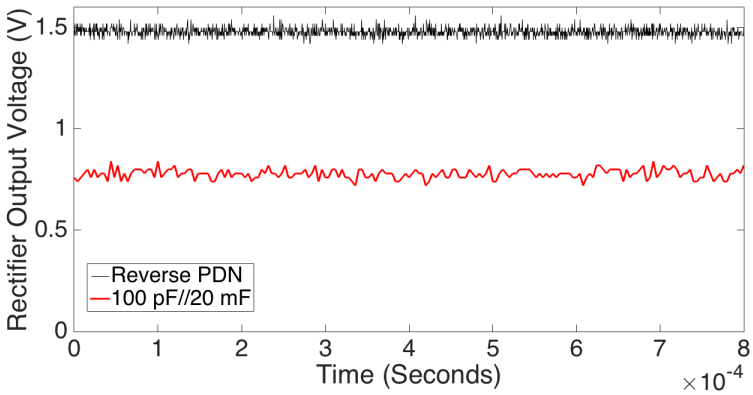

Figure 4.21: Comparison of measured rectifier output voltage in 4 coil system between 2 cap case and the reverse PDN

effects as demonstrated in this chapter through measurements, with various modeling solutions presented to guide effective selection of circuit component values. The second issue is the integration of the RF-DC conversion with a PDU, solved through the innovative use of a reverse power distribution network. The design metrics for the reverse PDN, namely target impedance and phase considerations, were presented in this chapter and the necessity of the reverse PDN was then demonstrated through measurement.

CHAPTER 5
INTEGRATED INDUCTOR FOR LIGHT LOAD APPLICATIONS

The previous chapters outline the design of a RFNFC system, discussing the efficiency and modeling challenges for each part of the system. Due to the unique goal of achieving a high efficiency system with RF source, various integration challenges arise from electromagnetic effects that other WPT systems do not need to account for. In the preceding chapter, these issues were identified and solutions presented.

One last part for a complete, fully integrated WPT system is needed: the integration of embedded passives through advanced packaging technologies. This chapter discusses the fabrication and integration of embedded inductors with NiZn ferrite epoxy composite magnetic core into the final design. The fabrication and characterization details are outlined, discussing the advantages of the technologies utilized. A comparison between the designed components and prior art is also provided.

Integrated inductor design for two separate cases is examined. First, the design of package embedded inductor for a system in package implementation of a WPT system with integrated buck converter is investigated. In this case, the fabrication and characterization of the inductors are thoroughly explored, with a discussion about the application of these inductors to fully integrated systems such as mentioned in the future work section of Chapter 7. Second, integrated inductor design for a Texas Instruments TPS62615 synchronous buck converter for light load (1-10mW) applications is examined and compared to a SMT inductor. A revised loss analysis is provided in this second case and used to demonstrate an integrated inductor with higher efficiency in the designed WPT system than a comparable SMT inductor. This chapter is unique in that much of this work was collaborative. The contributions of postdoctoral researcher Dr. Mohamed L. F. Bellaredj and Ph.D. student Hakki Torun are noted where appropriate.

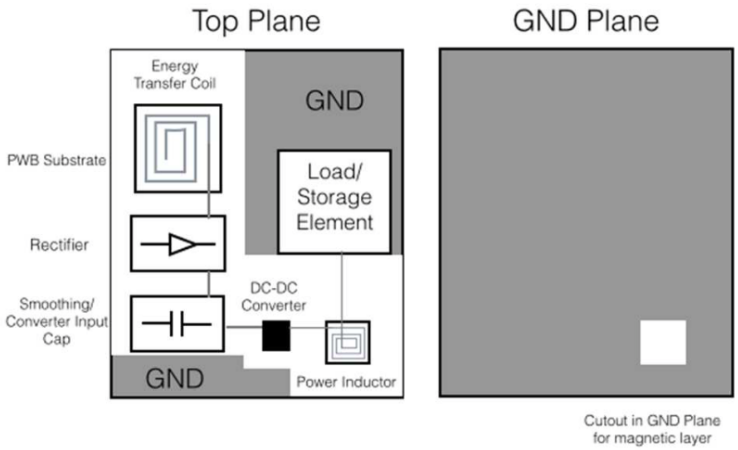

Figure 5.1: Example system in package implementation for RFNFC system with integrated inductor

5.1 Package Embedded Inductor for 10 MHz Integrated Buck Converter

5.1.1 System Architecture and Loss Analysis

The first case for integrated inductor considers a fully integrated, 1 GHz system in package (SiP) RFNFC system, such as shown in Fig. 5.1. As shown, the losses in the source, coil, and rectifier are dominant, such that the buck converter and inductor losses need to be minimal. As an example, the buck converter chip in Fig. 5.1 uses Global Foundries (GF) 130 nm process with a 3V input voltage. The chip, discussed in [89], has multiple conversion ratios and the 3:1V conversion ratio is used for this discussion. The inductor DC ($P_{Ind(DC)}$) and AC ($P_{Ind(AC)}$) power losses for the buck converter can be estimated as given in (2.16)-(2.17). The buck converter losses can be estimated using:

$$P_{Buck_{(Cond)}} = R_{SW}(I_{Load}^2 + \Delta I_{RMS}^2) \tag{5.1}$$

$$P_{Buck_{(Switching)}} = f_{SW}[C_{GSN}(\frac{V_{in}}{2})^2 + 2C_{GDN}(\frac{V_{in}}{2})^2 + C_{GSP}(\frac{V_{in}}{2})^2 + 2C_{GDP}(\frac{V_{in}}{2})^2] \tag{5.2}$$

$$\Delta I_{RMS} = \frac{\Delta I_{pk-pk}}{2\sqrt{3}} \tag{5.3}$$

where $P_{Buck_{(Cond)}}$ is the conduction loss in the buck converter transistors, $P_{Buck_{(Switching)}}$ is the buck converter switching losses calculated using the various gate capacitances with C_{GSN} = 0.813 pF, C_{GDN} = 0.583 pF, C_{GSP} = 0.71 pF, C_{GDp} = 0.59 pF, and R_{SW} is the resistance of the transistor switches [89]. For the GF 130nm process, the transistor resistances and capacitances were modeled for V_{in} = 3V, V_{out} = 1V, and output power of 50 mW. The quality factor Q for a power inductor can be defined as:

$$Q = \frac{\omega L}{R_{AC}} \tag{5.4}$$

where the Q factor takes into account both the winding and core losses. At 10 MHz, assuming a quality factor of 25 and a DC resistance of 600 mΩ for the inductor, an efficiency in the range of 82% - 92% is possible for inductances in the range of 200 nH-800 nH as shown in Fig. 5.2. Thus in this proposed SiP RFNFC implementation, the focus is on the design, fabrication and characterization of embedded planar power inductors where the inductance is in the range of 200-800 nH, a DC resistance less than 600 mΩ, and a quality factor of 25 or greater to ensure a buck converter efficiency higher than 80%.

5.1.2 Integrated Inductor Design

Planar spiral inductors have been shown to provide high inductance density and hence are used here, as shown in Fig. 5.3(a). The critical design parameters are the outermost length, d, metal trace width, w, the trace separation s, and number of turns, N. The inductor is designed both on a 2 layer PWB core of thickness 0.79 mm and 0.2 mm, as shown in Fig. 5.3(c) where the 0.2 mm thickness makes the substrate semi-flexible. The inductor windings are defined on the top while a ground plane is provided on the bottom layer with an void (cutout) in the ground plane beneath the inductor as shown in Fig. 5.3(b). The

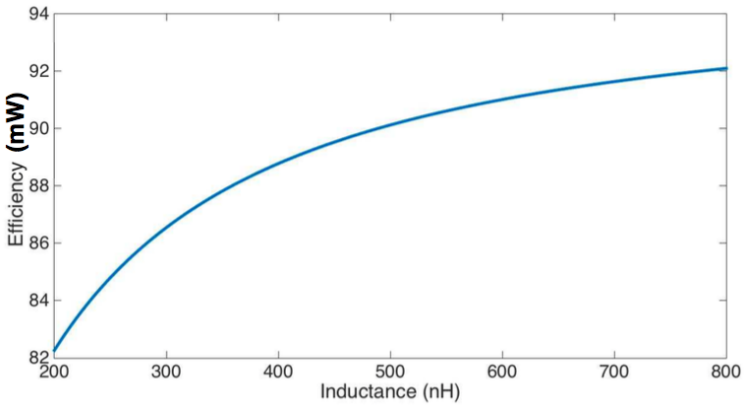

Figure 5.2: Plot of efficiency of the buck converter plus inductor stage, for the examined architecture. The inductor is assumed to have a quality factor 25 and DC resistance of 600 mΩ

cutout helps increase the inductance and Q factor of the inductors, leading to reduced area and losses as with the RF coils.

The magnetic material is applied to one or both sides of the inductor. For the double-sided case, inductance is increased over the single sided case due to the presence of the magnetic field in the magnetic material on both sides of the inductor. As a comparison, three structures have been designed and fabricated as shown in Fig, 5.3(c): air core inductor, single layer magnetic material inductor (on one side of the PWB) and two layer magnetic material inductor (on both sides of the PWB). By examining these various layer combinations with the different substrate thicknesses, the characterized inductors give comprehensive insight to the influence of the magnetic core on the inductor characteristics.

At 10 MHz, the magnetic material can introduce additional AC losses. The magnetic material used is a Nickel Zinc (NiZn) ferrite epoxy composite with a volume loading of 0.78, with details available in [90]. The magnetic composites used in this dissertation were designed and fabricated by Georgia Tech postdoctoral researcher Dr. Mohamed L.F. Bellaredj. To accurately model the inductor, the electromagnetic properties of the magnetic material are required. The measured permeability and permittivity spectrum of the NiZn ferrite composite magnetic material up to 100 MHz is shown in Fig. 5.4, measured by Dr. Bellaredj. Dr. Bellaredj synthesized the magnetic material from FP350 NiZn ferrite

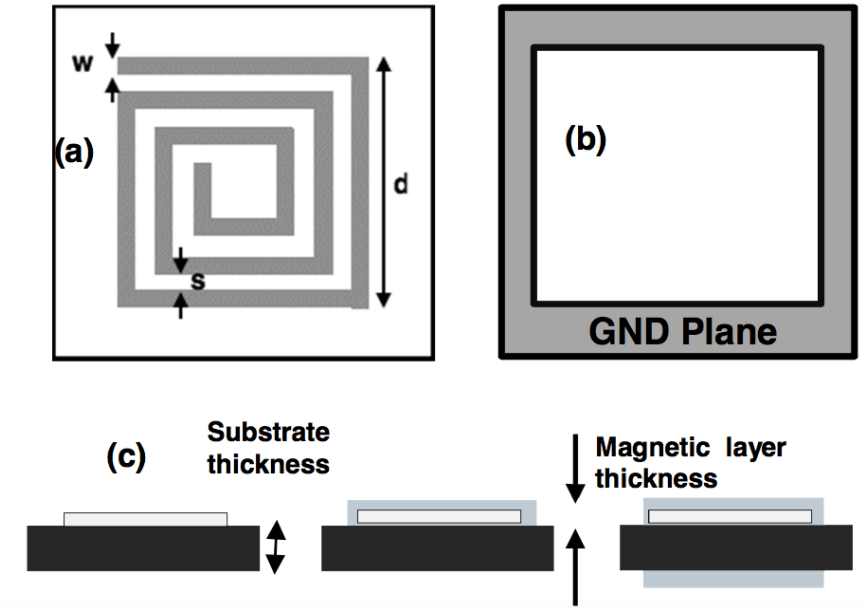

Figure 5.3: (a) Spiral inductor parameters of the top plane and (b) the bottom ground plane and (c) Side view of inductor with no magnetic layer, top magnetic layer, and top and bottom magnetic layer.

powder from pptechnology, prepping the powder with a variety of washing and jar rolling procedures, and then adding it to epoxy material. More detailed procedures on this process are available in [90]. This process results in ideal dispersion of the powder in the epoxy, and ideal viscosity of the ferrite power/epoxy composite for screen printing on organic substrate. Samples of the NiZn composite were fabricated using toroid aluminum molds. The dielectric and magnetic properties of the material were measured with a Keysight 4291B RF Impedance/Material Analyzer with 16453A Dielectric Material Test Fixture and 16454A Magnetic Material Test Fixture, from a frequency of 1 MHz to 400 MHz. The composite has a relative permeability of 9.3, magnetic loss tangent of 0.25, relative permittivity of 6.3, and dielectric loss tangent of 0.01 at a frequency of 10 MHz, which corresponds to the switching frequency. Notice μ_r peaks between 10-30 MHz while the magnetic loss tangent is slow to rise in this range - making this the optimal frequency range to apply the magnetic composite to integrated inductor design.

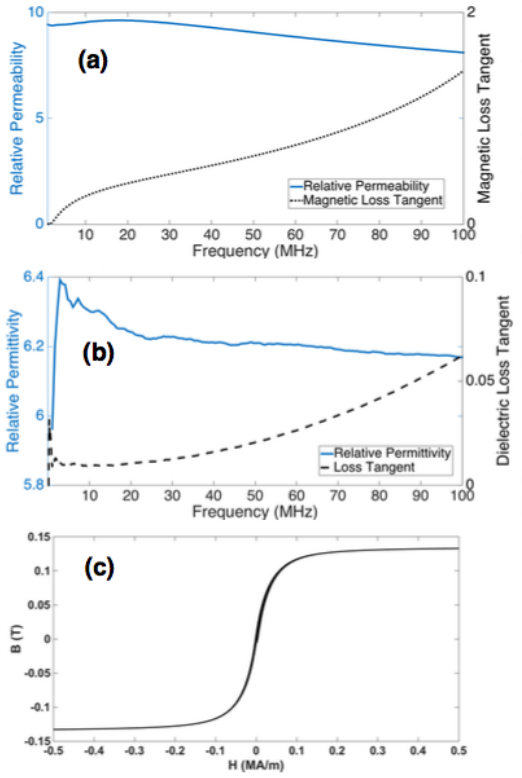

Figure 5.4: (a) Permeability and magnetic loss tangent measurements for the NiZn ferrite composite material (b) Permittivity and dielectric loss tangent measurements and (c) Hysteresis curve measurement

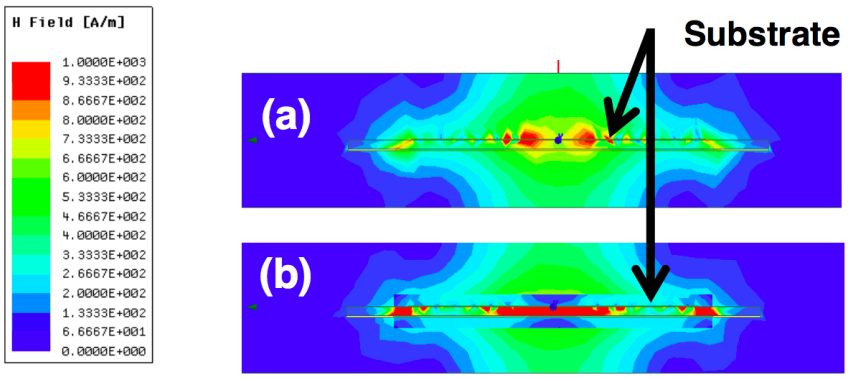

Figure 5.5: Simulated magnetic field strength on a plane centered on the inductor, viewed from the side for (a) air core and (b) double sided magnetic core inductor

5.1.3 Spiral Inductor Design and Modeling

The inductors were designed using HFSS to accurately estimate the AC losses at 10MHz. FR4 material (ϵ_r = 4.5, tan(δ) = 0.02) was used as the substrate to ensure low cost with thicknesses of 0.2 mm and 0.79 mm. The copper traces have a thickness of 35 m with trace width (w) and spacing (s) ranging from 100 to 250 μm. As seen in the inductor side cross section in Fig. 5.5, the application of magnetic material concentrates the magnetic field strength in the area of the inductor for increased inductance.

For initial simulations, a magnetic material thickness of 50 μm-600 μm was used - consistent with the thicknesses attained by the stencil printing process (50-600 μm) described in the following section. Figure 5.6 shows the effect of the magnetic layer thickness and the substrate thickness on the inductance and resistance at 10 MHz. For a spiral geometry of d = 7.5 mm, w = 0.15 mm, s = 0.20 mm, and N = 7, the magnetic layer thickness on both the top and bottom layer was swept for both a 0.79 mm thick and 0.2 mm thick PWB. As the magnetic layer thickness increases, both the inductance and the ac resistance increase, as expected. For the 0.2 mm thick, flexible substrate, the inductance and resistance increase is more significant due to the decreased distance between the bottom magnetic layer and spiral inductor. Since the core losses in the inductor must be carefully balanced with the inductance increase, a target magnetic layer thickness of 200-400 μm is desired. The in-

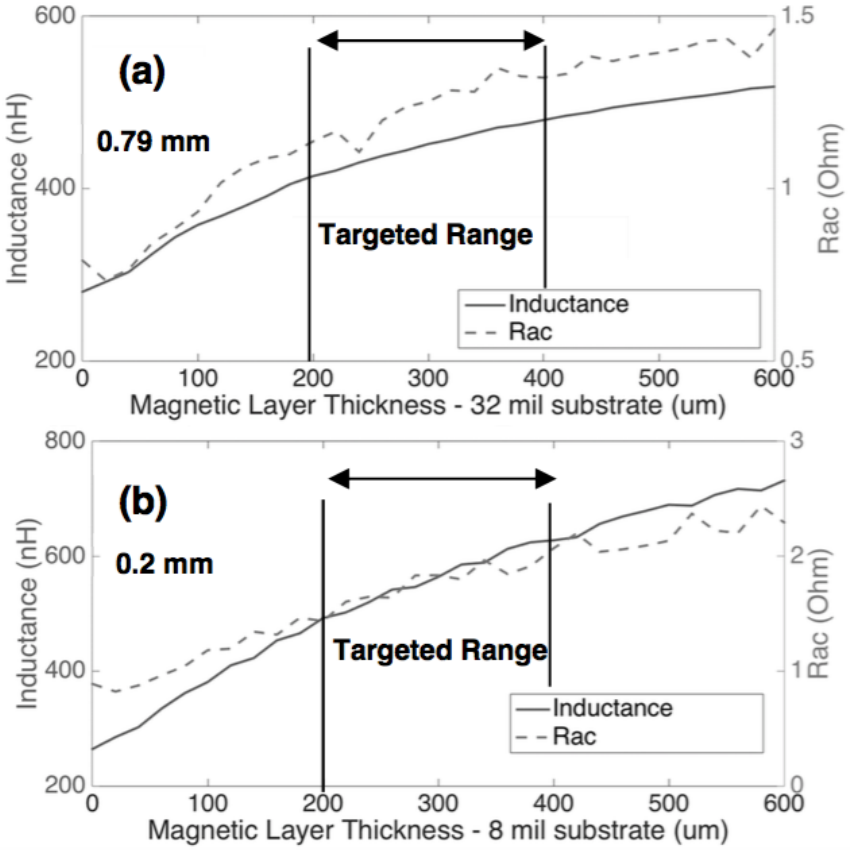

Figure 5.6: Plots of the simulated inductance and R_{AC} with increasing magnetic layer thickness, same for both layers, for (a) 0.79 mm thick substrate (b) 0.2 mm thick substrate

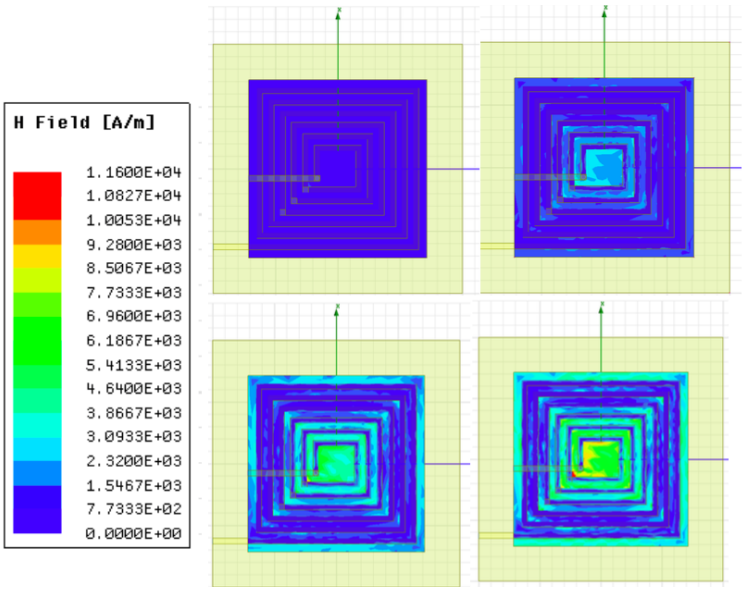

Figure 5.7: Simulated magnetic field strength with current excitation of (a) 100 mA (b) 500 mA (c) 1.0 A (d) 1.5 A

ductance and inductance density is less than desired with less than 200 μm thickness, and the quality factor can fall below 25 with greater than 400 μm thickness. This magnetic layer thickness range has sufficiently small ac resistance to have allowable quality factor for both substrate thicknesses while significantly increasing inductance from the magnetic layer.

Magnetization measurements were performed on the NiZn ferrite epoxy composite and the results showed that magnetic composite material saturates at 0.13 Tesla. From B = μH, with the saturating magnetic flux density B and permeability μ already known for the material, a HFSS simulation of the magnetic field strength as a function of inductor current can provide an estimate of the saturation current. This is shown in Fig. 5.7, where the inductor 1 geometry was simulated with a top magnetic layer of 0.3 mm thickness for varying current excitations. The magnetic field strength does not reach the saturation condition until approximately 1.5A, which is far greater than the currents typical for these low power applications. Thus it can be assumed the magnetic core will not saturate for the normal operation of these inductors.

Table 5.1: Spiral Inductor Geometries

$Inductor\#$	$d(mm)$	$w(mm)$	$s(mm)$	N turns	$R_{DC}(m\Omega)$	$L(nH)$	Peak Q	Peak Q Freq (MHz)
1	5.94	0.23	0.23	5	171	200	27	12
2	5.94	0.15	0.15	6	337	374	26	14
3	8.38	0.23	0.23	7	333	436	29	14
4	7.47	0.23	0.23	6	261	341	29	13
5	7.47	0.15	0.15	7	506	608	28	14

Based on simulations and requirements, five inductors were designed, with geometries defined in Table 5.1. Each design was simulated with no, one, and two magnetic layers and with 0.2 mm and 0.79 mm substrate thickness to determine the effect of NiZn ferrite composite on inductance density and magnetic losses in the inductor. The DC resistance of the inductor was calculated using (5.5), while the inductance and R_{AC} values were extracted from simulations at 10 MHz with 200 μm thick magnetic layers on the top and bottom, where N, d, w, and s are as described in Fig. 5.1 and ρ_{copper} is the resistivity of copper [91].

$$R_{DC} = \frac{\rho_{copper}(4Nd - 4N^2w - (2N-1)^2s)}{w(thickness_{copper})} \tag{5.5}$$

5.1.4 Package Embedded Inductor Fabrication

The fabrication process for the inductor is shown in Fig. 5.8. This fabrication process was mainly devised by Dr. Bellaredj, with assisted contribution from myself in stencil design and inductor fabrication. Starting with a basic two copper layer FR4 PWB, the top and bottom copper layers are etched, creating the inductor pattern and the ground plane void respectively, as shown in Fig. 5.8(a). The patterned planar inductors and voids are shown in Fig. 5.9. The copper trace width and separation were measured using an optical microscope. The copper trace thickness and void depth were obtained using the Veeco Dektak 150 surface profilometer. The copper trace thickness was around 42 μm and the void depth was 35 μm for the inductors.

The top magnetic layer was deposited with the NiZn ferrite composite using stencil

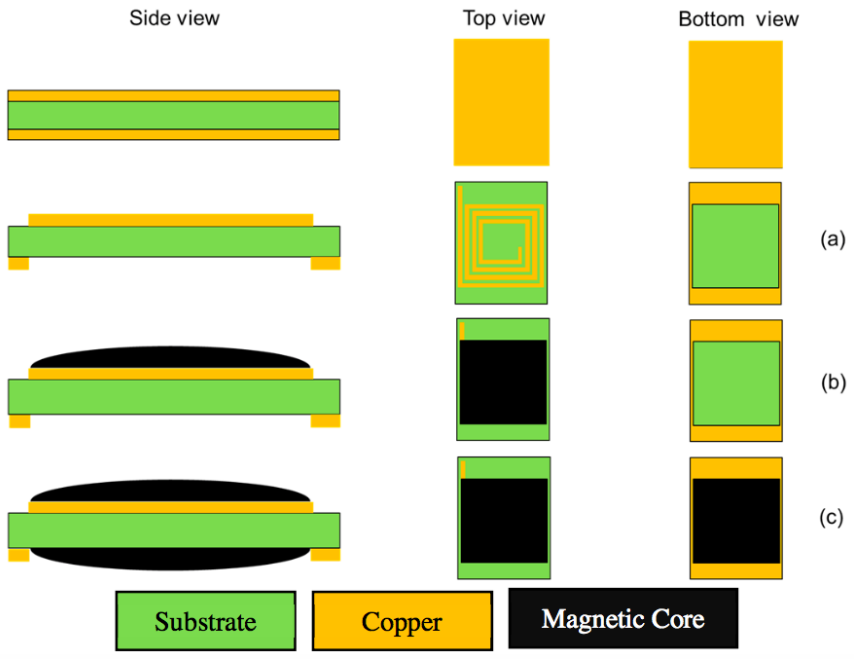

Figure 5.8: Fabrication process flow for the planar inductors: (a) PWB etching to define the inductor copper windings and back side trenches (b) Screen printing of NiZn ferrite core on the top side of the PWB (c) Screen printing of NiZn ferrite core on the back side of the PWB

printing (MPM SPM 7279 Semiautomatic Stencil Printer), as shown in Fig. 5.8(b). The board was designed symmetrically so the same stencil could be used for the top and bottom layers deposition. Alignment marks on the stencil and the board ensured that the magnetic material were placed precisely on the inductor.

The boards were cured for one hour at 180°C to form the top magnetic composite core. To prevent the creation of air bubbles, the curing temperature increased gradually up to the final temperature. For depositing the second magnetic layer, the same stencil screen and magnetic paste are used. The bottom magnetic layer was stencil printed and the boards were cured again for one hour at 180°C to form the bottom magnetic composite layer, as shown in Fig. 5.8(c).

A fabricated inductor and the thickness of the magnetic layers on the inductor measured using the profilometer is shown in Fig. 5.10. In addition to providing a low cost method for applying magnetic layers to both sides of the PWB, a key advantage of this process is

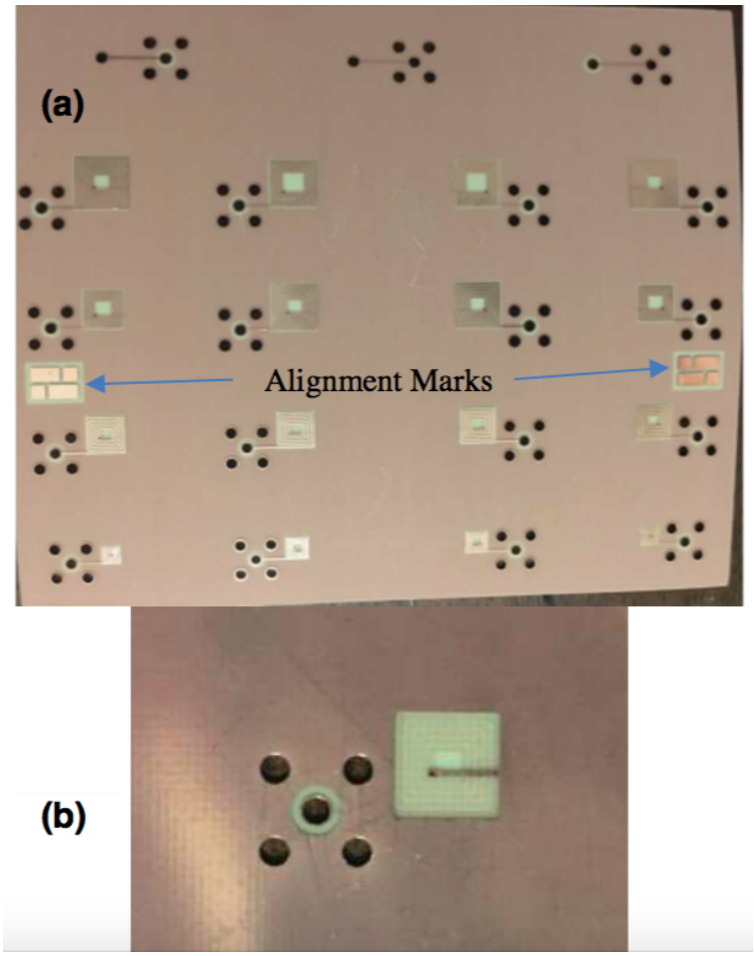

Figure 5.9: Inductor structure patterning on both sides of the flexible 0.2 mm PWB (a) full view of a 12 cm by 10 cm fabricated board top layer (b) Bottom layer with the cutout/void shown

ease of integration in a SiP solution for IoT applications. Since the spiral inductors can be co-designed and fabricated with the rest of the RFNFC system, an optimum design with high integrated reliability is possible, thereby enabling a higher power efficiency.

5.1.5 Inductor Measurement and Discussion

The fabricated inductors were measured between 10 MHz and 50 MHz using an Agilent H8363B Vector Network Analyzer, calibrated using SOLT standards. One port S-Parameters were measured and subsequently converted to Z-Parameters. The inductance and Q were extracted using (10) and (11) for a frequency range between 10 MHz and 50

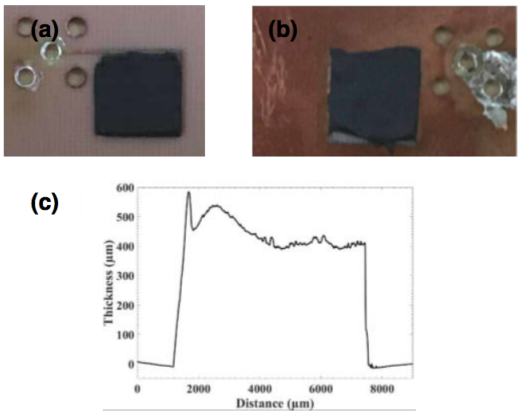

Figure 5.10: The fabricated inductors (a) top layer (b) bottom layer and (c) magnetic layer thickness profile

MHz, where Z_{11} is the Z-Parameter converted from the measured S-Parameter. The inductance of the feedline/SMA connector was also measured and de-embedded, which had an inductance contribution of 6-8 nH for the various line widths used in the designs.

$$L = \frac{Im(Z_{11})}{\omega} \tag{5.6}$$

$$Q = \frac{Im(Z_{11})}{Re(Z_{11})} \tag{5.7}$$

Fig. 5.11 shows the measurement results for inductor design 4, showing the comparison of inductance and quality factor between the different cases. For this comparison, all designs had the same spiral geometry and a void in the ground plane, where the rigid substrate has thickness 0.79 mm and the flexible substrate has thickness 0.20 mm. At 15 MHz, inductor 4 has an inductance increase from 194 nH to 268 nH from the application of a single magnetic layer on the top layer of the inductor - an increase of over 30%. At lower frequencies, the Q factor is higher for the single magnetic layer case compared to the air core case since the increase in inductance is much larger than the increase in resistance. At higher frequencies, however, the Q factor reduces because the loss tangent of the magnetic material increases with frequency while the permeability does not, as shown in Fig. 5.4.

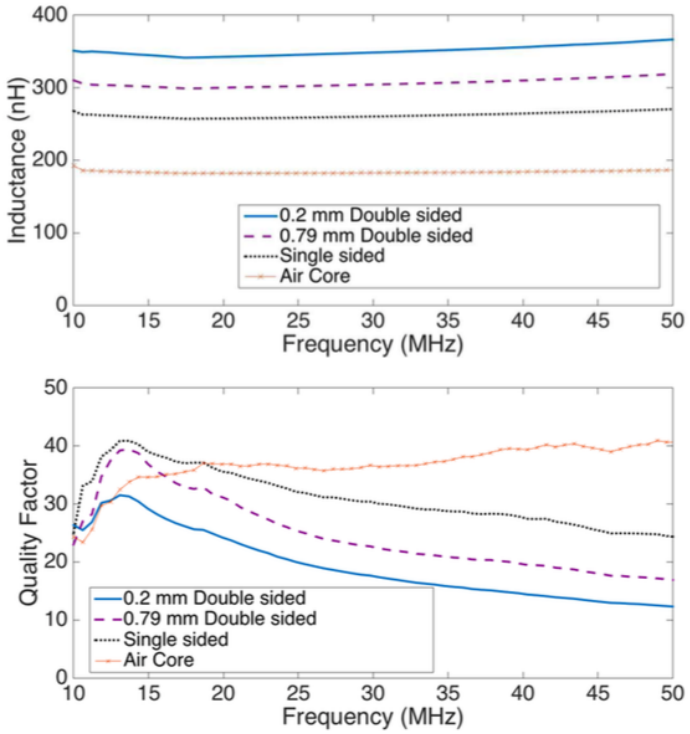

Figure 5.11: (a) Inductance comparison and (b) Q comparison for inductor 4

The peak Q occurs between 10 and 20 MHz.

For the rigid substrate with double magnetic layer, the inductance increases to 310 nH, which corresponds to a 60% inductance increase over the air core inductor. The Q factor has similar values as the single magnetic layer near the frequency of operation, and therefore AC losses are not significantly increased.

For the double sided magnetic layer on flexible substrate, the inductance measured was 351 nH for inductor 4. This inductance increase as compared to the rigid substrate can be attributed to the increased magnetic field density in the inductor due to the reduced substrate thickness. However, the higher magnetic field density results in increased magnetic losses which affects the quality factor of the inductors. As shown in Fig. 5.11, the quality factors are still above 25 and remain large enough to maintain the R_{AC} losses for the power inductor below the required value.

Based on the measurement results, the inductors were re-modeled using HFSS by ac-

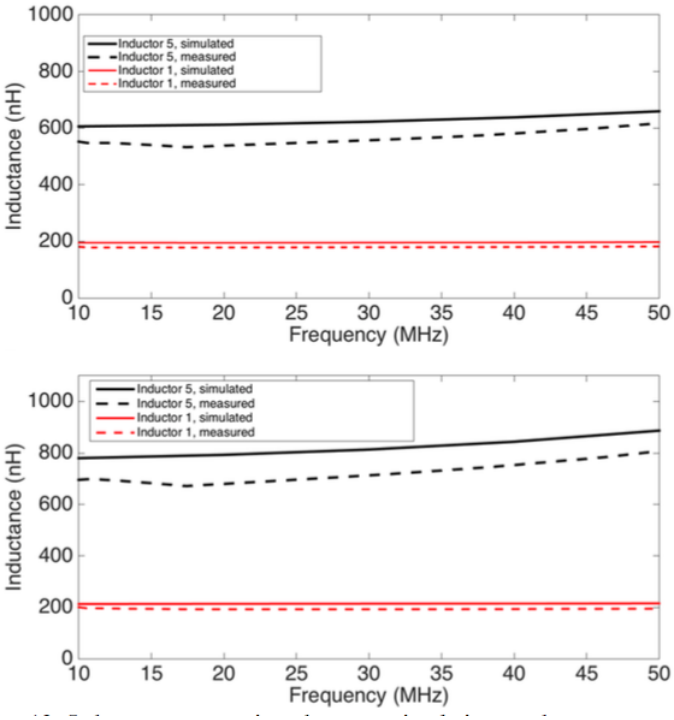

Figure 5.12: Inductance comparison between simulations and measurements (a) 0.79 mm thick PWB (b) 0.2 mm thick PWB

counting for the measured thickness for the magnetic material to obtain good model-to-hardware correlation. Here only inductors 1 and 5 are examined, as examples. Using a one port simulation the self-impedance was calculated from the S-parameter (S_{11}). The self-impedance provides the frequency response of the inductance loop, from which the inductance and Q factor can be extracted using (10) and (11).

The inductance comparison between simulation and measurement results for the 0.2 and 0.79 mm thickness boards are shown in Fig. 5.12. The simulations slightly overestimate the inductance, which can be attributed to the fabricated magnetic layers having minor air pockets after curing, which were not included in the simulations. As mentioned earlier, the magnetic thickness was modeled as an average thickness in HFSS based on measurements, accounting for some variation in the inductance and quality factor.

Table 5.2: Measured Inductor Comparison

$Inductor$ #	Air Core Inductance	Air Core Peak Q	Single Magnetic Layer Inductance	Single Magnetic Layer Peak Q	0.79 mm Two Magnetic Layers Inductance	0.79 mm Two Magentic Layers Peak Q	0.2 mm Two Magnetic Layers Inductance	0.2 mm Two Magnetic Layers Peak Q	Peak Q Freq (MHz)	Area (mm^2)
1	109 nH	26	145 nH	36	182 nH	40	201 nH	26	14	35.33
2	201 nH	27	258 nH	33	293 nH	34	357 nH	30	12	35.33
3	271 nH	32	374 nH	38	439 nH	37	501 nH	34	15	70.26
4	194 nH	32	268 nH	41	310 nH	39	351 nH	32	13	55.77
5	334 nH	32	468 nH	36	552 nH	38	696 nH	31	14	55.77

5.1.6 Inductor Comparison

All five inductor geometries were measured with no magnetic layers, with only a top magnetic layer, and with magnetic layers on the top and bottom. The measurement results for all seven inductor designs show similar trends as the data shown for inductor 4, and these results are listed in Table 5.2. For all seven designs, the inductance showed significant increase from the application of NiZn ferrite magnetic layer(s). As expected, the 0.2 mm substrate with double magnetic layers had the largest overall inductance, significantly increasing the inductance over the air core inductor without increasing the DC resistance.

Unlike SMT inductors which are discrete, these power inductors can be custom designed for obtaining the optimum efficiency for a variety of IoT applications. Figure 5.13 shows the modeled efficiency of the 10MHz buck converter using the measured data for the double sided, 0.20mm substrate thickness inductor for all the designs discussed. The modeled efficiency is between 85% - 94%. The breakdown of losses for the buck converter for inductor 5, double sided 0.2 mm thickness at 10 MHz is shown in Fig. 5.14. Inductor AC and DC loss contribute 45% and 10% of the total power losses, respectively. This compares to 45% of the power losses arising from the FET transistor losses (conduction and switching). From this analysis, it can be concluded that the integrated inductor with screen printed NiZn magnetic composite is suitable for fully integrated RFNFC systems with higher frequency (10 MHz in this case) buck regulator, ideal for use with future technologies as device frequency scales upwards and fabrication process nodes shrink.

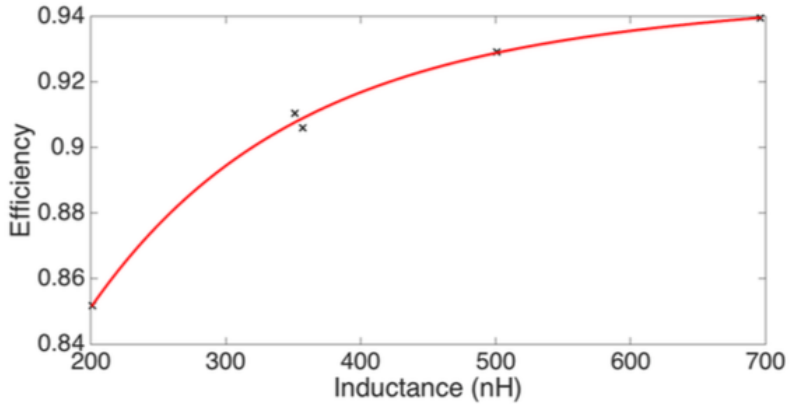

Figure 5.13: Modeled efficiency with measured inductor data for each 0.20mm substrate thickness, double magnetic layer design.

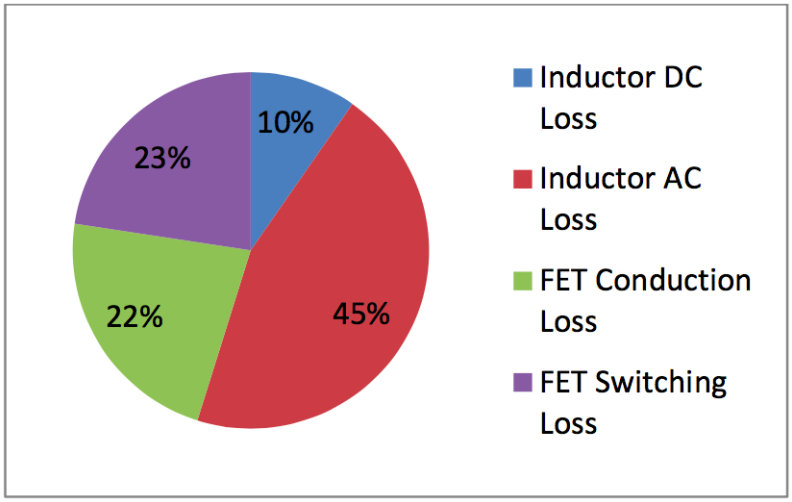

Figure 5.14: Breakdown of losses in converter/power inductor

5.2 Integrated Inductor for TPS62615 at Light Load Discontinuous Conduction Mode

5.2.1 Inductor Loss Analysis for Discontinuous Conduction Mode

Instead of demonstrating the WPT systems with SMT inductor alone, an integrated inductor is also designed for a demonstrated RFNFC system. For a comparison between the integrated inductor and a SMT inductor, a Texas Instruments TPS62615 buck converter in ball grid array (BGA) package is selected. The reason for this is the TPS62615 buck converter has an increased switching frequency - 6 MHz - which will highlight the influence of harmonics and the advantage of the designed integrated inductor much better than the 2.25 MHz LTC3564. In the previous chapter is was shown the magnetic composite is most effective at 10-20 MHz, such that the increased switching frequency is necessary to validate efficiency improvement compared to SMT inductor.

The calculation of inductor ripple current in DCM buck converter is shown in (5.8) - (5.9), where ΔI is the inductor ripple current, f_{sw} is the PDU switching frequency, L is the inductance of the integrated inductor, D is the duty cycle of the buck converter in DCM and where K is defined in (5.10) [92]. The calculation of the ripple current is the same as continuous conduction mode (CCM), but with an altered calculation of the duty cycle for DCM operation. All measured systems in this dissertation operate with the buck regulator in DCM, as the load power is small.

$$\Delta I = \frac{(V_{in,PDU} - V_{out})D}{f_{sw}L} \tag{5.8}$$

$$D = \sqrt{\frac{4K}{(2(\frac{V_{in,PDU}}{V_{out}}) - 1)^2 - 1}} \tag{5.9}$$

$$K = \frac{2Lf_{sw}}{R_{Load}} \tag{5.10}$$

5.2.2 Harmonics of DCM Inductor Current

The TPS62615 has two modes of operation: pulse width modulation (PWM) and pulse frequency modulation (PFM). PFM mode has increased efficiency at the load range considered in this dissertation, though PWM can be used for noise/output ripple sensitive applications [93]. Both will be examined in measurement between the integrated and SMT inductor. PWM operation has an added benefit - the ideal inductor current waveform is known for a given switching frequency, inductance, input voltage, and load, using (5.8) and (5.9). Figure 5.15(a) shows the ideal PWM inductor current calculated for the 6 MHz TPS62615 for 1.2V output, 2.5V input, 1.5μH inductance, and varying load power. Figure 5.15(b) shows the difference in frequency content of the inductor current for these different current waveforms. In DCM, as the load power decreases, there is increased influence of harmonics of the switching frequency. At 1 mW, the harmonic content of the inductor current is almost as significant as the switching frequency. PFM mode is similar to 'burst' mode for the LTC3564. The inductor current in this mode also has increased influence of harmonics as the load power decreases, though this effect is less severe than in the PWM case. Thus, in order to design integrated inductors for light load applications, the inductor characteristics at harmonics of the switching frequency must be accounted for in addition to the switching frequency.

5.2.3 DCM Inductor Loss Analysis

Incorporating the frequency content of the inductor current is particularly important for light load applications. A shortcoming in the analysis of other works for light load applications is the use of the Q-factor of the integrated inductor at the switching frequency without regard to higher order harmonic frequencies. To improve the evaluation of inductor power loss for buck converter in DCM mode, a calculation that includes the frequency spectrum of the inductor current is needed.

For evaluating inductor loss, the conventional formulation is given in (5.11), where R_{ind}

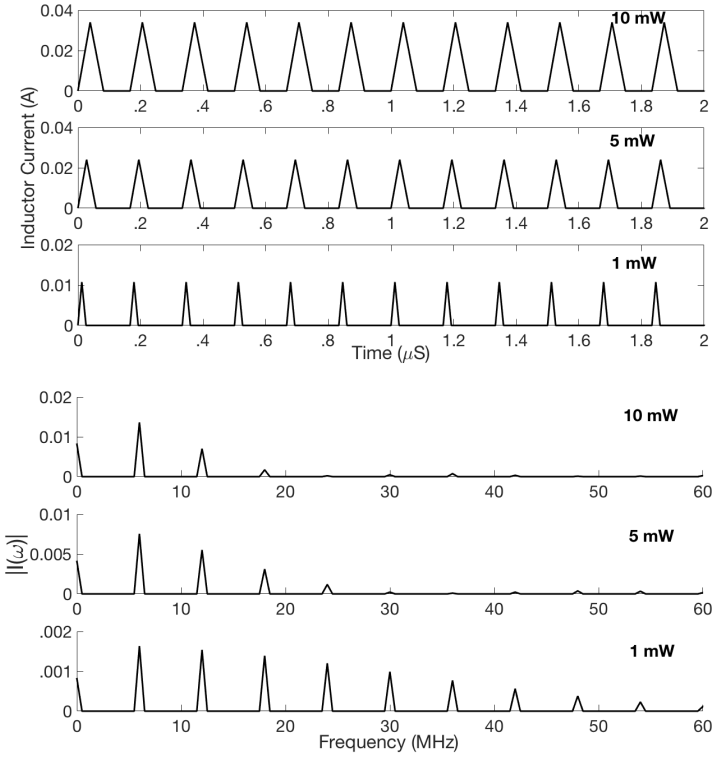

Figure 5.15: (a) PWM inductor current for different load power and (b) spectral content of these currents

is the inductor resistance and I_{out} is the PDU load current. This calculation is typically separated into the inductor DC resistance with I_{out} and the inductor AC resistance at the switching frequency with ΔI [89]. A calculation of just the inductor AC power loss from the ripple current is shown in (5.12).

$$P_{loss,L} = R_{ind} * (I_{out}^2 + (\frac{\Delta I}{2\sqrt{(3)}})^2) \tag{5.11}$$

$$P_{loss,L_{AC}} = R_{ind}(f_{sw}) * ((\frac{\Delta I}{2\sqrt{(3)}})^2) \tag{5.12}$$

The change in the frequency content of the inductor current with different inductance and load would not be an issue if the inductor resistance was constant with frequency, which is certainly not the case. Equation (5.11) assumes a perfect triangular wave form and approximates the inductor AC loss accordingly. An improved inductor loss equation for DCM is shown in (5.13). There are two differences between this revised calculation and the calculation in (5.11). First, the DC component is neglected. This is an approximation only valid for light load applications. Consider the maximum output current for the 1.2V output. At 10 mW output, this gives I_{out} = 8.3 mA. Even with a DC resistance of 1Ω, the inductor DC loss will be 69 μW - less than 1% efficiency decrease in the worst case scenario. In a WPT system supplied by a controlled power source, the input voltage to the PDU is not fixed as discussed in Chapter 2. As the load power changes, the PDU input voltage will vary such that the power at the output of the rectifier and the power needed at the input of the PDU are equal. As the efficiency of both the RF near field coupling coil+rectifier system and the PDU are affected by the input voltage to the PDU, the PDU input voltage that matches these two will vary with the load power. As such, the ripple current and corresponding inductor AC loss will increase as the PDU input voltage increases, such that the most important design consideration is designing for low inductor

AC loss across a wide range of $V_{in,PDU}$.

$$P_{loss,DCM} = R_{weighted} * (\frac{\Delta I}{2\sqrt{(3)}})^2 \tag{5.13}$$

The second difference is a weighted value of the resistance is used instead of the inductor resistance at the switching frequency. For a given DCM inductor current waveform, the frequency content is extracted from a fast Fourier transform as shown in (5.14), where $I(t)$ is the inductor current waveform. Then, $R_{weighted}$ is found from (5.15), where $R(\omega)$ is the frequency dependent resistance of the inductor over the frequency range ω_1:ω_2. The resistance is weighted with respect to the square of the spectral content of the inductor current, as this correlates better with power loss (i^2R). This is an improved resistance for loss calculation compared to the inductor AC resistance at the switching frequency.

$$I(\omega) = fft(I(t)) \tag{5.14}$$

$$R_{weighted} = \frac{\sum_{\omega=\omega_1}^{\omega_2} R(\omega)|I(\omega)|^2}{\sum_{\omega=\omega_1}^{\omega_2} |I(\omega)|^2} \tag{5.15}$$

5.2.4 Integrated Inductor Design

The integrated inductors have the same geometry as demonstrated in the previous section, with the key difference that a spiral inductor is located on the top and bottom layer, connected through a via as shown in Fig. 5.16. This leads to a much larger inductance density for the inductor, therefore this section briefly shows the design and characteristics of the inductor with this slight design change. The spiral inductor geometry was designed for 0.30mm thick FR4 substrate using a Two-Stage Bayesian Optimization algorithm by Ph.D. student Hakki Torun to achieve high inductance and low area while permitting very high DC resistance (around 1Ω). 1Ω DC resistance is allowable because minimal power loss from the DC resistance in the inductor is expected at the highest output power loads for

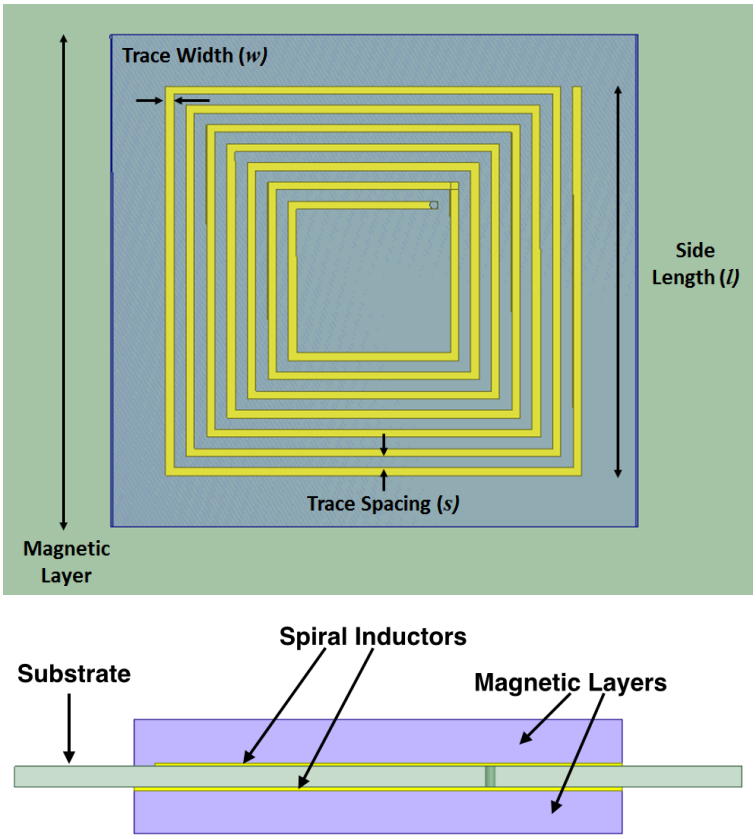

Figure 5.16: (a) Top view of inductor with geometry parameters and (b) side view of inductor structure

this system, while permitting much higher inductance density for smaller area inductor. The geometry of the spiral is given in Table 5.3.

A NiZn ferrite epoxy composite was screen printed on both layers of the spiral inductor, with material details available in [90]. The screen printed magnetic layer has area similar to the spiral, with 4.7x4.7mm area. The maximum thickness from a single screen printing application, 500μm, was selected as the core thickness for both the top and bottom layers. The reason for the selection of thicker magnetic layers is because at higher inductance, there

Table 5.3: Geometry Parameters of Both Integrated Inductors

Substrate Thickness	0.3 mm	0.79 mm
Side length (mm)	4.65	5.16
Trace width (mm)	0.1	0.1
Trace spacing (mm)	0.1	0.15
Number turns	7	7
Area (mm^2)	21.6	26.6

is less harmonic content in the DCM inductor current, shown in Fig. 5.17(a). The power loss for a 5 mW load for the designed integrated inductor is calculated from (5.13), with different value of $R_{weighted}$ extracted from the different inductor current waveforms. As the inductance increases, there is less power loss in harmonics of the switching frequency as shown in Fig. 5.17(b). For all three inductance cases, only a fraction of the power loss occurs at the switching frequency. In fact, the 1500 nH case has the largest power loss at the switching frequency. As the power loss contribution of higher order harmonics is considered, however, the 500 nH inductance case has a rapidly rising power loss while the 1500 nH case power loss levels off. However even this inductance consideration must be balanced, as the law of diminishing returns means there is a limit to how much increased inductance is beneficial. Eventually, adding extra inductance will have minimal effect on inductor current harmonics while increasing the area. For the demonstrated system, inductance beyond 1500 nH yields little benefit.

A second inductor was also designed for 0.79mm thick substrate using the same procedure as the 0.30mm thick substrate inductor. This inductor is less effective at similar area, as the inductance is less, and the design characteristics are shown in Table 5.3. This inductor is only used for full system measurements in Chapter 6 on designs with 0.79mm thickness substrate, and not used for any of the following comparisons/measurements in this chapter. The inductance is 928 nH and the Q is 7.8 at 2.25 MHz, for use only with the LTC3564.

5.2.5 Integrated Inductor and SMT Inductor Comparison

The integrated inductor is compared with a SMT inductor from Murata (Part LQM21PN1R5MC0) with 260 mΩ DC resistance. This is a multilayer inductor with ferrite core. This SMT inductor is selected because it has similar inductance to the embedded inductor, but more importantly, because it is an inductor recommended for use with the TPS62615 for good efficiency on the datasheet [93]. A comparison of the integrated inductor and the SMT

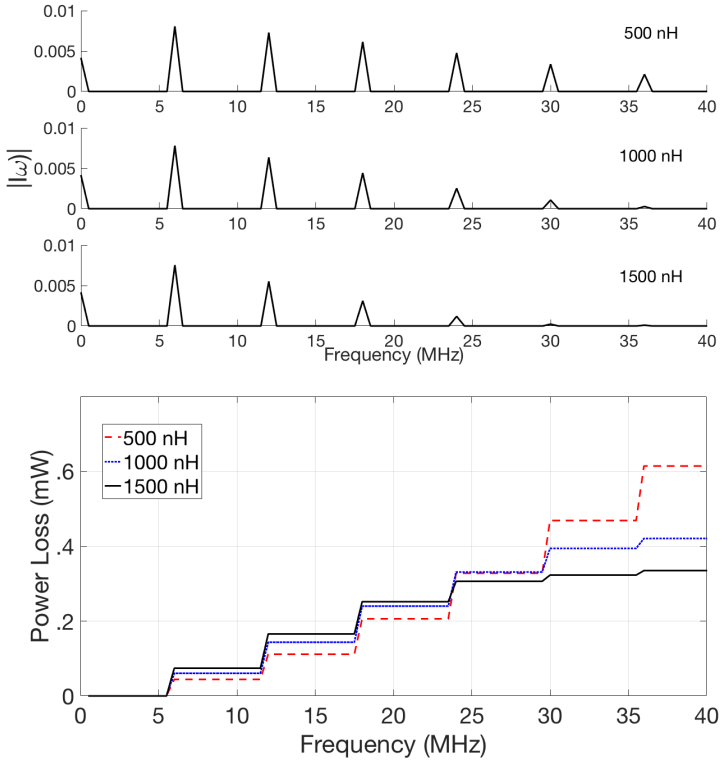

Figure 5.17: (a) Variation in inductor current spectral content with inductance value and (b) Cumulative power loss with frequency at 5 mW load with different inductance value

Table 5.4: Comparison of Embedded and SMT Inductor

	Embedded	SMT
L @ 6 MHz	1.36 μH	1.35 μH
Area (mm^2)	22	2.5
Height	0.5 mm (one layer)	0.5 mm
L Density (nH/mm^2)	63	540
R_{DC}	1Ω	260mΩ
R_{AC} @ 6 MHz	3.77Ω	4.3Ω
Self resonant freq	88 MHz	70 MHz
Q @ 6 MHz	13.6	11.9

inductor with manufacturer supplied data is shown in Table 5.4. The two inductors have similar inductance at 6 MHz, though the integrated inductor has slightly improved Q and the SMT inductor has smaller area. A comparison between the inductance and AC resistance of the two inductors is shown in Fig. 5.18.

When calculating the loss conventionally from (5.11), the power loss is very similar for the two inductors as shown in Fig. 5.19(a), for 2.5V input and 1.2V output. However, the two inductors differ greatly in their AC resistance at higher frequency, shown in Fig. 5.18. Data for the SMT inductor is only supplied up to 30 MHz, but at this frequency the SMT inductor has approximately 5x larger R_{AC} than the integrated inductor. The NiZn magnetic composite has a slowly increasing magnetic loss tangent in this frequency range, therefore the R_{AC} also increases at a much slower rate when compared to the SMT inductor. When accounting for harmonics of the switching frequency and calculating the inductor power loss with the developed analysis using (5.13), the power loss of the integrated inductor is much improved over the SMT inductor as shown in Fig. 5.19(a). While the resistance at 6 MHz is similar for the two inductors, $R_{weighted}$ is higher for the SMT inductor, shown in Fig. 5.19(b). By including the harmonic content of the inductor current, the inductor power loss evaluation changes considerably. When calculating the inductor loss with 3.5V input voltage compared to 2.5V, the power loss improvement from the integrated inductor from (5.13) becomes even greater as shown in Fig. 5.19(b). This is because the as the ripple

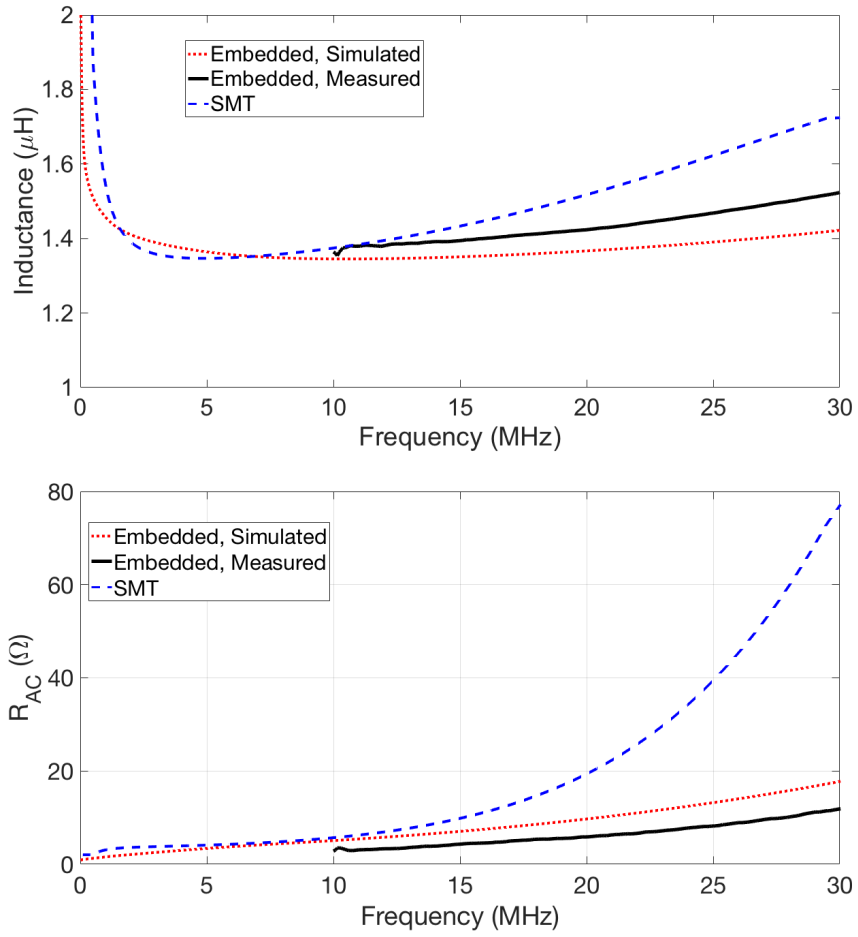

Figure 5.18: Comparison of integrated and SMT inductor (a) inductance and (b) R_{AC}

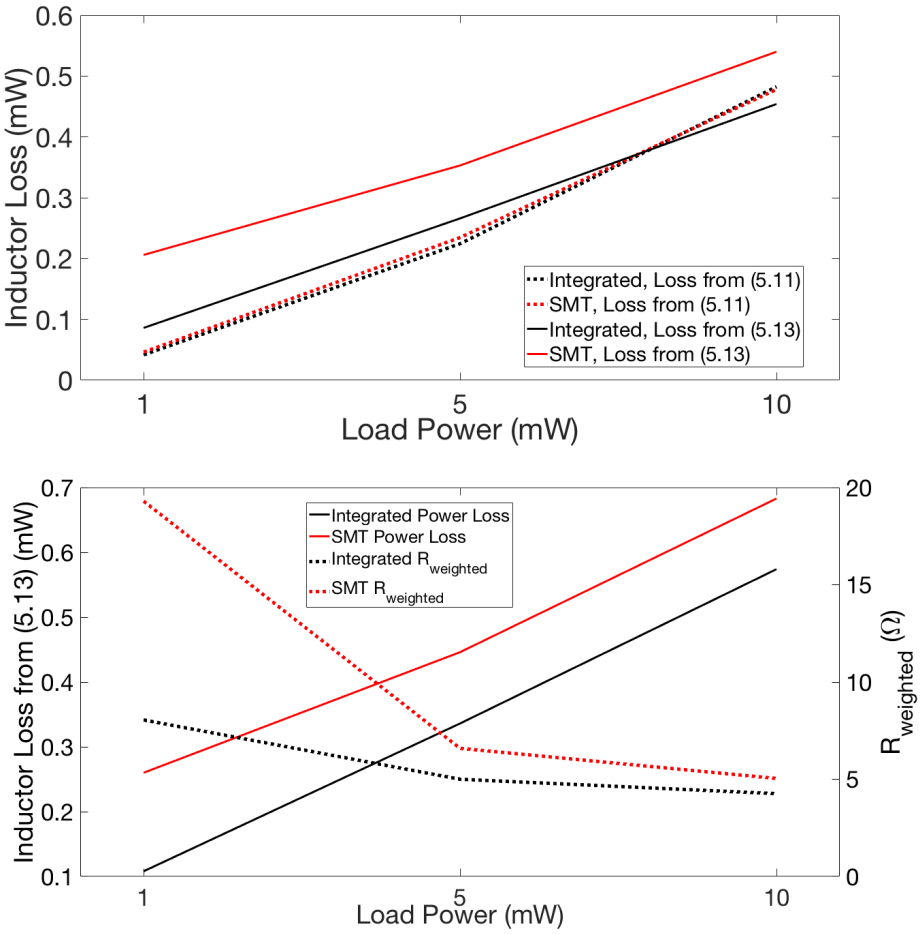

Figure 5.19: (a) Comparison of calculated inductor loss for SMT and integrated from (5.11) and (5.13) at 2.5V input and (b) comparison of calculated inductor loss from (5.13) and $R_{weighted}$ at 3.5V input

current increases, the difference in $R_{weighted}$ between the two inductors becomes even more significant.

5.2.6 Experimental Results

Receiver Fabrication

The complete WPT receiver was fabricated on 0.20mm thick FR4 substrate using standard PWB process. The NiZn ferrite epoxy composite was stencil and screen printed on the top and bottom layer on top of the copper windings defined on both sides of the substrate using the same stencil and cured at 180°C for 1h, with the fabricated inductor shown in

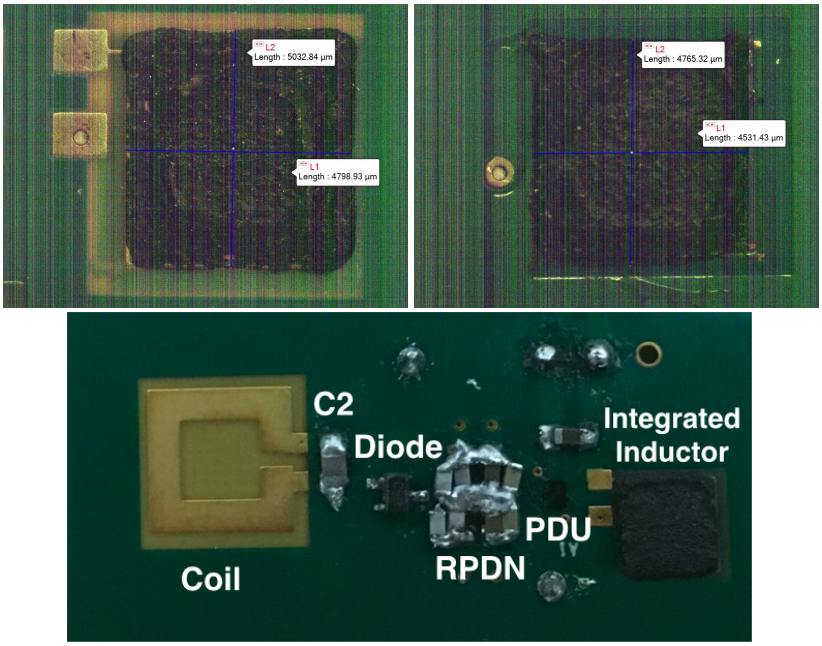

Figure 5.20: (a) Fabricated 0.2mm thick substrate integrated inductor top (left) and bottom (right) layer and (b) TPS62615 circuit with integrated inductor

Fig. 5.20(a) and the full receiver shown in Fig. 5.20(b). Following the screen printing, the BGA package TPS62615 and surface mount components were assembled with reflow soldering, and then the remaining through hole components were soldered to the design. This demonstrates the durability of the integrated inductor with various assembly processes.

Comparison with PDU Only

First, just the PDU efficiency with the embedded and SMT inductor was compared. The efficiency as a function of input voltage was measured for 3 different output power with variable resistor load: 1mW, 5 mW, and 10 mW. The DC power supply was an Agilent E3633A, and the PDU input current was measured with a HP 3478A multimeter to determine the input power for each measurement point. The efficiency was measured for the buck converter operating in PFM mode (Fig. 5.21(a)) and PWM mode (Fig. 5.21(b)). In all cases, the integrated inductor has improved efficiency over the SMT inductor. For PFM

operation, the efficiency difference between the two inductors increases as the PDU input voltage increases. This is because the DC power loss in the inductor stays constant (the load is unchanged), but the inductor AC loss increases with the increase in inductor ripple current. Because the integrated inductor has lower resistance at harmonics of the switching frequency, the efficiency of the integrated inductor decreases less with the increase in input voltage. At 10 mW load at 2.5V input, the difference between the integrated and SMT inductor is very small - the added inductor DC loss in PFM mode and the fact $R_{weighted}$ is more similar at 10 mW is the cause of this. However, at 1 mW load, the efficiency difference is largest, and exists even at 2.5V input. This is supported by the calculation of inductor loss from (5.13) as shown in Fig 5.19. At 1 mW, there is greatly increased inductor current harmonics, leading to the more significant improvement from the embedded inductor. For PWM operation, the efficiency difference changes less with PDU input voltage. In PWM mode, the DC current component is less, thus at all input voltages the inductor power loss is dominated by the AC component. The demonstrates a reliable, integrated integrated inductor with compact, high frequency buck converter with improved efficiency over a SMT inductor. The fully integrated WPT receiver system measurements will be shown in the following chapter.

5.3 Inductor Comparison with State of the Art

The fabricated integrated inductors also compare favorably with other implementations of PWB compatible planar inductors with simple magnetic layer application published in the open literature, as shown in Table 5.5. In this comparison, the integrated inductor designed for the TPS62615 in the previous section is shown. Compared to [96] and [66], the inductance density of the demonstrated integrated inductor is much larger. The Q of the demonstrated inductor is similar to [96], [66], and [65], though the Q in [67] is larger. However, the inductance density and thereby inductance is smaller in [67], and the other inductors for that matter, such that there will be a much larger influence of harmonics in the inductor cur-

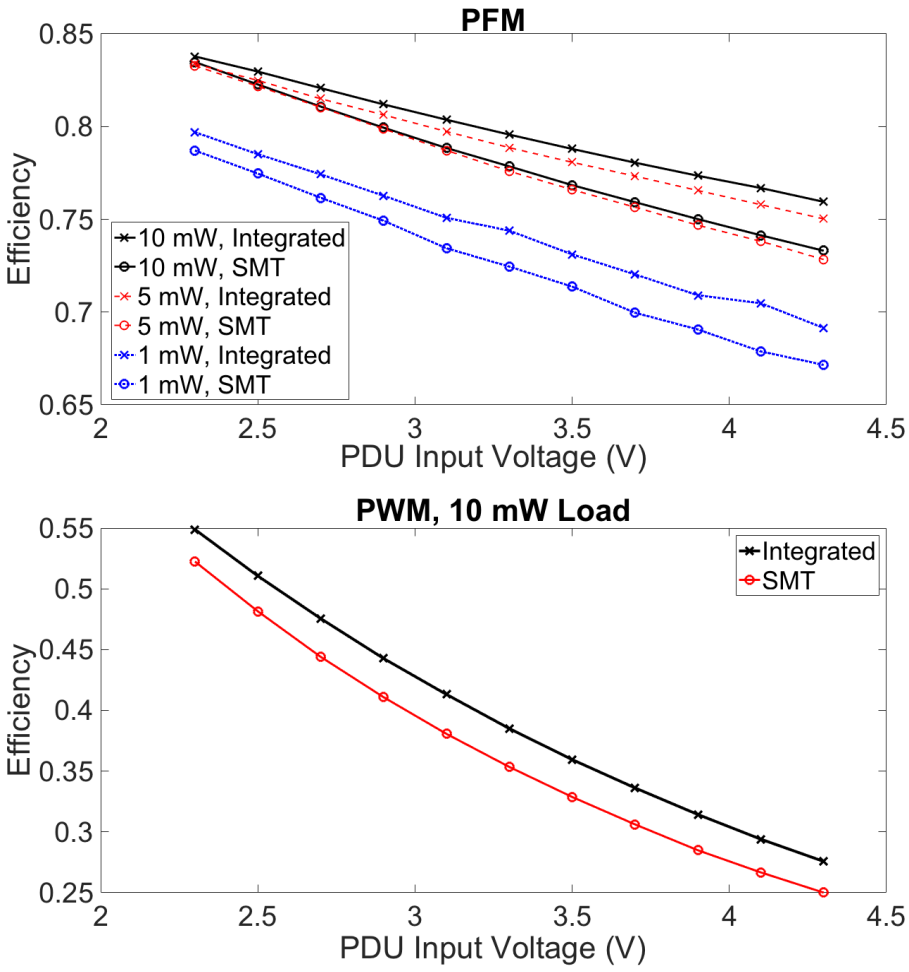

Figure 5.21: Measured PDU efficiency comparison between the two inductors in (a) PFM mode and (b) PWM mode

Table 5.5: Comparison with Other Package Inductors

	This Work	[96]	[67]	[66]	[65]
Inductor Fabrication	PWB Etch	Photo-lithography	PWB Etch	In-Silicon	In-Silicon
Magnetic Application	Screen Printing	Screen Printing	Screen Printing	Screen Printing	Manual Pressing
R_{DC}(mΩ)	1000	15	>2000	25	84
Inductance (nH)	1360	150	810	6.6	430
Peak Q	14	20	45	16	21
Inductance Density (nH/mm^2)	63	.7	33.1	6.6	47.8
Area (mm^2)	21.6	225	24.4	1	9
Frequency (MHz)	6	1	10	50	6

rent for application to DCM buck converter. In fact, the inductor in [66] was compared to essentially the same Texas Instrument buck converter (where the only difference is a 1.8V output compared to 1.2V), and the integrated inductor in that work demonstrated lower efficiency compared to the inductor that came with the evaluation board. The DC resistance in [67] is at least twice that of the demonstrated integrated inductor, which will start to introduce non-negligible power loss at the larger load power studied in this dissertation. The demonstrated integrated inductors show a simpler fabrication process needing less fabrication steps compared to the other screen printed magnetic core inductors and superior inductance density, while having electrical properties better suited for DCM buck regulator operation in integrated WPT receiver.

5.4 Summary

This chapter examined the fabrication, characterization, and design of embedded inductors for integrated WPT systems. A simply fabricated embedded inductor with screen printed NiZn ferrite magnetic core was characterized at a variety of substrate thickness and with different numbers of magnetic layers. An embedded inductor was then designed for discontinuous conduction mode buck converter by considering the AC resistance of the inductor at harmonics of the switching frequency. In measurement, a PDU demonstrated higher efficiency with the embedded inductor compared to a similar SMT inductor.

CHAPTER 6
COMPLETE SYSTEM MEASUREMENTS

Each of the previous chapters discuss various pieces and challenges for the design of integrated RFNFC systems. These included the system architecture development, the coil design, component selection, RF layout challenges, the reverse PDN, and embedded inductor integration. This chapter examines all of the work completed in prior chapters through measurements of complete systems. The experimental setup is explained, and the measurements of all complete systems are provided. This chapter demonstrates the dissertation objectives have been reached, and provides comparison to state of the art and discussion of the advantages and disadvantages of RF near field coupling.

6.1 Experimental Setup

The power supply for all measurements performed was a HP 8648D signal generator. The Textronic TDS 3012B oscilloscope was used to observe the waveforms at output of the DC-DC converter with variable resistor load, and the output resistance was measured and voltage verified with a multimeter. Plastic screws and clips were used to fix the transmission distance. This setup is shown in Fig. 6.1. The efficiencies presented in this dissertation are the total system efficiency, with the output power referenced to the input power at the transmit circuit from the signal generator. Specifically, this is not just the receiver efficiency, as is commonly reported, but the total system efficiency. This efficiency is given by (6.1), where V_{out} is the DC voltage at the output of the rectifier or buck converter (rectifier output for Chapter 3 measurements, PDU output for measurements in this chapter), R_{Load} is the load resistance, and P_{in} is the input power from the RF signal generator supplied to the transmitter circuit.

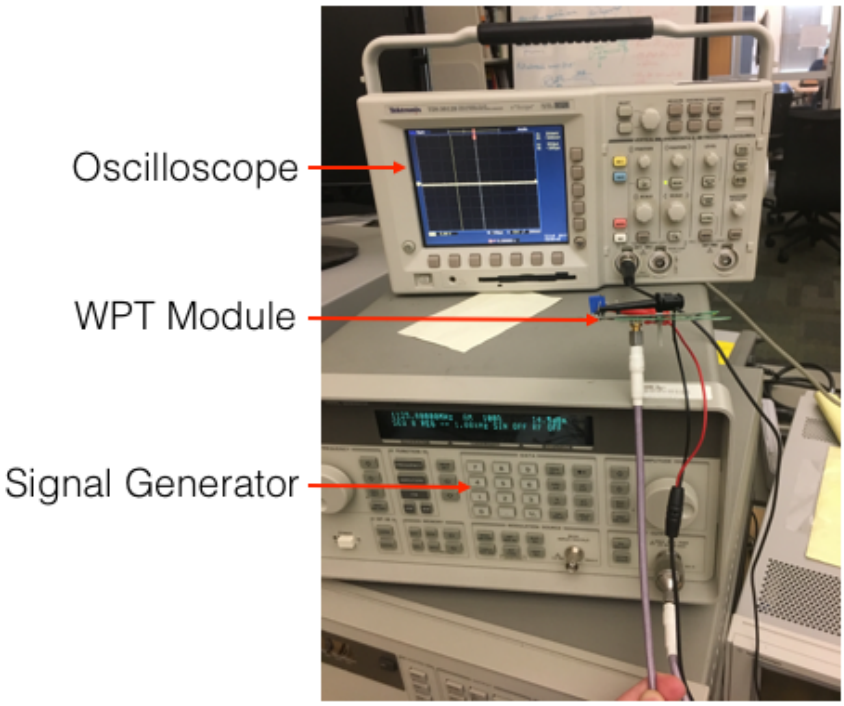

Figure 6.1: Experimental setup for all full system measurements

$$\eta_{WPT} = \frac{\frac{V_{out}^2}{R_{Load}}}{P_{in}} \tag{6.1}$$

For the full system, the measurement procedure differs from the PDU only measurement (with voltage source supply) and coil+rectifier only measurement (no PDU). Without the PDU, the input power can be freely increased and the rectifier output voltage will increase accordingly. As the purpose of the PDU is to supply output regulation, this will not occur for the full system. For full system measurements, the transmit circuit was supplied with 1 mW (0 dBm) and the power was slowly increased until there was sufficient power to supply the given load with constant DC output. This establishes the minimum input power necessary to achieve the desired voltage output and thus the peak efficiency for that operating point. Further increasing the input power would still result in the desired output voltage, but with lower efficiency as the output power is unchanged but the input power is increased.

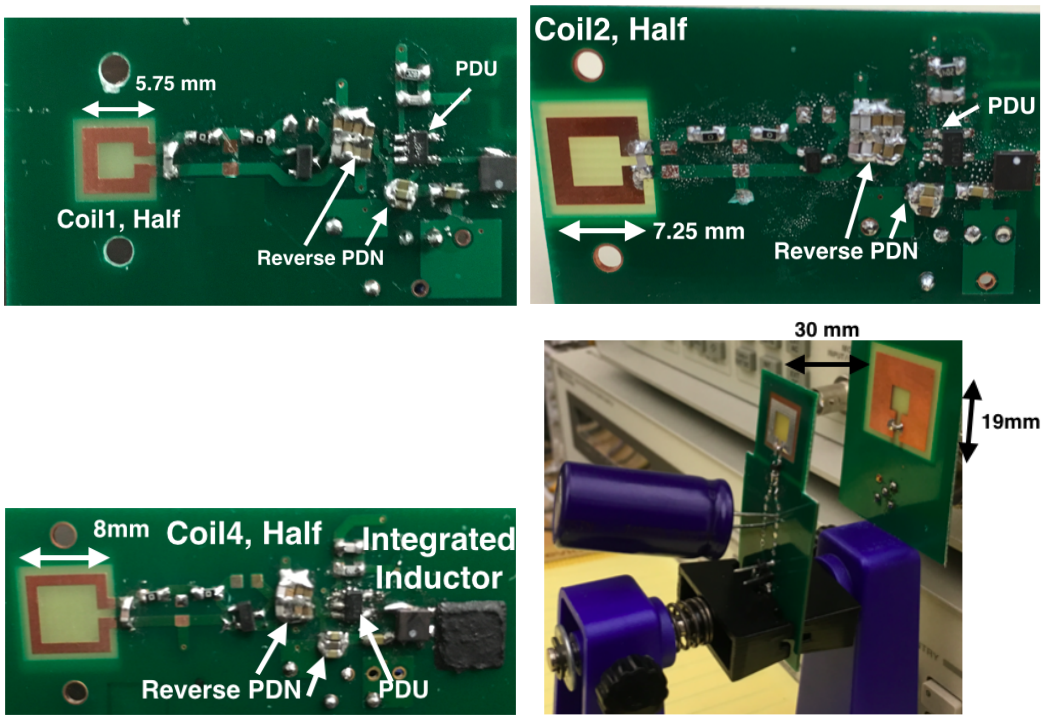

Figure 6.2: Fabricated full receivers for select 2 and (bottom right) 4 coil systems

6.2 Full System Measurements

6.2.1 Fabricated Full Systems

All designs with the LTC3564 were fabricated on 0.79mm thick FR4. The design with the TPS62615 was fabricated on 0.3mm thick substrate as discussed (and shown) in the previous chapter. Standard PCB manufacturing was used for the traces and metal patterns, on 1 or 2 oz copper. Only $bridge_{3,3}$ designs use 2 oz copper. The copper thickness only has a meaningful effect on the integrated inductor, which was not used for this system measurement. Some fabricated receivers are shown in Fig. 6.2.

6.2.2 Fully Integrated Systems Measurements

The differentiation between fully integrated and the other measurements in this chapter are the fully integrated systems in this section used the embedded inductor, and the other systems use a SMT inductor. The measurement of the $half_{4,4}$ system at 700 MHz, 1mm

transmission distance with the 0.79mm substrate thickness embedded inductor is shown in Fig. 6.3 at 3.3V and 1.2V output. At 3.3V output, the inductor is less active as the PDU switches seldomly, and the efficiency difference between SMT and integrated inductor in measurement was negligible. At 3.3V output, the buck converter is more efficient compared to 1.2V output, as the PDU losses are much lower. Also, at 1.2V output the PDU input voltage decreases at lower load power. When the load resistance is increased, the system wants to minimize the increase in $R_{in,PDU}$ to keep the coil efficiency from diminishing, thus it tries to minimize the voltage conversion ratio. At the higher load power, the load resistance is diminished such that $V_{in,PDU}$ has some flexibility to increase, for better rectifier and source efficiency, without compromising the coil efficiency. At the maximum power supplied by the RF source, the efficiency is 68.4% - the highest ever demonstrated for a RF near field coupling system. At 1.2V output the PDU more actively switches and the $1mu$H (similar inductance) Murata LQH3NPN1R0NJ0L SMT inductor has better efficiency at the 2.25 MHz switching frequency at higher output power. This SMT inductor has only 40 mΩ DC resistance, and in burst mode the LTC3564 has a larger inductor current DC component than typical for DCM. At the higher power output the significantly smaller DC resistance leads the SMT inductor to be more efficient. At lower output power (5 mW), the embedded inductor is more efficient. At this output power, the inductor current DC component is decreased and the AC loss dominates, such that the embedded inductor has slightly lower loss and is thus more efficient. Even at 2.25 MHz, below the optimal frequency for the embedded inductor, the lower resistance at harmonics of the switching frequency leads to better efficiency with the embedded inductor at lightest loads. The efficiency of the RFNFC system with embedded inductor and LTC3564 at 1.2V output peaks at 52.8%.

The $half_{2,2}$ system with the TPS62615 was measured with the integrated inductor on 0.3mm thick FR4 substrate. The system was supplied with a HP 8648D RF signal generator at 587 MHz and the coils were operated at 1 mm transmission distance. The measured efficiency for the full system is shown in Fig. 6.4. The peak efficiency is 42.7% at 1.2V

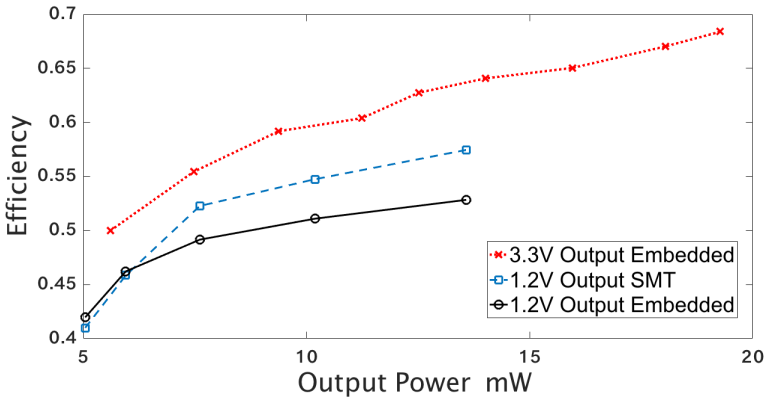

Figure 6.3: Measured efficiency of the complete $half_{4,4}$

output. This efficiency is lower than other systems at similar output voltage in this dissertation, but still offers an improved combination of coil area and efficiency in a WPT receiver compared to systems not in this dissertation. The efficiency decreases for a couple of reasons. First, other demonstrations use the LTC3564, which has better efficiency compared to the TPS62615. Also, this system is on 0.30mm thick substrate. In the curing process and reflow soldering process, the substrate warps. The system efficiency is highly dependent on the value of Q_2, and even minor warping can lead to minor decrease in this quality factor with noticeable efficiency decrease.

However, what differentiates this demonstration compared to the others is a high level of integration. In this design, a compact, 6 MHz chip is integrated with the embedded inductor - with improved efficiency as demonstrated in the previous chapter. The TPS62615 chip uses fewer components compared to the LTC3564 chip, increasing the reliability of the integrated solution. As such, the overall area of this receiver is smaller than the other demonstrations in this chapter. Excluding the reverse PDN and load, this implementation has only 3 external components and 1 chip added while demonstrating 42.7% efficiency and a reliable, compact, packaged, integrated solution.

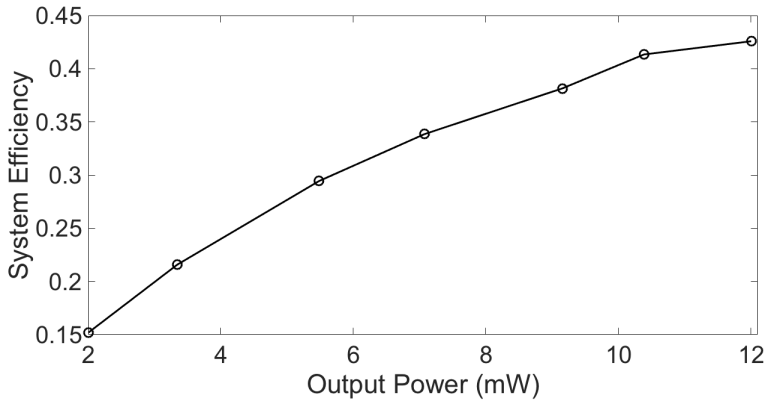

Figure 6.4: Measured system efficiency with integrated inductor and TPS62615

6.2.3 Other Systems with Half-Wave Rectifier

The measured efficiency of the system with $half_{4,1}$ at 689 MHz, 1mm transmission distance is shown in Fig. 6.5(a). The optimal frequency in measurement was 689 MHz as opposed to the designed 700 MHz, likely due to slight error in capacitor tolerances and transmission distance (honestly, it is very surprising the optimal source frequency for the $half_{4,4}$ system was exactly 700 MHz). While the efficiency is smaller than that of the $half_{4,4}$ system, the receiver coil area is almost half, demonstrating the tradeoff between efficiency and coil area in a RF near field coupling system. It also illustrates the importance of integrating a buck regulator. Figure 6.5(b) shows the input voltage to the PDU when the output voltage is 1.0V in the $half_{4,1}$ system at 15 mW load power. First, the input voltage ripple is at the metric set for the design of the reverse PDN (60 mV). Second, the PDU input/rectifier output voltage is about 3.7V. The rectifier is more efficient at this voltage and the $R_{in,PDU}$ is not a burden to coil efficiency at higher power with lower load resistance as discussed earlier. With a diode rectifier alone, the efficiency of the rectifier at 1.0V, 15 mW output would be much lower according to (2.9), compared to using a buck regulator with larger rectifier output voltage. As a final note, one can refer back to Fig. 3.14 to see that the measured efficiency follows the trends of the calculated coil+rectifier efficiency for $half_{4,4}$ - the best efficiency occurs at smallest load resistance (highest power), as opposed to the

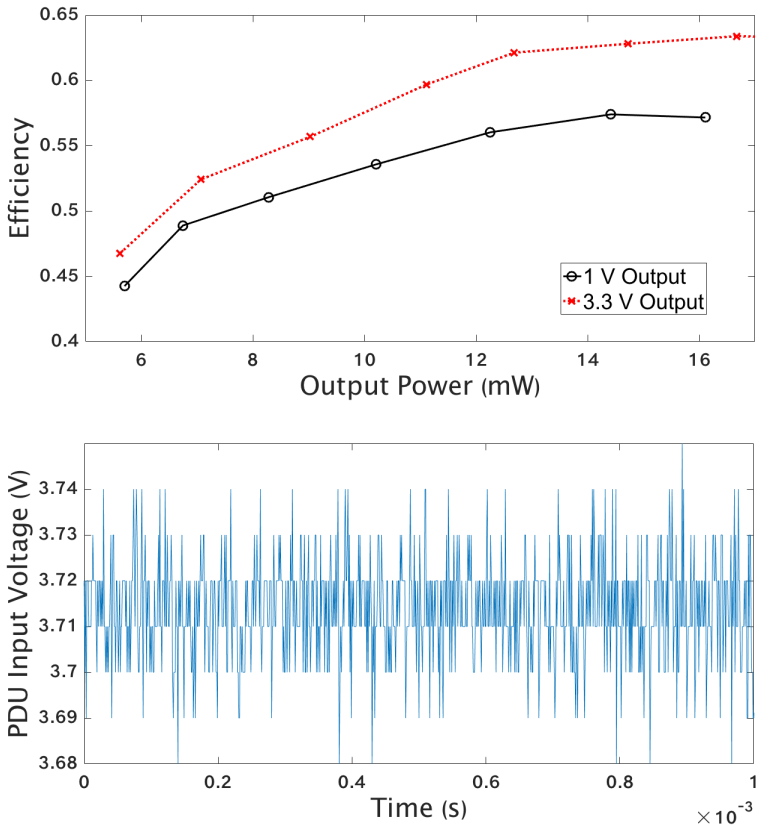

Figure 6.5: (a) Measured efficiency of the $half_{4,1}$ system and (b) PDU input voltage with 1V, 15 mW output

ADS simulated efficiency.

The measured efficiency of the $half_{2,1}$ system at 1mm transmission distance is shown in Fig. 6.6. The measurement uses a 786 MHz source frequency. The efficiency peaks at 67% at 3.3V output and 62% at 1.2V output. While the $half_{4,4}$ system has higher peak efficiency and utilizes integrated inductor, no other design demonstrated has over 60% measured efficiency at 1.2V output. In fact, nothing in all of academic literature comes close to this efficiency value at low voltage, and this is accomplished with a 33mm^2 area receiver coil. As expected, at low load power (high resistance) the efficiency is very low. With the small area receiver coil, a larger value of C_2 is necessary for resonance, degrading the coil efficiency at large load resistance. However, as the load resistance decreases, the efficiency rises. Because the coils are operated at 1mm, the k is large and high source

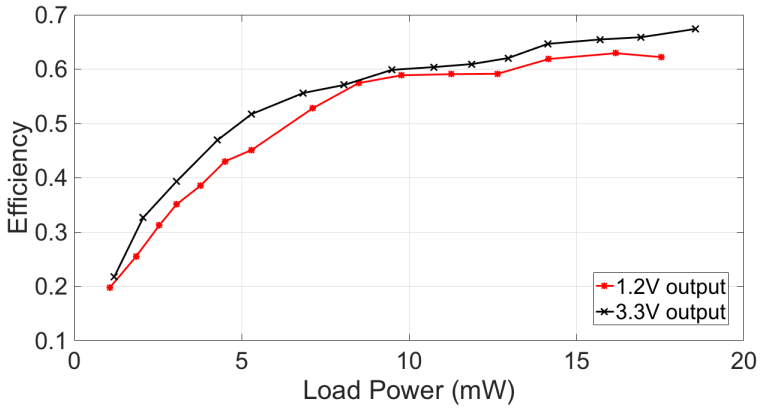

Figure 6.6: Measured efficiency of the $half_{2,1}$ system at 1.2V and 3.3V output at 1mm

efficiency is achieved even at lower load resistance as shown in the measurement in Chapter 3 without PDU. Interestingly, the optimal source frequency occurs around 50 MHz lower than the PDU absent measurement, as the additional microstrip line in the full system design downshifts the frequency.

The measured efficiency of the $half_{2,2}$ system at 2.5mm transmission distance with 800 MHz source frequency is shown in Fig. 6.7. A peak efficiency of 51% is achieved at this distance with 3.3V output. Unlike the other demonstrated designs at 1mm distance, where the efficiency peaks at either the maximum input power available from the source or close to it, the efficiency here peaks around 7 mW and then slightly decreases. As increasing the load power will decrease the load resistance for constant output voltage, the source efficiency degrades as this occurs. Thus the optimal load occurs lower power, higher resistance as also seen in the rectifier measurement at this transmission distance in Chapter 3. While this peak efficiency is lower than other demonstrated designs in this dissertation, this is also achieved at over 2x the transmission distance. This demonstrates how the developed design methodology can be used to sacrifice some efficiency to greatly increase the transmission distance. Even at 1.2V output, the 44% peak efficiency offers a never before seen combination of low output voltage, transmission distance, efficiency, and coil area.

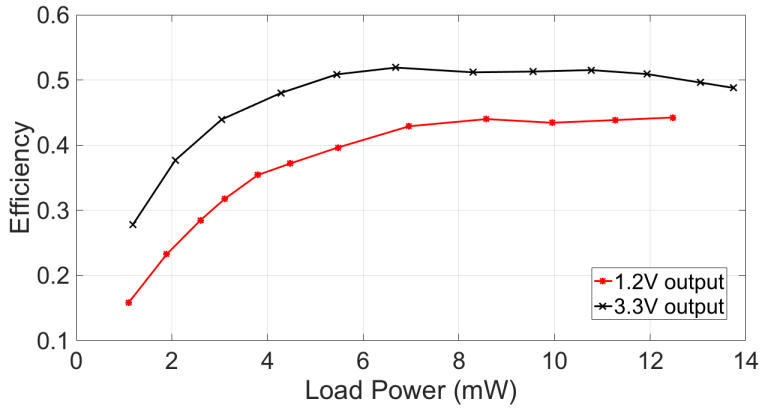

Figure 6.7: Measured efficiency of the $half_{2,2}$ system at 1.2V and 3.3V output at 2.5mm

6.2.4 Other Systems with Bridge Rectifier

The measured results for systems with bridge rectifiers are shown in Fig. 6.8 for $bridge_{2,2}$ (780 MHz) and Fig. 6.9 for $bridge_{3,3}$ (1008 MHz), both at 1mm transmission distance. The efficiency is lower when compared to the half-wave rectifier, as expected, but still higher than any other RF near field coupling system not in this dissertation. The measured results of these systems are also used for a direct comparison to a machine learning based design in the immediately following section. The measured results for $bridge_{3,3}$ demonstrate the effect of the loading resistance on the coil and source efficiency. The 3.6V output has lower efficiency than the 2.5V and 3V outputs at 5mW and 10mW. This seems counterintuitive as the output voltage is higher, and the corresponding rectifier output voltage is higher for improved rectifier efficiency. However, for equal load power across different output voltages, increased resistance is needed for increased output voltage. At the input voltage minimum for the LTC3564 (2.5V) and above, $R_{in,PDU}$ is transformed up by a similar proportion (PDU efficiency is very similar for all these areas). Thus, the $R_{in,PDU}$ is much higher for the 5 mW case at 3.6V (2600Ω) compared to 2.5V (1300Ω) and 3.0V (1800Ω). This leads to a large decrease in the coil efficiency, outpacing the gain in the rectifier efficiency. As the load power increases, $R_{in,PDU}$ decreases as R_{Load} decreases. At the maximum input power from the used supply, the 3.0V and 3.6V output efficiency are essentially equal. If larger

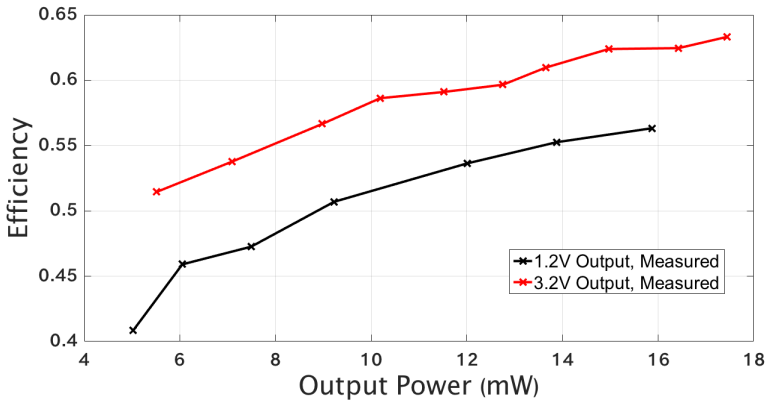

Figure 6.8: Measured results for $bridge_{2,2}$

power source were used, the efficiency of the 3.6V output would be higher than the lower output voltages via improved rectifier efficiency. This demonstrates the importance of designing for the system, factoring how the output power and voltage, for instance, affects the efficiency of all subsystems.

The $bridge_{2,2}$ system demonstrates higher efficiency than the $bridge_{3,3}$ system, despite similar coil characteristics, for a couple of reasons. First, the $bridge_{3,3}$ system was an earlier design iteration with well characterized efficiency as a function of PDU output voltage - valuable data for validating several efficiency trends as discussed in the preceding paragraph. However, this design has larger ohmic losses, especially with the PDU and reverse PDN through much longer traces. While the other measured complete systems use an upgraded PDU layout, the 'original' design in $bridge_{3,3}$ had 5-10% efficiency decrease on just the PDU subsystem in a separate measurement - undoubtedly the contribution of ohmic losses from longer traces on the input and output voltage lines because the input and output voltage capacitors were located much farther from the PDU. Second, the system operates at higher frequency - 1008 MHz - such that there is an increased contribution of diode switching loss and slight decrease in coil efficiency at this increased frequency.

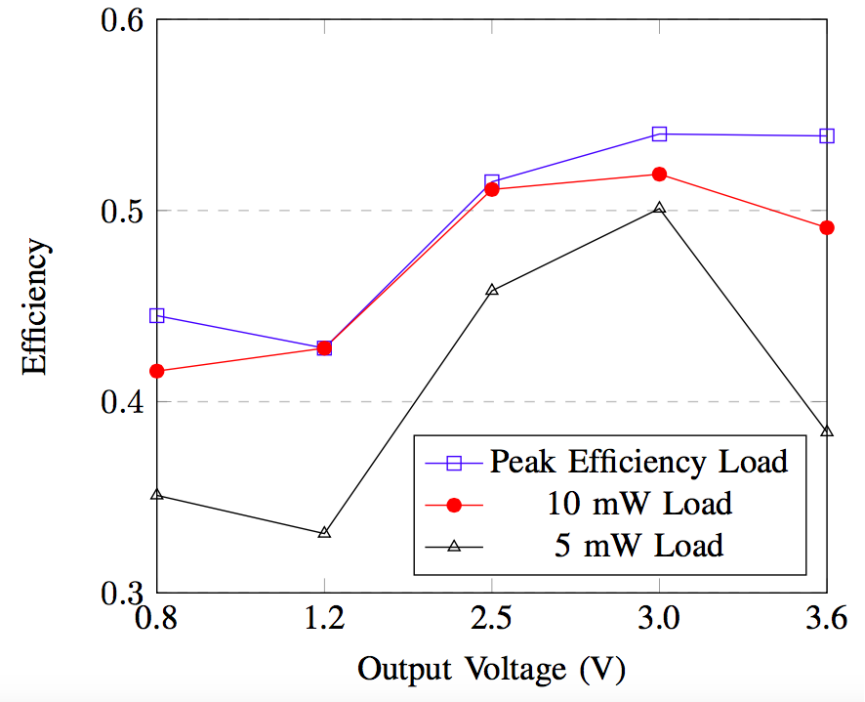

Figure 6.9: Measured results for $bridge_{3,3}$

Application of Machine Learning

Ph.D. student Hakki Torun applied his Two-Stage Bayesian Optimization (TSBO) to the full RFNFC system with a bridge rectifier at 1mm transmission distance, with the results shown in this dissertation to provide details on an avenue for continuing to decrease coil area/increase system efficiency. Full details of this process and results are provided in [94], with a summary provided here. This algorithm and design process used a stage by stage approach, with the algorithm process flow shown in Fig. 6.10.

This design process used the maximum PTE as the metric for the coils and optimized ADS simulations to determine the optimal coils for the design. One of the main benefits of utilizing a machine learning (ML) based design approach is that it enables many more geometric parameters to be explored. Specifically, the 'hand tuned' designs in this dissertation mainly focused on square coils with varying side length and line width. However, the ML based approach is able to consider many more geometric parameters, such as rectangular

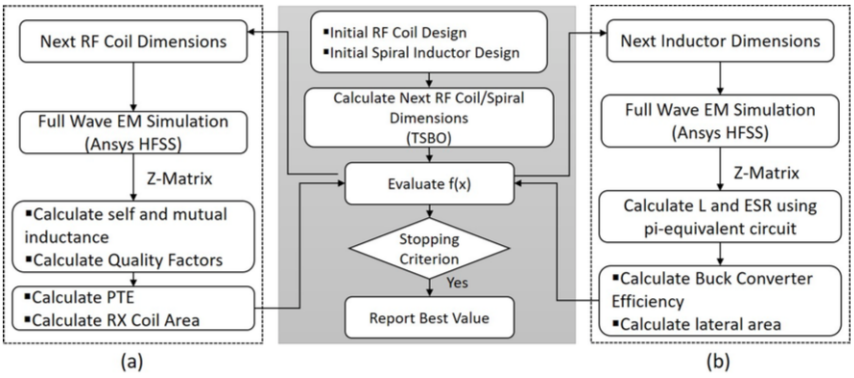

Figure 6.10: Algorithm flow process for (a) WPT coils plus rectifier front end and (b) PDU with embedded inductor

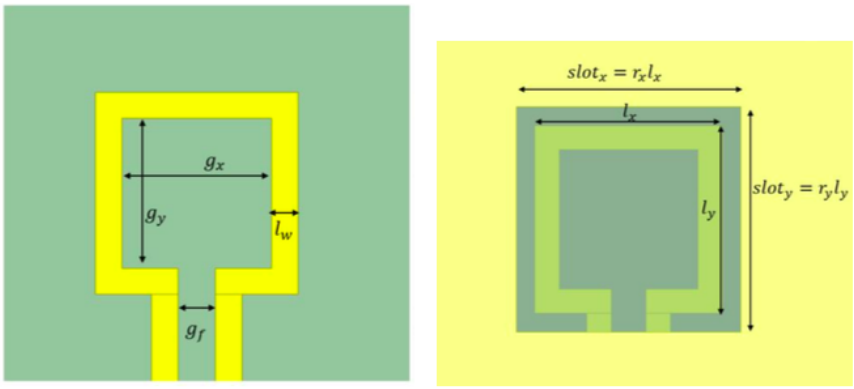

Figure 6.11: ML coil design geometry parameters for (left) top layer and (right) ground layer

coils, gap width, and ground plane void geometry as shown in Fig. 6.11. This enables the potential for much more efficient/smaller coils than able to be designed without aid of algorithms.

A fabricated ML design and measured result is shown in Fig. 6.12. In the provided photo, the ML design is compared to an earlier, published WPT system with bridge rectifier with 100 mm^2 coil area (this design was greatly improved upon in later dissertation work, thus not detailed in this dissertation). This ML receiver coil has 20.1 mm^2 area and peak 55.7% measured system efficiency at 3V output. A comparison with the measured $bridge_{2,2}$ and $bridge_{3,3}$ designs is shown in Table 6.1. The ML design is strictly superior to the $bridge_{3,3}$ design and has more than 60% area reduction compared to the $bridge_{2,2}$ design

Table 6.1: Comparison of ML design to other bridge designs

	ML Design	$bridge_{2,2}$	$bridge_{3,3}$
Efficiency	55.7%	63.3%	54.0%
Rx Coil Area	20.1 mm^2	53.3 mm^2	56.3 mm^2

with only 8% efficiency decrease. The ML algorithm enables much smaller receiver coil area without sacrificing much efficiency. Though the best designs with half-wave rectifier in this dissertation still offer an improved combination of coil area/efficiency, at varying output voltages, the following chapter on future work discusses how this same algorithm may be applied to great effect to further improve these designs as well.

6.2.5 4 Coil System with Boost Converter

The four coil link was measured at a distance of 30 mm. From Fig. 4.21, the rectifier output voltage with the reverse PDN is almost twice that of the two capacitor case, as the parallel resonance between the two capacitors greatly diminishes the output voltage as shown in Chapter 4. For the rectifier integrating the storage capacitance through the reverse PDN, the output was charged for a couple of minutes. Next, the 1.5V rectifier output with 20 mF total reverse PDN capacitance was used to power a Linear Technology LTC3400 boost converter with 3.2V, 10 mW load for approximately a second combined as shown in Fig. 6.13. From the output voltage and capacitance, a little over 2s worth of 10mW power is supplied, but much of this power is lost in the startup of the boost converter and efficiency loss of the boost converter while 'boosting'. Even so, by storing low voltage at large capacitance in the reverse PDN, 10 mW of discontinuous power at 3.2V could be supplied with a small power source (28 mW) and coil area (361 mm^2) at 30 mm distance. This is a unique approach to four coil systems as the source power is much smaller than typically seen in such systems, and an approach particularly suited for the needs of light load IoT applications with discontinuous power demands.

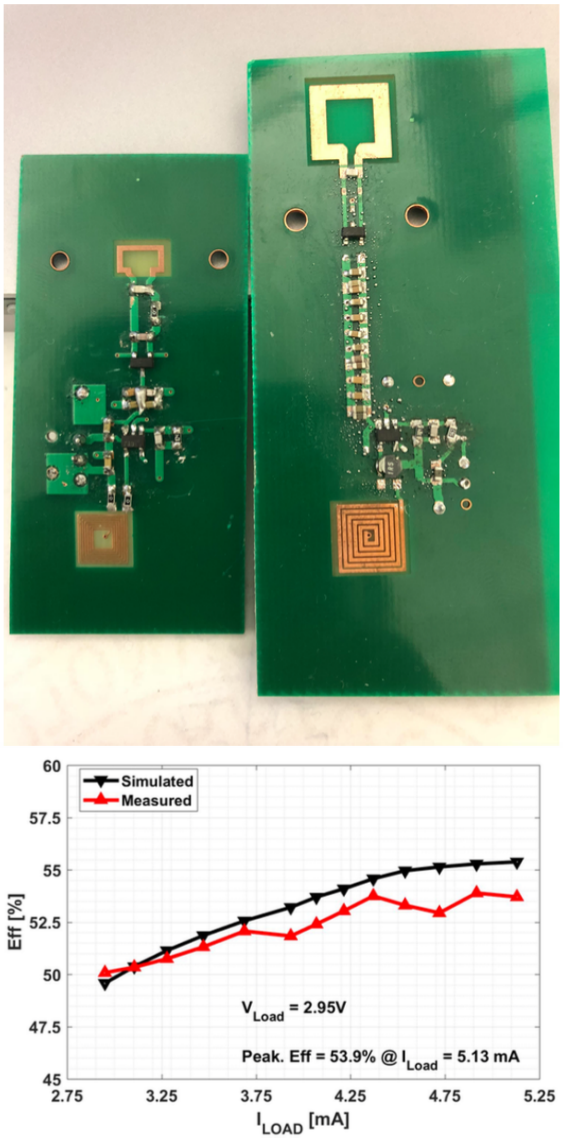

Figure 6.12: (a) Fabricated ML coil and comparison to an earlier design with 100 mm^2 coil area and (b) measured results

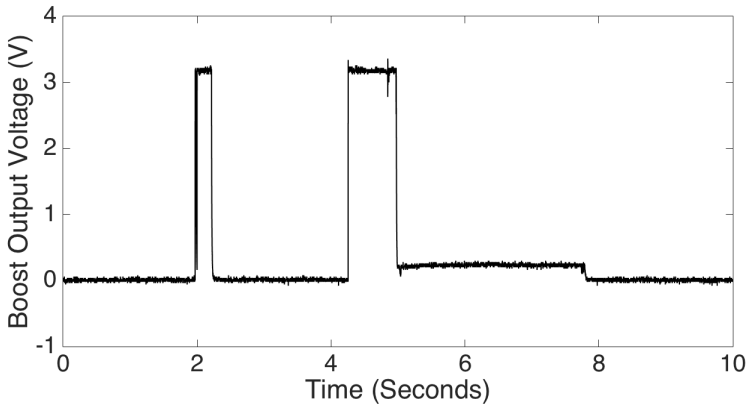

Figure 6.13: Measured boost converter output with reverse PDN in 4 coil system

6.3 Correlation with Calculated Efficiency Analysis and Loss Distribution

6.3.1 Calculated and Measured Efficiency Comparison

In this subsection, all measured results were shown previously in this chapter (not new results), but here compared with the efficiency analysis. A comparison of the measured and calculated efficiency analysis for the $bridge_{2,2}$ design at 1.2V output, 780 MHz is shown in Fig. 6.14(a), with the calculated subsystem efficiencies shown in Fig. 6.14(b). By tuning some of the variable modeling values, as discussed in Chapter 2, very good agreement between the calculated and measured efficiency is achieved. The calculated efficiency assumed 5cm of microstrip line length, and a Murata 1.5μH chip inductor with R_{AC} = 0.5Ω was used for the inductor AC loss calculation. At the largest output power, there is less than 1% efficiency difference between the calculated and measured efficiency. At the lowest output power, the error increases, likely due to overestimation of inductor loss.

One benefit to the proposed efficiency analysis is that the sources of the power loss can be compared to identify the areas to target for improved efficiency. At the lowest load power, the PDU is the dominant source of loss. This is because at the lowest load power, the PDU efficiency is lowest and inductor losses comprise a large portion of the overall loss. Moreover, rectifier and coil efficiencies are at their lowest at low load power. Due to

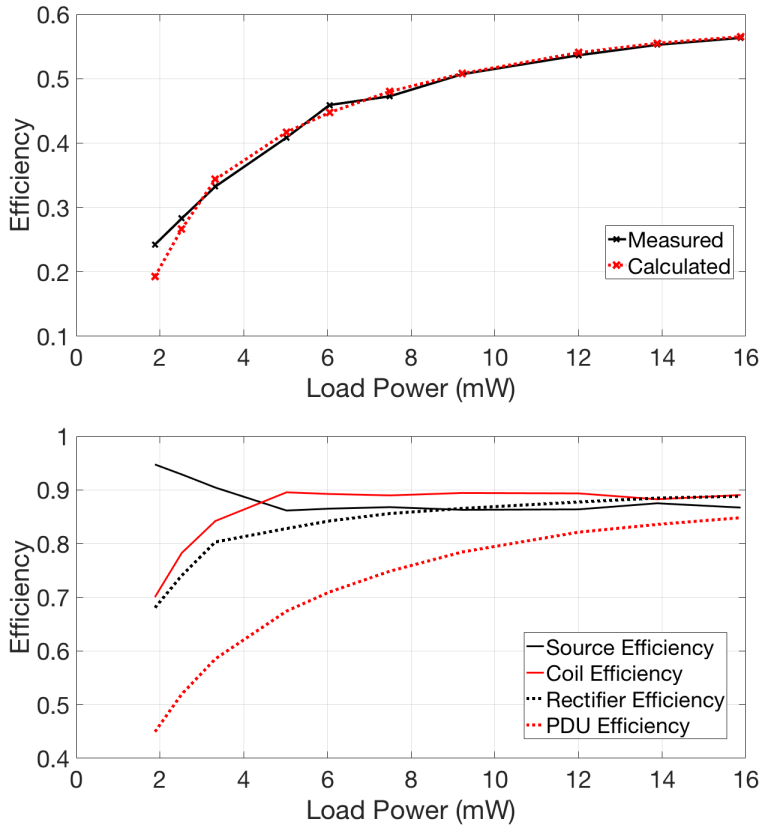

Figure 6.14: (a) Comparison between measured and calculated efficiency for $bridge_{2,2}$ and (b) calculated subsystem efficiency

small value of $V_{in,PDU}$ at lowest load power, the rectifier efficiency suffers from increased influence of forward voltage loss. As the value of R_{Load} is greatest at low load power for constant V_{out}, the corresponding increase in $R_{in,PDU}$ degrades the coil efficiency with this large loading resistance. Thus, from Chapter 2, improving the receive coil Q_2 would be the simplest path to improved coil efficiency. At the higher power loads, the source efficiency is a larger percentage of the power loss. This is because the higher power load has smaller load resistance, leading to a smaller value of R_{eq} and correspondingly lower source efficiency. To improve the efficiency at the highest load power, the transmit coil inductance or k should be increased.

A comparison between the measured and calculated efficiency for the $half_{2,1}$ system at 1mm transmission distance at both 1.2V and 3.3V PDU output is shown in Fig. 6.15.

Here, there is more error between the calculated and measured efficiency. The most likely culprit for this is the coil parameters used in the calculation - if the measurement occurs at a slightly different transmission distance (rather than the exact 1mm simulated) or there is slight difference in the k, Q, or L simulated, there will be discrepancy between measured and calculated efficiency. Because this comparison shows the most difference, it is likely there is some error in the simulated parameters of $coil_1$, as the systems using only $coil_2$ show much better agreement.

In the calculated individual subsystem efficiencies, the trends are similar to the $bridge_{2,2}$ efficiency trends. The source efficiency decreases slightly with load power, as R_{Load} decreases. The coil and PDU efficiency decrease sharply at the lightest loads. At this load power, R_{Load} is very high, and inductor loss comprises a larger portion of the overall loss, such that these efficiencies are very tough to design for at this load power. The rectifier efficiency stays relatively steady (with some variance for the ML modeling switching loss), decreasing slightly with load power. There is strange behavior in the calculated rectifier efficiency at the lightest load, due to the diode switching loss. At small load power, slight errors in the ML modeling diode switching loss are magnified. This error can be mitigated with increased training data.

A comparison between the measured and calculated efficiency for the $half_{2,2}$ system at 2.5mm transmission distance at both 1.2V and 3.3V PDU output is shown in Fig. 6.15. The agreement to measurement is much better here compared to $half_{2,1}$ at both output voltages, and the efficiency trend with load power is very similar to the measured data as well. As discussed earlier, this is likely because the simulated parameters for the $coil_{2,2}$ link are more accurate. This correlation demonstrates the robustness of the efficiency analysis for guiding design in various operating conditions, as this comparison is for a 2.5mm transmission distance.

The calculated subsystem efficiency demonstrates the efficiency analysis understands how the distribution of losses changes for different operating conditions. At the increased

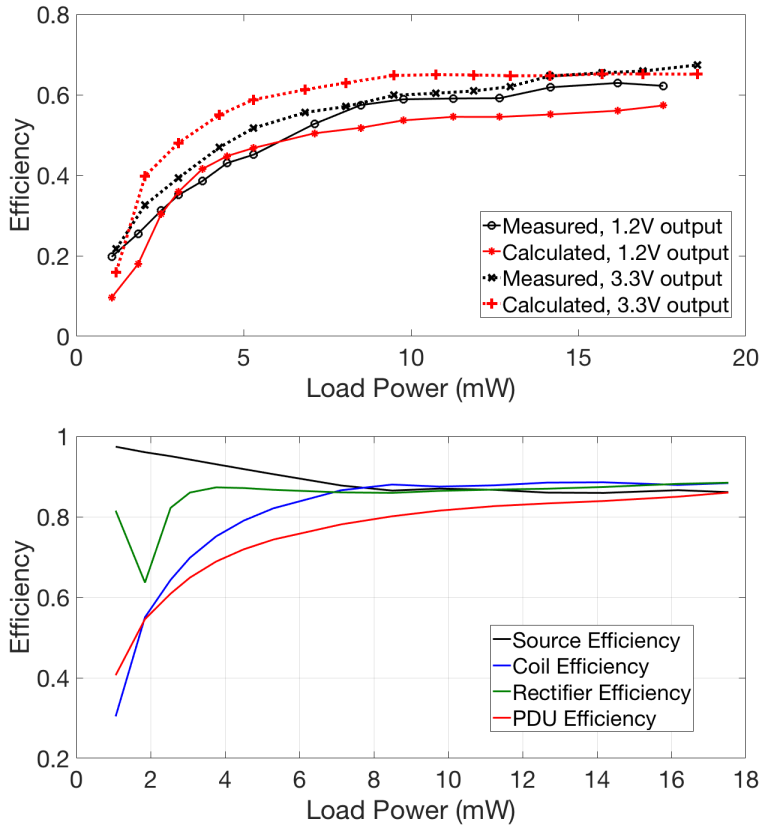

Figure 6.15: (a) Comparison between measured and calculated efficiency for $half_{2,1}$ at 1mm transmission and (b) calculated subsystem efficiency

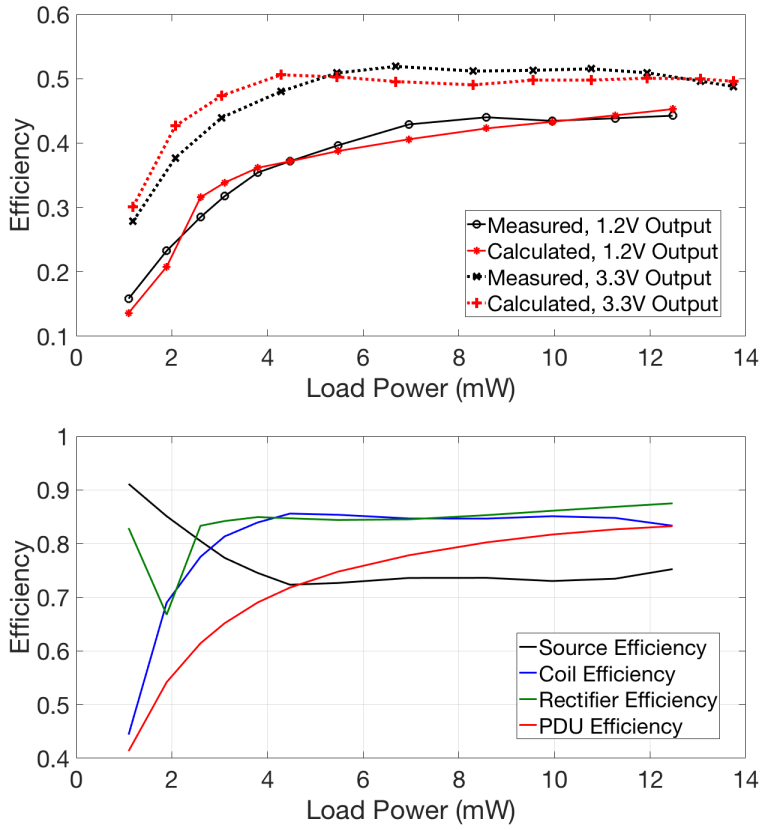

Figure 6.16: (a) Comparison between measured and calculated efficiency for $half_{2,2}$ at 2.5mm transmission distance and (b) calculated subsystem efficiency

transmission distance, the k is much smaller (approximately 0.23). Accordingly, the source efficiency is much less at larger load power when compared to the designs at 1mm while the other subsystems show much less difference, as agrees with intuition from previous discussion in this dissertation.

It should also be noted the bridge efficiency shows much better correlation with measurement. One explanation for this is the complex interaction of the half-wave rectifier with the coils as explained in Chapter 4. If the effective inductance of the coil is acting differently than the expectation from HFSS simulation, then the equations used to calculate the source and coil efficiencies cannot be expected to be as accurate as they would be for use with the bridge rectifier.

6.3.2 Measured PDU Input Voltage

The value of $V_{in,PDU}$ in measurement for a few test cases is shown in Fig. 6.17. This data shows that the efficiency analysis correlates with the general trends of the PDU input voltage with load power, but specific buck regulator peculiarities inhibit consistent, accurate prediction of this value. The $half_{2,2}$ link $V_{in,PDU}$ was measured with the TPS62615 at 1.2V output. Because simulated losses for the TPS62615 are not available, only measured data is available for this case. As the load power increases, the input voltage to the PDU increases. This is exactly as expected: at low output power the load resistance is largest. $V_{in,PDU}$ wants to be small, else the value of $R_{in,PDU}$ will be transformed to a very large value and greatly decrease the coil efficiency much more than the source efficiency would benefit (source efficiency is already large at this load range). In addition, larger value of $V_{in,PDU}$ would lead to larger PDU switching and PDU inductor AC loss. However, as the load power increases, R_{Load} decreases. Accordingly, $V_{in,PDU}$ increases, such that the transformed value of $R_{in,PDU}$ is increased and maintains its value better over the load range. The gains in source efficiency and rectifier efficiency (less forward voltage efficiency loss) by doing this outpace the losses in coil/PDU efficiency at higher power, larger $V_{in,PDU}$.

A similar trend is seen with the $half_{2,2}$ measurement at 1.2V output with the LTC3564 at 2.5mm, but here much more peculiar PDU behavior may observed. At 2.5mm transmission distance, $V_{in,PDU}$ needs to take a large value to overcome the low coupling coefficient else the source efficiency will be very low, even at large R_{Load}. In addition, after 5 mW, the measured PDU input voltage gradually increases as seen with the TPS62615, to overcome the decrease in R_{Load}. This is predicted by the efficiency analysis. However, in the 4-5 mW load region, an input voltage to the PDU below 2V is measured. First, these data points are at odds with rest of the data. More significantly, this value is more than half a Volt below the specified minimum operating input voltage for the LTC3564 - and the system successfully regulates! This is not measurement error, as this phenomenon was replicated in the $half_{2,1}$ system at 1mm transmission distance as well at similar loading conditions.

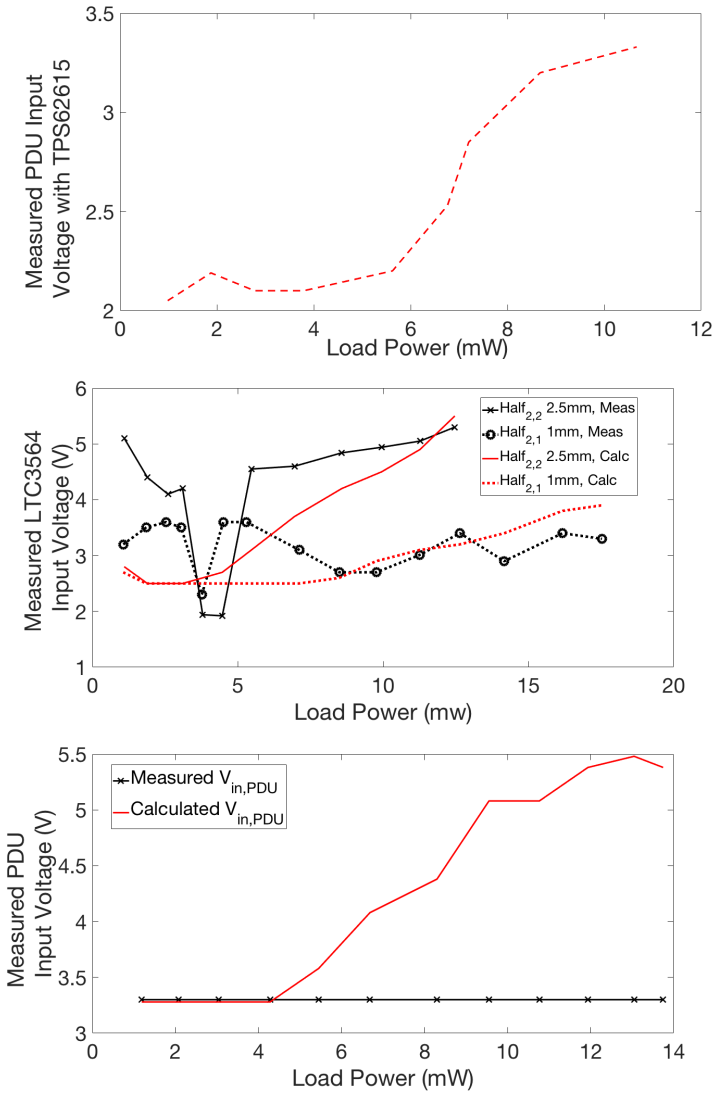

Figure 6.17: Measured $V_{in,PDU}$ for (a) $half_{2,2}$ at 1mm, 1.2V output with TPS62615 (b) $half_{2,2}$ at 2.5mm and $half_{2,1}$ at 1mm, 1.2V output with LTC3564 and (c) $half_{2,2}$ at 2.5mm, 3.3V output with LTC3564

While the exact cause of this is not known, it is suspected this is a transition point in the operating mode for the LTC3564 (based on the output current value and output voltage waveforms observed). As seen in Fig. 6.7, however, there is no unusual behavior in the system efficiency at this load power, meaning the efficiency analysis correlates much better with the measured efficiency than the measured PDU input voltage does. Compare $half_{2,2}$ at 2.5mm to $half_{2,1}$ at 1mm, however. $V_{in,PDU}$ shows no strong trend with $half_{2,1}$, though at 4 mW load the strange behavior is again observed. This is not surprising, as a large value of $V_{in,PDU}$ is not necessary for high source efficiency as the k is large. As the input power and load resistance is varied discretely, the variation in $V_{in,PDU}$ to dissipate slight extra, unneeded power is stronger than any trend due to load power in this range. Observe though that $V_{in,PDU}$ is smaller in this case than $half_{2,2}$ at 2.5mm distance. This is not what might be expected, as this is opposite of what was seen for these links at these distances without PDU in Chapter 3. At greater transmission distance the efficiency was less, so the rectifier output voltage was less for $half_{2,2}$ at 2.5mm distance than $half_{2,1}$ at 1mm. However, as captured in the developed efficiency analysis, the PDU input voltage settles at higher value in the increased transmission distance case to overcome the limitations of the small k on source efficiency. This is a crucial piece of data, as the measured PDU input voltage both validates the efficiency analysis procedure of varying $V_{in,PDU}$ to find the optimal efficiency and demonstrates the effect of source efficiency. If these two were not true, then the PDU voltage should not be higher at increased transmission distance at the same load power.

What happens when the PDU output voltage is greater than the minimum operating input voltage? As discussed in Chapter 2, the PDU input bootstraps to the output, and the PDU input voltage is equal to the output voltage at all values. The same measurement result has been observed for other coil links at other PDU output voltage greater than 2.5V for the LTC3564. This is not what the efficiency analysis predicts, as it suggests at the larger output power the input voltage should increase for improved source efficiency as seen in other measurements. However, the efficiency analysis still better predicts the system efficiency

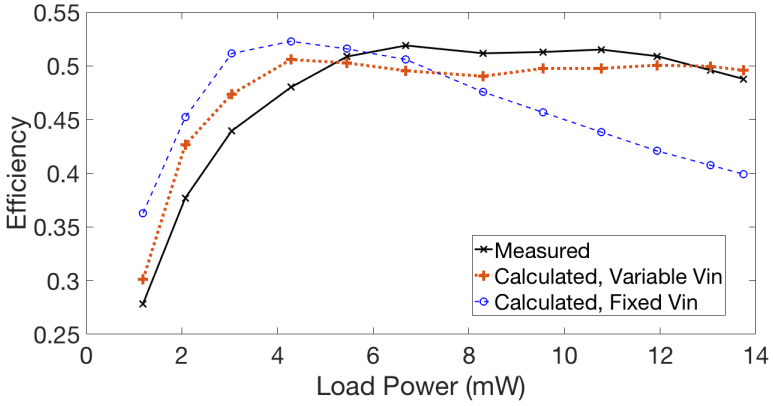

Figure 6.18: Comparison of measured and calculated efficiency for $half_{2,2}$ at 2.5mm transmission distance for variable $V_{in,PDU}$ (developed efficiency analysis) and fixed $V_{in,PDU}$

than trying to correlate the efficiency with the measurement. Calculating the power losses with the measured $V_{in,PDU}$, and $R_{in,PDU}$ equal to R_{Load}, leads to very inaccurate results, while using the modeled values from the efficiency analysis well predicts the system efficiency as shown in Fig. 6.18. In this comparison, the efficiency is calculated both as done normally in all other cases (variable $V_{in,PDU}$) and with assuming $V_{in,PDU} = V_{out}$ (fixed $V_{in,PDU}$). The best explanation for why the variable $V_{in,PDU}$ approach better matches the measured system efficiency, despite less measured agreement with $V_{in,PDU}$, is that while the equation for correlating $R_{in,PDU}$ and R_{Load} based on the PDU input/output voltage is generally true (2.14), the LTC3564 operates at times with complex behavior where that relationship does not hold. A better understanding of this dynamic would be a good area for future work. It should be noted that in the cases when $V_{in,PDU} = V_{out}$, the efficiency analysis uses the variable $V_{in,PDU}$ approach but assumes far reduced inductor losses, accounting for the very infrequent switching action in this case. The overall conclusion drawn is that while the efficiency analysis well predicts the general trends in the system efficiency under these various conditions, it cannot (and frankly should not) predict and capture unusual device specific behavior as it relates to the PDU input voltage and resistance. Thus as stated in Chapter 2, the developed efficiency analysis is ideal for guiding system design, but not for consistent, accurate predictions of the system efficiency.

Table 6.2: Comparison to RF near field coupling systems in literature

	Frequency	Load Power	Transmission Distance	Coil Area	Efficiency	Rectifier	PDU
$half_{4,4}$	700 MHz	19.3 mW	1 mm	64 mm^2	68.4%	Y	Y
$half_{4,1}$	689 MHz	17.4 mW	1 mm	33 mm^2	63.3%	Y	Y
$bridge_{2,2}$	780 MHz	17.4 mW	1 mm	53 mm^2	63.3%	Y	Y
$bridge_{3,3}$	1008 MHz	15.2 mW	1 mm	56 mm^2	54.0%	Y	Y
$half_{2,1}$	786 MHz	18 mW	1 mm	33 mm^2	67%	Y	Y
$half_{2,2}$	800 MHz	11 mW	2.5 mm	53 mm^2	51%	Y	Y
[25]	986 MHz	1 mW	5 mm	2.25 mm^2	7%	Y	Y
[56]	4.7 GHz	0.1 μW	1.2 mm	0.01 mm^2	1%	N	N
[54]	5.8 GHz	10 μW	1 mm	0.01 mm^2	1%	N	N
[47]	1 GHz	12 mW	30 μm	0.04 mm^2	14%	Y	N
[64]	460 MHz	10 μW*	200 mm	100 mm^2	0.6%	N	N

6.4 Comparison to State of Art

Multiple comparisons are made between the measured designs in this dissertation and prior art. First, a comparison to other RF near field coupling systems is shown in Table 6.2. This comparison demonstrates a RF WPT system has never been designed with such a system architecture and for these design goals before. Most RF near field coupling systems focus on achieving as small area as possible with the coil area, with little attention to efficiency or incorporating an integrated, regulated solution. This dissertation uses larger, though still not large, coil area to dramatically increase the efficiency to higher points than ever demonstrated before in RF near field coupling systems, for all full systems demonstrated! The table does not demonstrate an improved design approach compared to the prior art as the design goals for this dissertation are much different than the other RF near field coupling systems. Said another way, this dissertation applies RF near field coupling system much differently than has ever been previously demonstrated, incorporating high efficiency, power regulation, and integrated inductor in the same RF near field coupling receiver.

Next a comparison is made between the compact, integrated design with the TPS62615 and integrated inductor and other fully integrated WPT designs (with SMT inductor) as shown in Table 6.3. This dissertation design offers the best combination of efficiency and low coil area as an integrated solution for low power, regulated, compact IoT devices. None of the other designs utilize an embedded inductor.

Next a comparison is made to the best, regulated inductive resonant coupling systems

Table 6.3: Comparison to Integrated WPT Systems in Literature

Reference	Frequency	Load Power	Efficiency	Output Regulation	Coil Area
$half_{2,2}$	600 MHz	12 mW	43%	Yes	53 mm^2
[40]	6.78 MHz	5 W	51%	Yes	1600 mm^2
[63]	160 MHz	1 mW	1%	Yes	4 mm^2
[33]	100 MHz	741 mW	85.6%	No	100 mm^2
[30]	13.56 MHz	151 mW	15.1%	Yes	0.02 mm^2

Table 6.4: Comparison to Complete WPT Systems with Regulated Output

Reference	Frequency	Load Power	Transmission Distance	Coil Area	Efficiency
$half_{4,4}$	700 MHz	19.3 mW	1 mm	64 mm^2	68.4%
$half_{2,1}$	800 MHz	18 mW	1 mm	33 mm^2	67%
[23]	305 kHz	7.6 W	55 mm	12272 mm^2	76%
[35]	13.56 MHz	60 mW	3 mm	71 mm^2	50%
[58]	13.56 MHz	40 W	150 mm	80425 mm^2	70%
[30]	13.56 MHz	151 mW	140 μm	0.02 mm^2	15.1%
[40]	6.78 MHz	5 W	30 mm	1600 mm^2	51%
[25]	986 MHz	1 mW	5 mm	2.25 mm^2	7%

previously demonstrated in literature in Table 6.4. The $half_{4,4}$ and $half_{2,1}$ designs have slightly lower efficiency than the lower frequency WPT systems of [23] and [58], but much improved receiver coil area with decreased transmission distance and decreased load power. Compared to [35] and [40], both the efficiency and the coil area is improved. In [25] and [30], the coil area is much smaller than this designs of this dissertation, but the efficiency of the designs in this dissertation are much higher at similar transmission distance. While the transmission distance is smaller than all but [30], the purpose of this dissertation was to demonstrate a high efficiency, small coil area WPT system, and the final chapter will provide a discussion on a simple way to improve transmission distance without sacrificing efficiency as part of future work. This comparison demonstrates the dissertation objective has been met - if the design considerations for a WPT system are the best combination of coil area and efficiency, RF near field coupling is the leading option. In addition, the demonstration of $half_{4,4}$ is an integrated solution, with embedded inductor and regulated output across a wide range of output conditions, showing the fully integrated solutions coveted for WPT are possible in a RF near field coupling system.

Finally, a comparison is made to other low power, IoT oriented WPT systems in Table 6.5 at low voltage output. This comparison demonstrates the application space in which

Table 6.5: Comparison to IoT related power delivery systems

	Type	Frequency	Source Power	Efficiency	Load Power	Receive Element Area	Regulation	Transmission Distance
$half_{4,4}$ @ 1.2V output	Near Field Coupling	700 MHz	28 mW	52.8%	15.2 mW	64 mm^2	Y	1 mm
$half_{2,1}$ @ 1.2V output	Near Field Coupling	800 MHz	28 mW	62%	17 mW	33 mm^2	Y	1 mm
$4coil$	Near Field Coupling	967 MHz	28 mW	<1%	10 mW	361 mm^2	Y	30 mm
[13]	Harvesting	150 kHz	N/A	<1%	29 μW	250 mm^2 (solar cell)	Y	N/A
[17]	Farfield	30 GHz	10W	<1%	1 μW	8 mm^2	N	68 cm
[26]	Resonant Coupling	50 kHz	20 mW	<1%	3 μW	41 mm^2	Y	85 mm

the demonstrated RF near field coupling system is advantageous over other forms of WPT. The efficiencies shown are referenced to the source power, instead of the power received by the receiver (popular with rectenna metrics). The demonstrated system has larger load power than harvesting based WPT systems such as [13]. In addition, compared to farfield power transfer, the source power is much smaller, as well as much smaller in area compared to rectenna based systems such as [17]. The demonstrated RF near field coupling system is not strictly superior to all IoT based WPT systems. A harvesting WPT system can operate with unknown power source, and a farfield power transfer system has far superior transmission distance. Different applications will prefer different solutions. But for IoT applications needing milliwatt-scale power, small area, and high efficiency, especially wearables and battery charging for compact IoT devices, the demonstrated RF near field coupling architecture has value.

6.5 Discussion and Summary

Based on the measurements of the complete systems (and the analysis in the preceding chapters), it is clear that designing a near field coupling receiver to utilize an RF source has clear advantages for low power applications but likely not much utility otherwise. First and foremost, this dissertation has demonstrated that a RF near field coupling system with

regulated output, embedded passives, and greater than 50% efficiency is possible. This had never before been demonstrated in prior academic literature. Furthermore, it is clear that by using a RF source, the coil size may be much smaller than many previous, low frequency demonstrations.

The mW load application space is very important for this dissertation. Achieving high efficiency with such small coil area has never been demonstrated before, and low applications are more likely to need an integrated solution with small receiver area. The coil area is the biggest detriment to circuit area for other high efficiency systems, thus this dissertation has asserted and proven that RF operation can attain minimal coil area with greater than 50% efficiency. When designing a WPT charging solution for mW load power and maximizing efficiency and not transmission distance, designing the system for RF operation should be one of the (if not the) primary options.

Above mW load power, it is harder to justify RF design for NFC systems. First and foremost, there is an upper limit to the amount of input power this system can utilize before destroying the copper traces, even if the active components are updated for higher power architecture. Small coils integrated on organic substrate are not meant for high power use. Second, higher power applications (say 100W for a laptop charger) are fine with larger coil size to maximize efficiency. RF near field coupling has a fundamentally lower maximum efficiency than lower frequency systems, when factoring in microstrip losses, diode switching losses, and dynamic electromagnetic effects leading to difficulty designing the matching networks. When maximum power efficiency is the primary design objective, or if high efficiency at farther transmission distance is needed, RF operation will not be suitable for these design goals. Also, as discussed, the source efficiency for RF near field coupling is dependent on an adequately large value of $R_{in,PDU}$. If the load power is increased beyond 100 mW, without a very large increase in ouptut voltage, $R_{in,PDU}$ will substantially decrease such that high efficiency is no longer possible. In this way, low power applications and RFNFC systems are made for each other - low power applications need the small

coil area and efficiency afforded only through RFNFC, while RFNFC needs low power operation for high efficiency to be possible.

The final consideration for RF near field coupling systems is complexity. Without a doubt, there are modeling challenges and peculiarities in RFNFC systems not found in lower frequency systems. While the traditional resonant inductive coupling system can use the conventional equations to design a WPT link at lower frequency with little difficultly, the same cannot be said about RF. Various factors such as frequency detuning from microstrip lines, switching frequency mismatch between the PDU and rectifier, revised efficiency analysis, etc. must be considered for RFNFC design, moreso than lower frequency systems. Thankfully, these are the exact issues discussed and solved in the prior chapters of this dissertation!

CHAPTER 7
CONCLUSION

7.1 Future Work

The preceding chapters discussed the design, analysis, and challenges for RF near field coupling. While the demonstrated systems had the best combination of efficiency and coil area previously demonstrated in WPT, there are several areas this thesis could be extended to enhanced the application space of RF near field coupling. The following will discuss a few of the most interesting areas.

7.1.1 Decreasing Source Resistance

The biggest weakness with RF near field coupling is the transmission distance is limited compared to other WPT systems. The main culprit for this, as discussed earlier, is the source efficiency via the source resistance. If the source resistance is decreased, can the transmission distance be increased? Yes! This has already been demonstrated before in lower frequency WPT with a similar coil area, in [33], showing an unregulated system where the efficiency improved from 44.0% to 85.6% when using a source with 50Ω resistance vs using a bipolar amplifier source with 3.3Ω resistance a 2mm transmission distance. Figure 7.1 shows the effect of decreasing the source resistance on the system efficiency. For the $half_{4,4}$ coil link, the k that gives the same $\eta_{source} * \eta_{coil}$ greatly decreases as R_s decreases. If 3.3Ω source resistance is used, the k yielding the same efficiency is 0.108, which can lead to improved transmission distance. While that is still not improved over other WPT systems (if it was, then RF near field coupling would actually be the unquestionably best system architecture), this is an increase in the distance just by changing a parameter not controlled in this dissertation. Further transmission distance is possible at

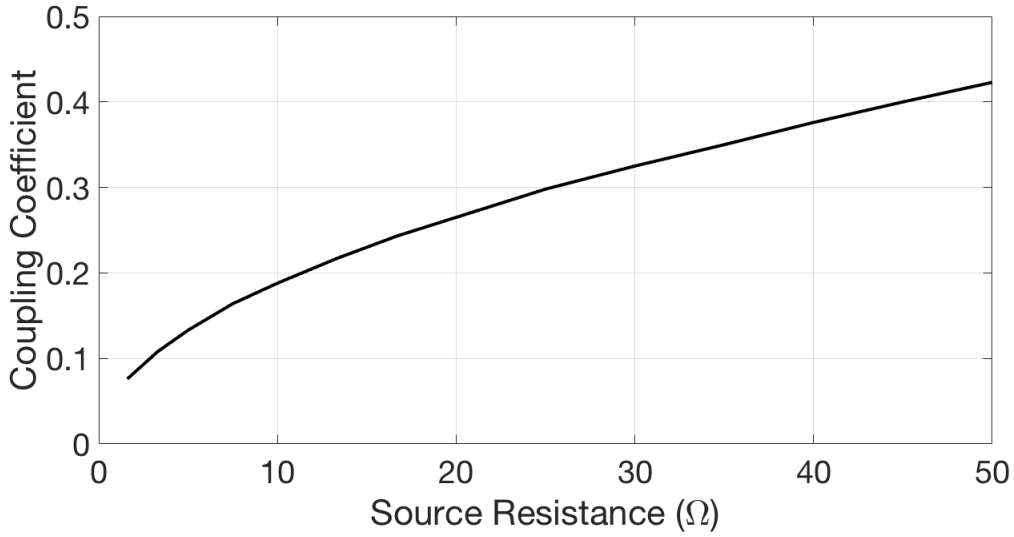

Figure 7.1: Coupling coefficient necessary for the same system efficiency as the source resistance changes. Efficiency calculated for $half_{4,4}$ system with 1000Ω rectifier load and 14.5 dBm, 700 MHz source

even smaller R_s or by sacrificing a little efficiency to meet application needs.

7.1.2 Application of Machine Learning

The application of a Two-Stage Bayesian Optimization (TSBO) algorithm to the coils and power inductor, using the simulation procedures developed as part of this dissertation, has already been demonstrated [94]. The results of this showed that the coil area can be greatly decreased with only small decrease in efficiency. However, this optimization was done without the calculated efficiency analysis, specifically not considering the source efficiency. In addition, relying on simulators such as ADS to determine what designs have optimal efficiency is less accurate than using analytical methods such as those developed in this dissertation, as was already demonstrated. Also, the optimization was done for RF near field coupling system with bridge rectifier - while this dissertation has demonstrated a half-wave rectifier is superior for efficiency.

The same algorithm can be reapplied to account for the transmit coil inductance (for improved source efficiency) while maximizing k and Q to further push the system effi-

ciency higher while decreasing the area of the receiver coil. The coils in this dissertation were designed with mainly two geometric parameters varied - the side length and the line width. The TSBO algorithm can include several more geometric factors, such as rectangular shapes, the ground plane cutout shape, etc, to find a more optimal design than possible using the 'hand-tuned' process of this dissertation.

7.1.3 Flexible Hybrid Electronics

Flexible hybrid electronics (HBE) is a rapidly developing research area. Based on the application space for low power, compact devices suitable for near field coupling, FHE is a natural area to apply RF near field coupling [97], [98]. For low power wearbles, RF near field coupling can help develop FHE charging systems with better efficiency and coil size than any other WPT method may offer.

The microstrip line loss in this thesis is not negligible. Depending on the design, over 5% loss could be observed just from the contribution of the microstrip line loss. An obvious improvement to the demonstrated system would be to design for high quality RF substrate rather than use FR4. While this dissertation used off the shelf components for the rectifier and regulator chip, Chapter 5 discussed the power inductor design for an integrated, 10 MHz buck converter. Specifically, smaller inductance was needed for this chip compared to the LTC3564, and a fully integrated system on package RF near field coupling system could integrate very high frequency buck converter, synchronous rectifier, and the designed RF coils for a very compact receiver with minimal area. Such a demonstration could take advantage of advanced substrates and multiple layers, the latter of particular interest to further decreasing power inductor area.

7.1.4 Figure of Merit for Inductive WPT Systems

One challenge with comparing WPT systems is that different efficiencies are possible at varying system parameters, making comparisons very difficult. For instance, refer back

to Table 6.2 to observe how the systems demonstrated in this dissertation are substantially different in operating conditions from any RF near field coupling system previously demonstrated. As such, comparisons are difficult when substantial difference in one system parameter, such as load power, has huge implications on efficiency. In fact, the key comparison in Table 6.4 is meant mainly to show that compared to the best inductive coupling systems, this work offers a unique combination of high efficiency and small coil area - not necessarily an improved system. These RFNFC systems operate at short transmission distance, where higher efficiency is more easily achieved compared to the transmission distances demonstrated in the other compared systems. However, this dissertation work also operates at lower power and with much smaller coil area, making high efficiency more challenging.

A figure of merit (FOM) to compare these systems would be of great utility. Varying system metrics, such as transmission distance, receiver coil area, load power, output voltage, etc would be included to robustly compare inductive WPT systems of very different operating conditions. The resultant FOM should show similar value/quality of work between this dissertation and the best systems compared in Table 6.4, representing high quality WPT implementations for a variety of application spaces. The development of this FOM could draw from data in published literature and the efficiency relationships drawn from the analysis in this dissertation.

7.1.5 Improved Efficiency Analysis

The demonstrated efficiency analysis has proven useful for guiding the design of RFNFC systems and for capturing many of the peculiarities of RFNFC systems. However, two major improvements would be useful for more consistent, precise analysis. First, understanding the complex interaction of the half wave rectifier with WPT systems, and any resulting changes in the efficiency analysis, needs to be completed. While the introduction of L_{half} as a modeling term is useful for predicting the shift in resonant frequency, how

this effects the calculation of the coil and source efficiency specifically is unknown.

Second, several of the measurements, specifically the measurement of the PDU input voltage, point towards pecularities in the chosen PDU (LTC3564) that are not sufficiently captured by the efficiency analysis. Understanding the exact relationship of $V_{in,PDU}$ and $R_{in,PDU}$ under various loading conditions is needed for more accurate system efficiency prediction, though the used modeling does provide a general approach that has good accuracy in the majority of cases, with sufficient accuracy for basing coil design on.

7.1.6 Multi-power Charging Platform

One area of interest, especially for the IoT, is how to charge devices with varying power requirements. One of the largest problems is providing enough power to charge high power devices, like a laptop, without overloading a lower power device being charged at the same time. RF near field coupling can provide a simple solution for this. Higher power, larger area, higher efficiency coils could be used to charge higher power devices at a frequency such as 13.56 MHz (such as previously demonstrated). Meanwhile, the charging platform can be configured to concurrently charge low power devices using RF near field coupling. Setup this way, a low power, compact device could be concurrently charged with high efficiency, without fear of being overloaded by the 13.56 MHz higher power source as the RF receiver coil is configured for much, much higher frequency. And because of the very different coil areas, integrating the different frequency charging coils in the same platform would also pose little issue.

7.2 Key Accomplishments

The main objective for this dissertation was completed: demonstrate that RF near field coupling offers a superior combination of coil area and efficiency for milliwatt-scale load power over other methods of WPT, while also demonstrating an integrated solution with embedded inductor and regulated output. In order to accomplish this, several research

contributions were accomplished, listed as follows with some key findings and conclusions in this dissertation for each contribution in what serves as a summary of the preceding:

- Novel efficiency modeling approach specific to RF near field coupling that determines not only system efficiency, but distribution of losses in the system. The modeling approach was validated with several measurements
  - Power losses specific to low power, RF system were categorized
  - The subsystem design tradeoffs were explored as a result of the analysis
  - The analysis determines the input voltage of the PDU, for a controlled power source system, by enforcing power matching at the input of the PDU and the output of the rectifier
  - Calculated efficiency analysis demonstrates improved accuracy over simulation based techniques, though error occurs when assuming no matching loss over a wide range of load resistance
- System architecture and design process for efficient RF near field coupling system, specifically identifying how the design approach differs from conventional inductive magnetic resonance coupling design
  - System architecture developed for continuous/discontinuous power demand
  - The design approach considers factors such as the transmit inductance, source efficiency, and complex relationship of load resistance to system efficiency not as significant in other WPT systems
  - Half-wave rectifiers yield optimal efficiency in a RFNFC, low power system
- Demonstration of a reverse power distribution network with measurement validation, as a key component for linking RF-DC conversion with a PDU.
  - Established target impedance from both the PDU and rectifier perspective

  - Identified phase as an important consideration in reverse PDN design
  - Developed design rules for integrating large storage capacitance in RFNFC system with the reverse PDN

- Identification and modeling of dynamic electromagnetic effects in RF near field coupling systems to pick the right component values in the circuit, especially the secondary resonant capacitor.
  - Half wave rectifiers interact with the RF coil resonant network differently than bridge rectifiers, leading to a downshift in frequency
  - Developed a process for selecting component values via the aid of simulators such as ADS, rather than relying on conventional equations

- Demonstration of cheap, simple packaging technology for integrating an embedded inductor with magnetic core into RFNFC receiver.
  - Completed design and characterization of embedded inductor for an integrated buck converter
  - Developed a revised inductor loss analysis for DCM buck regulator
  - Demonstrated integrated inductor with COTS buck regulator showing improved PDU efficiency compared to similar SMT inductor

- Meeting main dissertation objective of achieving very high efficiency with very small coil area in a RFNFC system in a reliable, integrated solution
  - All full systems demonstrated superior efficiency to all other RFNFC systems
  - Demonstrated systems demonstrate improved combination of efficiency and coil area compared to resonant coupling system at any frequency, at the expense of transmission distance

- Discussion and identification of the application space the developed RFNFC systems are advantageous compared to other low power WPT architectures

7.3 Conclusion and Summary

This dissertation discussed the advantages and limitations of RF near field coupling. This dissertation identified low power applications as a particularly suitable area to apply RF near field coupling. The body of this dissertation focused on the efficiency analysis, design process, integration and modeling challenges, packaging technology integration, and measurement demonstration of RF near field coupling systems with the best combination of system efficiency and coil area ever demonstrated in literature. Along the way, novel design approaches, new analysis techniques and equations, and innovative solutions to integration challenges were developed to meet the dissertation objectives.

When this research began, I had a very metric based validation of the work. If high efficiency was achieved, then the research must be good. In fact, these metrics were met months before the completion of this dissertation. But as this research matured, the contributions of this dissertation became less about the numbers and the comparison to state of art (while still important), and more about demonstrating the advantages and disadvantages of RF near field coupling and presenting solutions to challenges no one else had solved as no one else had previously demonstrated very high efficiency and very small coil area for RF WPT. I will not state that RF near field coupling is the 'best' WPT method, as the transmission distance is very limited, there is a maximum power limitation, and the theoretical best efficiency cannot match that of lower frequency systems. Nor will I claim that this dissertation represents the 'best' WPT work, because again that is viewing this dissertation incorrectly. What I can confidently state, and hopefully have demonstrated, is that there is a real application space for the high efficiency RF near field coupling systems demonstrated in this dissertation, and that this dissertation is a good resource for understanding the various challenges and design procedures specific to integrated solutions for

RF near field coupling. There is still more interesting work that can be done in the area of integrated RF near field coupling to increase efficiency, decrease area, and integrate more packaging technologies. Flexible hybrid electronics and system on package implementations can build on this work to make more practical systems for real applications. I sincerely hope this dissertation helps others utilize RF near field coupling for innovative and cutting edge applications. To move towards that end, I fully believe this dissertation offers a guide for anyone looking to explore and learn about high efficiency RF near field coupling, and ultimately this is the body of knowledge that I have added to the field of electrical engineering.

7.4 Publications

- Journals
  - **C. Pardue**, M. Bellaredj, A. K. Davis, M. Swaminathan, P. Kohl, T. Fujii, S. Nakazawa, "Design and Characterization of Inductors for Self-Powered IoT Edge Devices" in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 2018.
  - M.L.F. Bellaredj, **C. Pardue**, P. Kohl, M. Swaminathan, "Fabrication of package embedded spiral inductors with two magnetic layers for flexible SIP point of load converters in Internet of Everything devices,"in *Microelectronic Engineering*, 189, 2017.
  - **C. Pardue**, H. Torun, M. Bellaredj, M. Swaminathan, "RF Near Field Coupling System using Reverse PDN and Considering Electromagnetic Effects" in *IEEE Trans. on Electromagnetic Compatibility*, accepted (April 2018).
  - **C. Pardue**, A. K. Davis, M. Bellaredj, M. F. Amir, M. Swaminathan, S. Mukhopadhyay, "Reverse Power Delivery Network for Wireless Power Transfer" in *IEEE Microwave and Wireless Components Letters*, accepted (May 2018).

- **C. Pardue**, M. Bellaredj, H. Torun, M. Swaminathan, P. Kohl, A. K. Davis, "RF Wireless Power Transfer using Integrated Inductor" in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, submitted (April 2018).
- **C. Pardue**, et al, "System Level Modeling and Design for Regulated RF Near Field Coupling for IoT Applications" in *IEEE Internet of Things Journal*, (in progress).

- Conferences
  - **C. Pardue**, K. Naishadham, X. Song and M. Swaminathan, "Integration of carbon nanotube films with SRRs for air quality sensing applications," *WAMICON 2014*, Tampa, FL, 2014, pp. 1-3.
  - **C. Pardue**, M. Swaminathan and J. B. Balaguru, "Lossy frequency selective surfaces for gas sensing using ZnO films," *Proceedings of the 2015 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH15)*, Boston, MA, 2015, pp. 19-20.
  - **C. Pardue**, M. F. Bellaredj, A. K. Davis and M. Swaminathan, "Miniaturization of Planar Packaged Inductor Using NiZn and Low Cost Screen Printing Technique," *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, Orlando, FL, 2017, pp. 2275-2281.
  - **C. Pardue**, A. K. Davis, M. L. F. Bellaredj, and M. Swaminathan, "Wireless Power Transfer Integrated Board for Low Power IoT Applications", *2017 IEEE Conf. Technol. for Sustainable Technology (SusTech)*, Phoenix, AZ, 2017.
  - H. M. Torun, **C. Pardue**, et al, "Machine Learning Driven Advanced Packaging and System Miniaturization of IoT for Wireless Power Transfer Solutions," *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, 2018 accepted.

– **C. Pardue**, A. K. Davis, M. Bellaredj, M. Swaminathan, "Reverse Power Distribution Network and Phase Considerations for Low Power RF Near Field Coupling in IoT Applications" at *2018 IEEE Symposium on Electromagnetic Compatibility, Signal and Power Integrity (EMC+SIPI)*, Long Beach, CA, 2018 (accepted).

– **C. Pardue**, H. Torun, M. Bellaredj, M. Swaminathan, "System Level Efficiency Analysis for Regulated RF Near Field Coupling", at *2018 Wireless Power Transfer Conference (WPTC)*, Montreal, CA, 2018 (accepted).

Appendices

APPENDIX A

LITERATURE SURVEY COMPARISONS

A.1 Comparison of Inductive WPT Systems

A.2 Comparison of Frequency vs Coil Size

Table A.1: Complete Resonant Inductive Coupling Systems in Prior Literature

Reference	Transmission Frequency	Load Power	Transmission Distance	Receive Coil Area	Efficiency	Regulated Output
[23]	305 kHz	7.6 W	55 mm	122.7 cm^2	76%	Y
[24]	22 kHz	0.753 W	30 mm	19.6 cm^2	88.1%	N
[25]	986 MHz	1 mW*	5 mm	2.25 mm^2	7%	Y
[26]	50 kHz	4.2 μW	85 mm	41 mm^2	0.1%	Y
[27]	13.56 MHz	40 W	150 mm	804.2 cm^2	70%	Y
[28]	137 kHz	534 W	20 mm	200 cm^2	92%	N
[29]	100 kHz	6 W	200 mm	1576 cm^2	96%	Y
[30]	100 MHz	151 mW	140 μm	0.017 mm^2	15.1%	Y
[31]	13.56 MHz	24 mW	15 mm	1256.6 cm^2	49%	N
[32]	6.78 MHz	2 W	30 mm	2400 mm^2	72%	Y
[33]	107 MHz	856 mW	3 mm	100 mm^2	44%	N
[34]	100 kHz	10 W	100 mm	400 cm^2	72%	Y
[35]	13.56 MHz	60 mW	3 mm	70.9 mm^2	50%	Y
[36]	13.56 MHz	8 W	30 mm	100 cm^2	84%	N
[37]	134 kHz	295 W	10 mm	169 cm^2	76%	N
[38]	6.78 MHz	600 mW	5 mm	201 mm^2	42.1%	Y
[39]	6.78 MHz	10 W	5 mm	14.5 cm^2	80%	N
[40]	6.78 MHz	5 W	30 mm	1600 mm^2	51%	Y
[41]	90 kHz	3300 W	200 mm	3600 cm^2	96.6%	N
[42]	435 kHz	3500 W	150 mm	314 cm^2	82.1%	Y
[43]	5 MHz	5 W	300 mm	707 cm^2	65.9%	N
[44]	1 MHz	4.5 W	100 mm	187 cm^2	76.3%	N
[45]	1 MHz	8 W	50 mm	79 cm^2	70%	Y
[46]	22 kHz	6600 W	162 mm	3795 cm^2	94.4%	N
[47]	1 GHz	12 mW	30 μm	0.04 mm^2	14%	N
[48]	46.7 kHz	420 W	200 mm	177 cm^2	90%	N
[49]	1 MHz	2 W	200 mm	707 cm^2	73.6%	Y
[50]	250 kHz	1500 W	80 mm	707 cm^2	95.6%	Y
[51]	500 kHz	100 W	10 mm	71 cm^2	88%	N
[52]	100 kHz	4.5 W	20 mm	573 mm^2	65%	Y
[53]	230 MHz	12 mW	50 μm	0.25 mm^2	13%	N

Table A.2: Resonant Inductive Coupling Coils in Literature

Reference	Frequency	Load Power	Transmission Distance	Coil Area	Efficiency	Rectifier
[23]	305 kHz	7.6 W	55 mm	122.7 cm^2	76%	Y
[22]	85 kHz	560 W	100 mm	1600 cm^2	90%	Y
[24]	22 kHz	0.753 W	30 mm	19.6 cm^2	88.1%	Y
[25]	986 MHz	1 mW*	5 mm	2.25 mm^2	7%	Y
[26]	50 kHz	4.2 μW	85 mm	41 mm^2	0.1%	Y
[27]	13.56 MHz	40 W	150 mm	804.2 cm^2	70%	Y
[28]	137 kHz	534 W	20 mm	200 cm^2	92%	Y
[29]	100 kHz	6 W	200 mm	1576 cm^2	96%	Y
[30]	100 MHz	151 mW	140 μm	0.017 mm^2	15.1%	Y
[55]	13.56 MHz	5 W	50 mm	176 cm^2	90%	N
[31]	13.56 MHz	24 mW	15 mm	1256.6 mm^2	49%	Y
[32]	6.78 MHz	2 W	30 mm	2400 mm^2	72%	Y
[33]	107 MHz	856 mW	3 mm	100 mm^2	44%	Y
[34]	100 kHz	10 W	100 mm	400 cm^2	72%	Y
[56]	4.7 GHz	0.1 μW	1.2 mm	0.01 mm^2	1%	N
[57]	6.78 MHz	6 W	N/A	899 mm^2	49%	Y
[35]	13.56 MHz	60 mW	3 mm	70.9 mm^2	50%	Y
[36]	13.56 MHz	8 W	30 mm	100 cm^2	84%	Y
[37]	134 kHz	295 W	10 mm	169 cm^2	76%	Y
[38]	6.78 MHz	600 mW	5 mm	201 mm^2	42.1%	Y
[39]	6.78 MHz	10 W	5 mm	14.5 cm^2	80%	Y
[53]	300 kHz	40 mW	500 mm	12.6 cm^2	1.5%	N
[59]	60 MHz	1.3 mW	16 mm	1.13 mm^2	2.4%	N
[40]	6.78 MHz	5 W	30 mm	1600 mm^2	51%	Y
[41]	90 kHz	3300 W	200 mm	3600 cm^2	96.6%	Y
[42]	435 kHz	3500 W	150 mm	314 cm^2	82.1%	Y
[43]	5 MHz	5 W	300 mm	707 cm^2	65.9%	Y
[44]	1 MHz	4.5 W	100 mm	187 cm^2	76.3%	Y
[45]	1 MHz	8 W	50 mm	79 cm^2	70%	Y
[54]	5.8 GHz	10 μW	1 mm	0.01 mm^2	1%	N
[46]	22 kHz	6600 W	162 mm	3795 cm^2	94.4%	Y
[47]	1 GHz	12 mW	30 μm	0.04 mm^2	14%	Y
[60]	700 kHz	100 mW	20 mm	380 mm^2	82%	N
[48]	46.7 kHz	420 W	200 mm	177 cm^2	90%	Y
[49]	1 MHz	2 W	200 mm	707 cm^2	73.6%	Y
[61]	100 MHz	N/A	140 μm	2.25 mm^2	34%	Y
[50]	250 kHz	1500 W	80 mm	707 cm^2	95.6%	Y
[62]	20 kHz	5000 W	150 mm	1920 cm^2	90%	N
[63]	160 MHz	2 mW	10 mm	4.36 mm^2	1%	N
[64]	460 MHz	10 μW*	200 mm	100 mm^2	0.6%	N
[51]	500 kHz	100 W	10 mm	71 cm^2	88%	Y
[52]	100 kHz	4.5 W	20 mm	573 mm^2	65%	Y
[53]	230 MHz	12 mW	50 μm	0.25 mm^2	13%	Y

BIBLIOGRAPHY

[1] Intel.com, 'The Internet of Things Start with Intel Inside', 2018. [Online]. Available: https://www.intel.com/content/www/us/en/internet-of-things/overview.html. [Accessed: 1- Jan- 2018]

[2] M. Nariman, F. Shirinfar, S. Pamarti, A. Rofougaran and F. De Flaviis, "High-Efficiency Millimeter-Wave Energy-Harvesting Systems With Milliwatt-Level Output Power," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 6, pp. 605-609, June 2017.

[3] G. Sun, B. Muneer, Y. Li and Q. Zhu, "Ultracompact Implantable Design With Integrated Wireless Power Transfer and RF Transmission Capabilities," *IEEE Transactions on Biomedical Circuits and Systems*, vol. PP, no. 99, pp. 1-11.

[4] T. P. Delhaye, N. Andr, S. Gilet, C. Gimeno, L. A. Francis and D. Flandre, "High-efficiency wireless power transfer for mm-size biomedical implants," *2017 IEEE SENSORS*, Glasgow, 2017, pp. 1-3.

[5] Y. Bu and S. C. Mukhopadhyay, "Equalization Method of the Wireless Power Transfer in an Electronic Shelf Label Power Supply System," *IEEE Transactions on Magnetics*, vol. 53, no. 11, pp. 1-5, Nov. 2017.

[6] E. Heo, K. Choi, J. Kim, J. Park, and H. Lee, "A wearable textile antenna for wireless power transfer by magnetic resonance," in *Textile Research Journal*, 2017.

[7] businesswire.com, "Dialog Semiconductor and Bosch Sensortec Collaborate on Low Power Smart Sensor Wireless Platform for IoT Devices", 2015. [Online]. Available: https://www.businesswire.com/news/home/20151012006222/en/Dialog-

Semiconductor-Plc.-Dialog-Semiconductor-Bosch-Sensortec. [Accessed: 1- Feb-2018]

[8] U. Muncuk, K. Alemdar, J. D. Sarode and K. R. Chowdhury, "Multi-band Ambient RF Energy Harvesting Circuit Design for Enabling Battery-less Sensors and IoTs," *IEEE Internet of Things Journal*, vol. PP, no. 99, pp. 1-1.

[9] S. Keyrouz, H. J. Visser and A. G. Tijhuis, "Ambient RF energy harvesting from DTV stations," *2012 Loughborough Antennas and Propagation Conference (LAPC)*, Loughborough, 2012, pp. 1-4.

[10] V. Palazzi et al., "Design of a ultra-compact low-power rectenna in paper substrate for energy harvesting in the Wi-Fi band," *2016 IEEE Wireless Power Transfer Conference (WPTC)*, Aveiro, 2016, pp. 1-4.

[11] D. Ferreira, L. Sismeiro, A. Ferreira, R. F. S. Caldeirinha, T. R. Fernandes and I. Cuias, "Hybrid FSS and Rectenna Design for Wireless Power Harvesting," *IEEE Transactions on Antennas and Propagation*, vol. 64, no. 5, pp. 2038-2042, May 2016.

[12] W. Guo, S. Zhou, Y. Chen, S. Wang, X. Chu and Z. Niu, "Simultaneous Information and Energy Flow for IoT Relay Systems with Crowd Harvesting," in *IEEE Communications Magazine*, vol. 54, no. 11, pp. 143-149, November 2016.

[13] X. Liu and E. Sanchez-Sinencio, "A Highly Efficient Ultralow Photovoltaic Power Harvesting System With MPPT for Internet of Things Smart Nodes," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 12, pp. 3065-3075, Dec. 2015.

[14] Y. K. Ramadass and A. P. Chandrakasan, "A Battery-Less Thermoelectric Energy Harvesting Interface Circuit With 35 mV Startup Voltage," in *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 333-341, Jan. 2011.

[15] K. W. Choi, A. A. Aziz, D. Setiawan, N. M. Tran, L. Ginting and D. I. Kim, "Distributed Wireless Power Transfer System for Internet-of-Things Devices," in *IEEE Internet of Things Journal*, vol. PP, no. 99, pp. 1-1.

[16] K. S. Yildirim, R. Carli and L. Schenato, "Safe Distributed Control of Wireless Power Transfer Networks," in *IEEE Internet of Things Journal*, vol. PP, no. 99, pp. 1-1.

[17] J. Charthad, N. Dolatsha, A. Rekhi and A. Arbabian, "System-Level Analysis of Far-Field Radio Frequency Power Delivery for mm-Sized Sensor Nodes," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 2, pp. 300-311, Feb. 2016.

[18] F. Erkmen, T. S. Almoneef and O. M. Ramahi, "Electromagnetic Energy Harvesting Using Full-Wave Rectification," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 5, pp. 1843-1851, May 2017.

[19] C. Song et al., "Matching Network Elimination in Broadband Rectennas for High-Efficiency Wireless Power Transfer and Energy Harvesting," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 5, pp. 3950-3961, May 2017.

[20] R. Jegadeesan, K. Agarwal, Y. X. Guo, S. C. Yen and N. V. Thakor, "Wireless Power Delivery to Flexible Subcutaneous Implants Using Capacitive Coupling," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 1, pp. 280-292, Jan. 2017.

[21] C. Y. Liou, C. J. Kuo and S. G. Mao, "Wireless-Power-Transfer System Using Near-Field Capacitively Coupled Resonators," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 9, pp. 898-902, Sept. 2016.

[22] G. Buja, M. Bertoluzzo and K. N. Mude, "Design and Experimentation of WPT Charger for Electric City Car," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 12, pp. 7436-7447, Dec. 2015.

[23] D. Ahn, S. Kim, J. Moon and I. K. Cho, "Wireless Power Transfer With Automatic Feedback Control of Load Resistance Transformation", in *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7876-7886, Nov. 2016.

[24] M. T. Ali, A. Anwar, U. Tayyab, Y. Iqbal, T. Tauqeer and U. Nasir, "Design of high efficiency wireless power transmission system at low resonant frequency," *2014 16th International Power Electronics and Motion Control Conference and Exposition*, Antalya, 2014, pp. 1128-1133.

[25] F. L. Cabrera and F. R. de Sousa, "Achieving Optimal Efficiency in Energy Transfer to a CMOS Fully Integrated Wireless Power Receiver", in *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 11, pp. 3703-3713, Nov. 2016.

[26] M. Choi, T. Jang, J. Jeong, S. Jeong, D. Blaauw and D. Sylvester, "A Resonant Current-Mode Wireless Power Receiver and Battery Charger With -32 dBm Sensitivity for Implantable Systems," in *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2880-2892, Dec. 2016.

[27] M. Fu, H. Yin, X. Zhu and C. Ma, "Analysis and Tracking of Optimal Load in Wireless Power Transfer Systems", in *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3952-3963, July 2015.

[28] G. Guidi and J. A. Suul, "Minimizing Converter Requirements of Inductive Power Transfer Systems With Constant Voltage Load and Variable Coupling Conditions," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 6835-6844, Nov. 2016.

[29] K. Hata, T. Imura and Y. Hori, "Maximum efficiency control of wireless power transfer via magnetic resonant coupling considering dynamics of DC-DC converter for moving electric vehicles," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015, pp. 3301-3306.

[30] J. Song, S. Park, S. Kim, J. J. Kim and J. Kim, "Active Silicon Interposer Design for Interposer-Level Wireless Power Transfer Technology for High-Density 2.5-D and 3-D ICs," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 6, no. 8, pp. 1148-1161, Aug. 2016.

[31] S. Iguchi, P. Yeon, H. Fuketa, K. Ishida, T. Sakurai and M. Takamiya, "Wireless Power Transfer With Zero-Phase-Difference Capacitance Control," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 4, pp. 938-947, April 2015.

[32] S. Y. Kim, T. Y. Kim and J. R. Choi, "Design of high efficiency resonant coil and receiver IC for wireless power transfer in mobile device," *2016 5th International Conference on Modern Circuits and Systems Technologies (MOCAST)*, Thessaloniki, 2016, pp. 1-4.

[33] S. Kim et al., "High-Efficiency PCB- and Package-Level Wireless Power Transfer Interconnection Scheme Using Magnetic Field Resonance Coupling", in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 5, no. 7, pp. 863-878, July 2015.

[34] D. Kobayashi, T. Imura and Y. Hori, "Real-time coupling coefficient estimation and maximum efficiency control on dynamic wireless power transfer using secondary DC-DC converter," *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, Yokohama, 2015, pp. 004650-004655.

[35] X. Li, C. Y. Tsui and W. H. Ki, "A 13.56 MHz Wireless Power Transfer System With Reconfigurable Resonant Regulating Rectifier and Wireless Power Control for Implantable Medical Devices," in *IEEE Journal of Solid-State Circuits*, vol. 50, no. 4, pp. 978-989, April 2015.

[36] M. Liu, Y. Qiao, S. Liu and C. Ma, "Analysis and Design of A Robust Class E^2

DC-DC Converter for Megahertz Wireless Power Transfer," in *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2835-2845, April 2017.

[37] Z. N. Low, R. A. Chinga, R. Tseng and J. Lin, "Design and Test of a High-Power High-Efficiency Loosely Coupled Planar Wireless Power Transfer System," in *IEEE Transactions on Industrial Electronics*, vol. 56, no. 5, pp. 1801-1812, May 2009.

[38] Y. Lu, M. Huang, L. Cheng, W. H. Ki, S. P. U and R. P. Martins, "A Dual-Output Wireless Power Transfer System With Active Rectifier and Three-Level Operation," in *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 927-930, Feb. 2017.

[39] H. Mao, B. Yang, Z. Li and S. Song, "Controlled-resonance power architecture enables efficient flexible wireless power transfer," *2016 IEEE Wireless Power Transfer Conference (WPTC)*, Aveiro, 2016, pp. 1-4.

[40] J. Moon, H. Hwang, B. Jo, C. K. Kwon, T. G. Kim and S. W. Kim, "Design and implementation of a high-efficiency 6.78MHz resonant wireless power transfer system with a 5W fully integrated power receiver," in *IET Power Electronics*, vol. 10, no. 5, pp. 577-587, 4 21 2017.

[41] S. Moon and G. W. Moon, "Wireless power transfer system with an asymmetric 4-coil resonator for electric vehicle battery chagers," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015, pp. 1650-1657.

[42] A. Moradi, F. Tahami and M. A. GhaziMoghadam, "Wireless Power Transfer Using Selected Harmonic Resonance Mode," in *IEEE Transactions on Transportation Electrification*, vol. 3, no. 2, pp. 508-519, June 2017.

[43] T. Nagashima et al., "Analytical design procedure for resonant inductively coupled wireless power transfer system with class-E^2 DC-DC converter," *2014 IEEE International Symposium on Circuits and Systems (ISCAS)*, Melbourne VIC, 2014, pp. 113-116.

[44] T. Nagashima, X. Wei, E. Bou, E. Alarcon, M. K. Kazimierczuk and H. Sekiya, "Analysis and Design of Loosely Inductive Coupled Wireless Power Transfer System Based on Class-E^2 DC-DC Converter for Efficiency Enhancement," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 11, pp. 2781-2791, Nov. 2015.

[45] Y. Narusue, Y. Kawahara and T. Asami, "Maximum efficiency point tracking by input control for a wireless power transfer system with a switching voltage regulator," *2015 IEEE Wireless Power Transfer Conference (WPTC)*, Boulder, CO, 2015, pp. 1-4.

[46] O. C. Onar, S. L. Campbell, L. E. Seiber, C. P. White and M. Chinthavali, "A high-power wireless charging system development and integration for a Toyota RAV4 electric vehicle," *2016 IEEE Transportation Electrification Conference and Expo (ITEC)*, Dearborn, MI, 2016, pp. 1-8.

[47] L. Sun, J. Xu, W. Mao, S. Zou, P. Lv and X. Zhu, "1GHz wireless power delivery using 0.2x0.2mm^2 on-chip inductor for 3-D stacked chips," *2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Singapore, 2015, pp. 475-478.

[48] S. Samanta and A. K. Rathore, "Wireless power transfer technology using full-bridge current-fed topology for medium power applications," in *IET Power Electronics*, vol. 9, no. 9, pp. 1903-1913, 7 27 2016.

[49] J. Youn and J. R. Choi, "High efficiency magnetic resonance wireless power transfer system and charging IC for mobile devices," *2015 11th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Glasgow, 2015, pp. 224-227.

[50] A. Q. Cai and L. Siek, "A 2-kW, 95% Efficiency Inductive Power Transfer System Using Gallium Nitride Gate Injection Transistors," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 458-468, March 2017.

[51] C. Zheng, L. Zhang, X. Zhao, J. Choe and J. S. Lai, "Asymmetrical loosely coupled transformer for wireless laptop charger with higher misalignment tolerance," *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015, pp. 3119-3126.

[52] W. X. Zhong and S. Y. R. Hui, "Maximum Energy Efficiency Tracking for Wireless Power Transfer Systems," in *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 4025-4034, July 2015.

[53] W. Mao, L. Sun, J. Xu, J. Wu and X. Zhu, "Analysis and design of high performance wireless power delivery using on-chip octagonal inductor in 65-nm CMOS," *2015 28th IEEE International System-on-Chip Conference (SOCC)*, Beijing, 2015, pp. 401-405.

[54] B. T. Nukala, J. Tsay, D. Y. C. Lie, J. Lopez and T. Q. Nguyen, "Efficient near-field inductive wireless power transfer for miniature implanted devices using strongly coupled magnetic resonance at 5.8 GHz," *2016 Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS)*, Waco, TX, 2016, pp. 1-4.

[55] H. M. Hsu, W. Z. Huang, G. W. Lee and C. Y. Chen, "Coil distance effect in magnetic resonance power transfer system," *2016 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Taipei, 2016, pp. 1-3.

[56] N. C. Kuo, B. Zhao and A. M. Niknejad, "Inductive Wireless Power Transfer and Uplink Design for a CMOS Tag With 0.01 mm^2 Coil Size," in *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 10, pp. 852-854, Oct. 2016.

[57] Ron-Chi Kuo, P. Riehl, A. Satyamoorthy, W. Plumb, P. Tustin and Jenshan Lin, "A 3D resonant wireless charger for a wearable device and a mobile phone," *2015 IEEE Wireless Power Transfer Conference (WPTC)*, Boulder, CO, 2015, pp. 1-3.

[58] M. Fu, C. Ma and X. Zhu, "A Cascaded BoostBuck Converter for High-Efficiency Wireless Power Transfer Systems," in *IEEE Transactions on Industrial Informatics*, vol. 10, no. 3, pp. 1972-1980, Aug. 2014.

[59] S. A. Mirbozorgi, P. Yeon and M. Ghovanloo, "Robust Wireless Power Transmission to mm-Sized Free-Floating Distributed Implants," in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 11, no. 3, pp. 692-702, June 2017.

[60] A. K. RamRakhyani, S. Mirabbasi and M. Chiao, "Design and Optimization of Resonance-Based Efficient Wireless Power Delivery Systems for Biomedical Implants," in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 5, no. 1, pp. 48-63, Feb. 2011.

[61] J. Song, S. Jeong, S. Park, J. Kim, Y. Cho and J. Kim, "PCB-package to chip wireless power transfer scheme using magnetic-field resonance coupling for high-density 3-D IC," *2016 IEEE Wireless Power Transfer Conference (WPTC)*, Aveiro, 2016, pp. 1-4.

[62] S. Wang, D. G. Dorrell, Y. Guo and M. F. Hsieh, "Inductive Charging Coupler With Assistive Coils," in *IEEE Transactions on Magnetics*, vol. 52, no. 7, pp. 1-4, July 2016.

[63] M. Zargham and P. G. Gulak, "Fully Integrated On-Chip Coil in 0.13 $murmm$ CMOS for Wireless Power Transfer Through Biological Media," in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 9, no. 2, pp. 259-271, April 2015.

[64] B. Zhao, N. C. Kuo and A. M. Niknejad, "A Gain Boosting Array Technique for Weakly-Coupled Wireless Power Transfer," in *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 7130-7139, Sept. 2017.

[65] Y. Kondo et al., "Embedded planar power inductor technology for package-level DC power grid," *2015 International Conference on Electronics Packaging and iMAPS All Asia Conference (ICEP-IAAC)*, Kyoto, 2015, pp. 814-817.

[66] J. Li, V. Tseng, Z. Xiao and H. Xie, ”A High-Q In-Silicon Power Inductor Designed for Wafer-Level Integration of Compact DC-DC Converters,” in *IEEE Transactions on Power Electronics* , vol.PP, no.99, pp.1-1.

[67] D. H. Bang and J. Y. Park, ”Ni-Zn Ferrite Screen Printed Power Inductors for Compact DC-DC Power Converter Applications,” in *IEEE Transactions on Magnetics*, vol. 45, no. 6, pp. 2762-2765, June 2009.

[68] L. L. Jenkins, J. M. Aggas, B. K. Rhea, W. E. Abell, C. G. Wilson and R. N. Dean, ”Design and implementation of planar inductors for low voltage GaN-based power converters,” *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015, pp. 1381-1387.

[69] Y. Nour, Z. Ouyang, A. Knott and I. H. H. Jorgensen, ”Design and implementation of high frequency buck converter using multi-layer PCB inductor,” *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, 2016, pp. 1313-1317.

[70] Z. Dang and J. A. A. Qahouq, ”On-chip coupled power inductor for switching power converters,” *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Fort Worth, TX, 2014, pp. 2854-2859.

[71] N. Tang et al., ”Fully Integrated Buck Converter With Fourth-Order Low-Pass Filter,” in *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3700-3707, May 2017.

[72] Chih-Shen Yeh, Xiaonan Zhao and Jih-Sheng Lai, ”A MHz zero voltage switching (ZVS) tapped-inductor buck converter for wide-input high step-down low-power applications,” *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, Kaohsiung, 2017, pp. 494-499.

[73] C. Yan, Z. Gan and E. Salman, ”In-package spiral inductor characterization for high

efficiency buck converters," *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, MD, 2017, pp. 1-4.

[74] S. W. Yoon, T. S. Dang, N. D. H. Lai and J. Y. Park, "Efficient Wi-Fi Power Amplifier LTCC Module Using a Buck Converter With a Power Inductor Implemented in Ferrite-Filled PCB Technology," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 5, no. 7, pp. 887-894, July 2015.

[75] A. Berger, M. Agostinelli, C. Sandner, S. Vesti and M. Huemer, "High efficient integrated power receiver for a Qi compliant Wireless Power Transfer system," *2016 IEEE Wireless Power Transfer Conference (WPTC)*, Aveiro, 2016, pp. 1-4.

[76] A. Kavungal Davis, "Effect of magnetic coupling between the mounting loops of two parallel capacitors on antiresonance," in *IET Science, Measurement and Technology*, vol. 10, no. 8, pp. 889-899, 11 2016.

[77] K. Agarwal, R. Jegadeesan, Y. X. Guo and N. V. Thakor, "Wireless Power Transfer Strategies for Implantable Bioelectronics," in *IEEE Reviews in Biomedical Engineering*, vol. 10, pp. 136-161, 2017.

[78] M. Zargham and P. G. Gulak, "Maximum Achievable Efficiency in Near-Field Coupled Power-Transfer Systems," in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 6, no. 3, pp. 228-245, June 2012.

[79] D. W. Seo, J. H. Lee and H. S. Lee, "Optimal Coupling to Achieve Maximum Output Power in a WPT System," in *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 3994-3998, June 2016.

[80] K. V. Schuylenbergh, R. Puers, "Exact Link Formulae," in *Inductive Powering*, Springer, 2009.

[81] D. M. Pozar, *Microwave Engineering*, 4th Edition, John Wiley and Sons Inc., pp. 178-194, 2011.

[82] P. Sidharthan, G. Narayanan and S. K. Datta, "Experimental investigation on reverse recovery characteristics of high-performance high-frequency diodes," *2017 IEEE International Conference on Signal Processing, Informatics, Communication and Energy Systems (SPICES)*, Kollam, 2017, pp. 1-6.

[83] Y. Huang, N. Shinohara and T. Mitani, "Impedance Matching in Wireless Power Transfer," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 2, pp. 582-590, Feb. 2017.

[84] Linear Technology, *LTC3564*, LTC3564 Datasheet, 2008.

[85] A. Ayachit, D. K. Saini, M. K. Kazimierczuk and T. Suetsugu, "Three-coil wireless power transfer system using class E2 resonant DC-DC converter," *2015 IEEE International Telecommunications Energy Conference (INTELEC)*, Osaka, 2015, pp. 1-4.

[86] C. Schmidt and M. Buchholz, "Extended Discussion on Non-Identical Planar Resonant Coils for Frequency Splitting Elimination in Wireless Power Transfer Systems," *Smart SysTech 2016*, Duisburg, Germany, 2016, pp. 1-11.

[87] L. D. Smith and E. Bogatin, *Principles of Power Integrity for PDN Design–Simplified: Robust and Cost Effective Design for High Speed Digital Products*. Prentice Hall, 2017.

[88] M. Swaminathan and A. E. Engin, *Power Integrity Modeling and Design for Semiconductors and Systems*. Prentice Hall 2007.

[89] S. Mueller et al., "Design of High Efficiency Integrated Voltage Regulators with Embedded Magnetic Core Inductors," *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, 2016, pp. 566-573.

[90] M. L. F. Bellaredj, et al.,"Fabrication, characterization and comparison of composite magnetic materials for high efficiency integrated voltage regulators with embedded magnetic core micro-inductors", in *Journal of Physics D: Applied Physics*, September 2017.

[91] B. Razavi. *Rf Microelectronics*. Upper Saddle River, NJ, Prentice Hall, 1998.

[92] Texas Instruments, *Understanding Buck Power Stages in Switchmode Power Supplies*, March 1999.

[93] Texas Instruments, *350-mA, 6-MHz High-Efficiency Step-Down Converter in Low Profile Chip Scaling Package*, TPS62615 Datasheet, 2010.

[94] H. M. Torun et al., "Machine Learning Driven Advanced Packaging and System Miniaturization of IoT for Wireless Power Transfer Solutions," *IEEE 68th Electron. Compon. Technol. Conf. (ECTC)*, 2018 accepted.

[95] H. M. Torun, M. Swaminathan, A. K. Davis and M. L. F. Bellaredj, "A Global Bayesian Optimization Algorithm and its Application to Integrated System Design", in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2018.

[96] I. Kowase, T. Sato, K. Yamasawa and Y. Miura, "A planar inductor using Mn-Zn ferrite/polyimide composite thick film for low-Voltage and large-current DC-DC converter," in *IEEE Transactions on Magnetics*, vol. 41, no. 10, pp. 3991-3993, Oct. 2005.

[97] D. Hackler, D. G. Sime and S. F. Wald, "Enabling Electronics With Physically Flexible ICs and Hybrid Manufacturing," in *Proceedings of the IEEE*, vol. 103, no. 4, pp. 633-643, April 2015.

[98] M. Poliks et al., "A Wearable Flexible Hybrid Electronics ECG Monitor," *2016 IEEE*

66th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, 2016, pp. 1623-1631.