Greetings from

Georgia Tech

Integrated Approach to Power Delivery for Electronic Systems (An Industry/University Consortium)

Madhavan Swaminathan

John Pippin Chair in Electromagnetics

School of Electrical and Computer Engineering

Director, Interconnect and Packaging Center

Georgia Tech Institute for Electronics and Nanotechnology

INTERCONNECT and PACKAGING CENTER

Outline

- Overview
    - Integration trends and Power Delivery

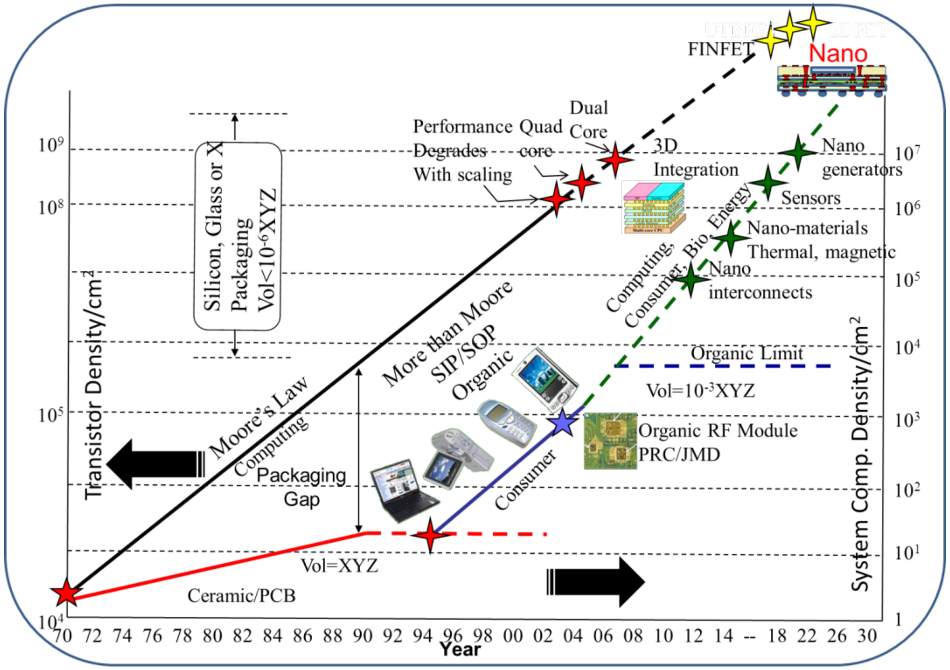
- Industry/University Consortium
    - Consortium Model & Details
    - Thrust Areas

- Facilities

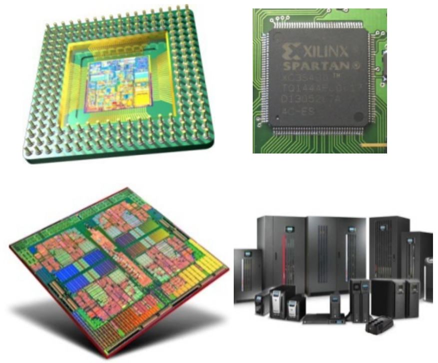
- Summary

Overview

IC and Package Integration Trends



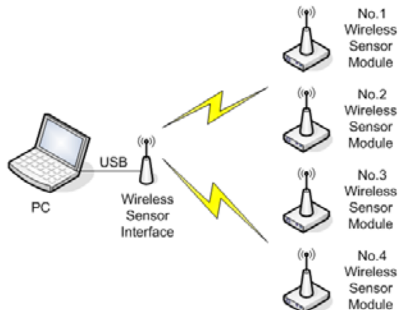
Ref: M. Swaminathan and K. Han, "Design and Modeling For 3D ICs and Interposers", WSPC 2013



High/Med Power

Low Power

Ultra Low Power

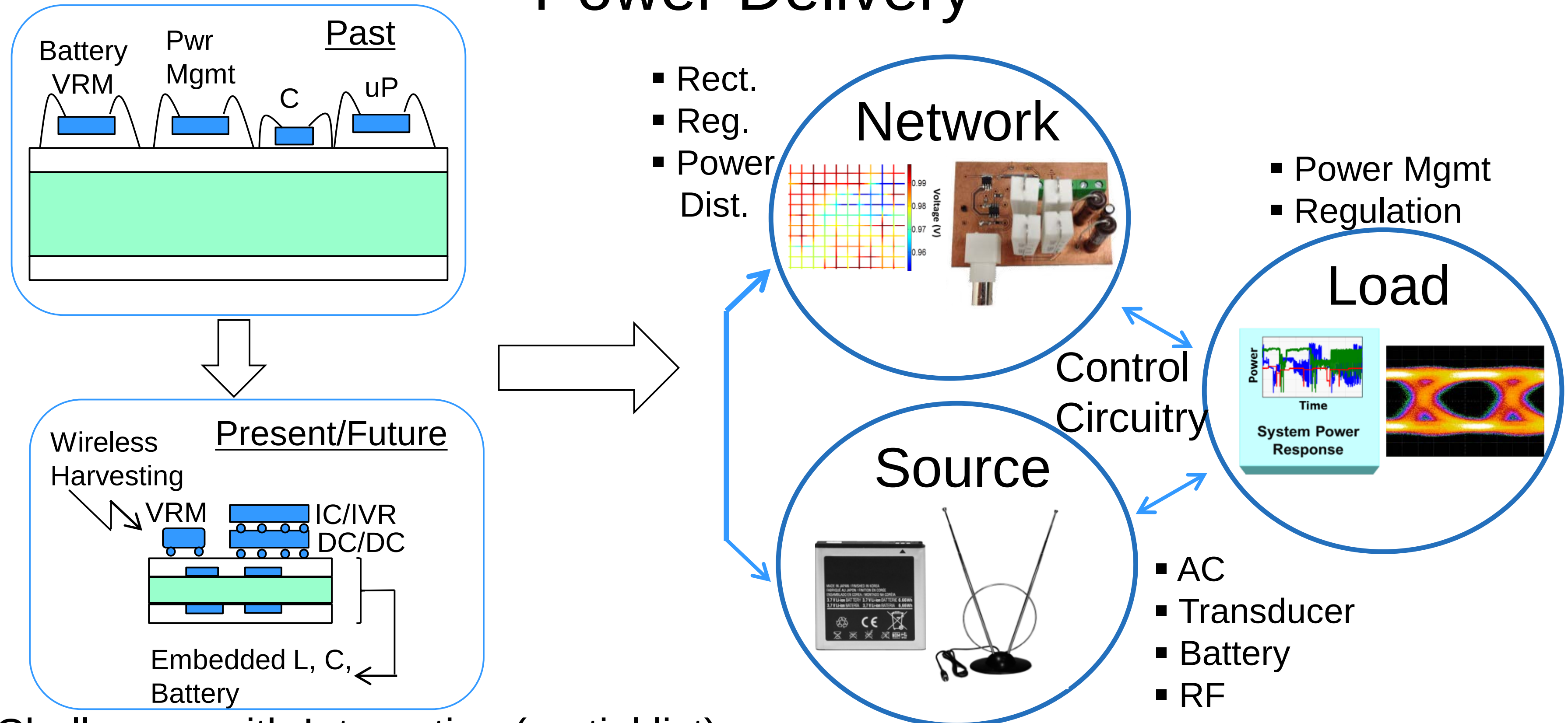


Ultra-Ultra Low Power

- Volume of Systems is decreasing
- Functionality is increasing
- Made possible through <u>Moore Scaling</u> (IC) & <u>More than Moore Scaling</u> (Packaging)
- Providing CLEAN POWER is becoming a major challenge

- Multitude of systems
- Each system class with unique power requirements
- Poses unique challenges for POWER DELIVERY

Power Delivery



- Challenges with Integration (partial list)
  - Need for high speed & high efficiency Integrated Voltage Regulators
  - Integration of high density storage elements such as Caps and Inductors
  - Wireless power transfer with buck/boost converters and integrated battery
  - Power distribution/Isolation networks with minimum decoupling capacitors
  - Rectifier less energy conversion & Energy Harvesting from far field
  - Architectural level power management
  - ....

Industry-University Consortium

- To address the integration challenges for Power Delivery, Georgia Tech proposes a Industry/University Consortium
  - Launch date: Sep 15, 2015

- Consortium Model
  - Based on industry membership ($60K/year for 2 years min.)
  - Pre-competitive research
  - 6 year duration with 2 year long projects
  - Industry joins for a minimum of 2 years
  - Industry defines and mentors projects working with faculty & students
  - Access to students, research trained in power delivery, for internship or full time positions
  - Consortia wide Non Exclusive Royalty Free (NERF) IP Model
  - Technology transfer to industry
  - Significant Leveraging through IEN/GT investment

Consortium Details

- Four Thrust Areas
  - Thrust I: Integrated Voltage Regulators
  - Thrust II: Power Distribution
  - Thrust III: Wireless Power Transfer
  - Thrust IV: Power Delivery Solutions for Self Powered IoT Devices
- Projects cut across thrusts
  - Integrated approach to power delivery
  - Industry joins consortium (not thrust)
  - Industry defines and mentors projects working with faculty
- Project scope and Duration
  - Design – Build – Characterize – Deliver
  - 2 year deliverable with technology transfer
  - Fabrication either by industry or/and Georgia Tech
- An Integrated Industry/Faculty/Student/Management Team
  - Faculty with complementary expertise
  - Students mentored by industry
  - Managed by Full time Center Staff

Integrated Team


Paul Kohl PhD


Muhannad Bakir PhD

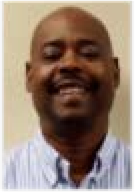

Saibal Mukhopadhyay PhD


Arijit Raychowdhury PhD


Madhavan Swaminathan PhD


Hua Wang PhD


Sudhakar Yalamanchili PhD


George E White PhD


Dean Sutter

Faculty Expertise

- Digital/Analog
- RF/Wireless
- IC/Package Design
- Control
- Passives
- Integration 2D/2.5D/3D
- Packaging
- Architecture
- Co-Design
- IVR/LDO
- Harvesting
- Battery

Industry/Faculty/Student Team

Consortium Managed by full time staff through IEN and IPC @ Georgia Tech

Georgia Tech Institute for Electronics and Nanotechnology

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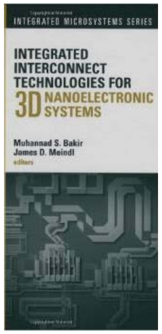
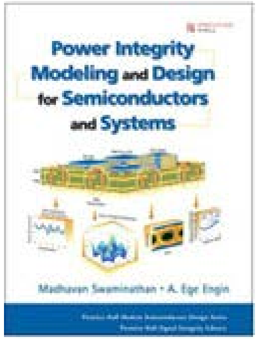
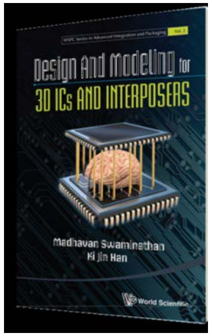
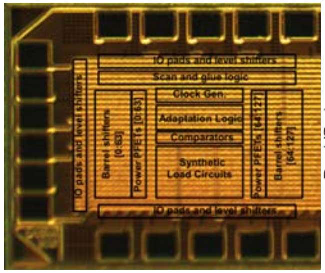
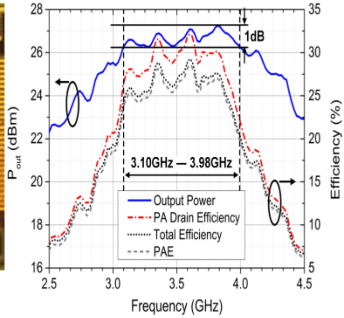
Prior Work (published) & Know How



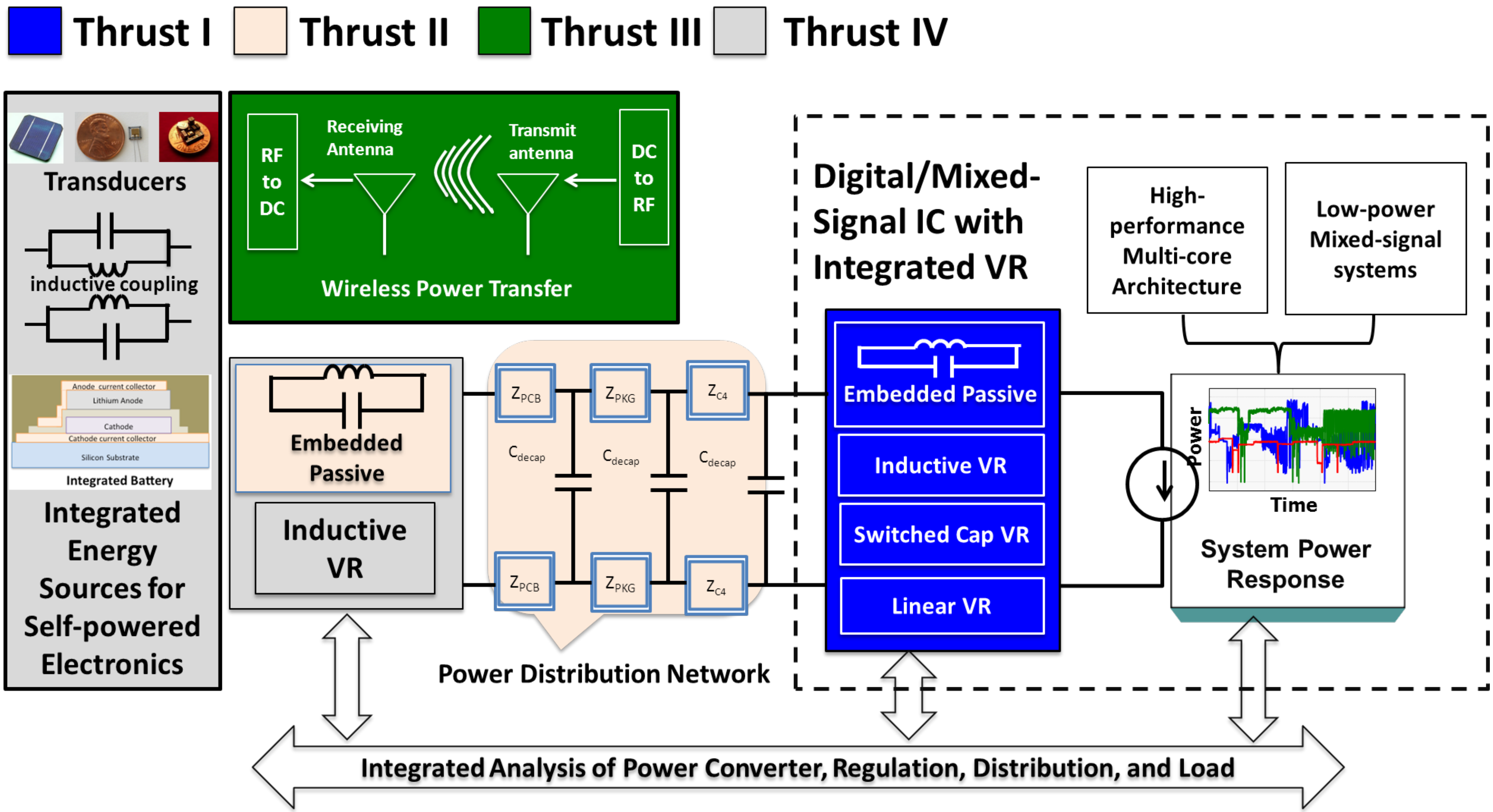








Integrated Approach to Power Delivery



Thrust I: Integrated Voltage Regulators

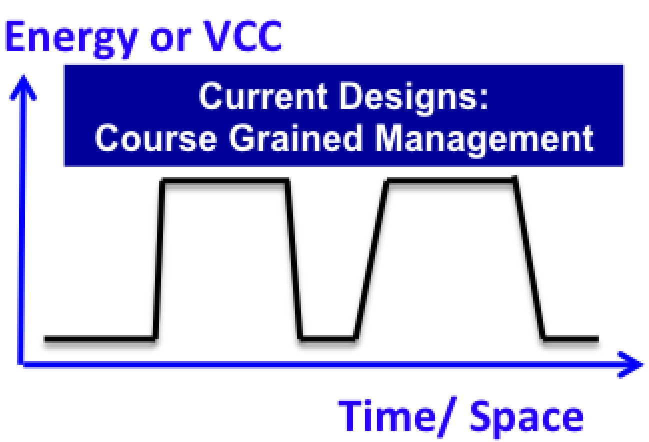
Thrust Leader: Prof. Arijit Raychowdhury

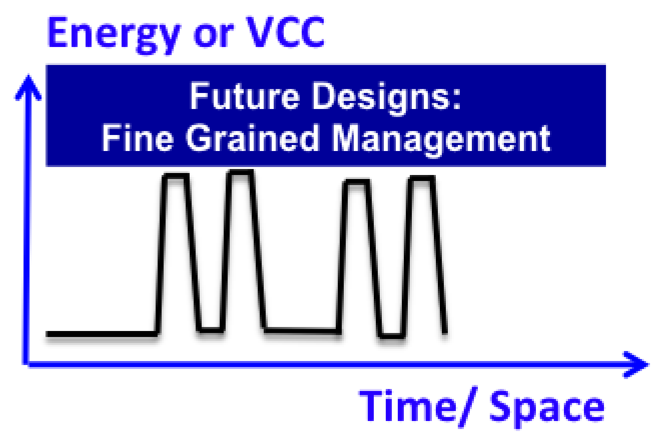
❑ Objective

Develop new circuits and topologies for integrated DC-DC converters and voltage regulators in conjunction with micro-architecture for energy-efficient and fine-grained spatio-temporal power management with wide dynamic ranges.

❑ Tasks

1. Integrated Buck Converters
2. Switched Capacitor IVRs
3. Linear point-of-load (PoL) IVRs
4. Embedded Passives
5. IVR enabled Microarchitecture level Power Management

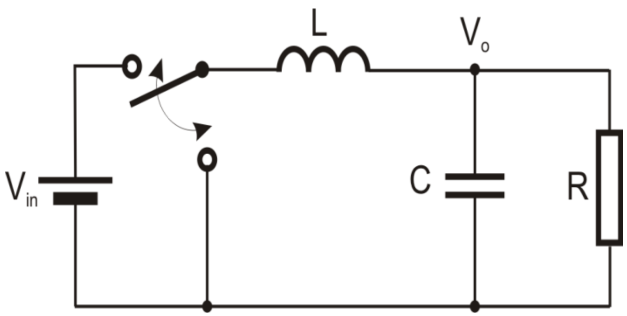


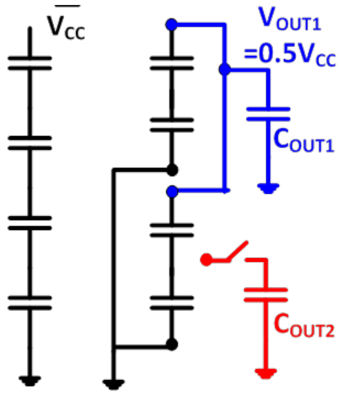


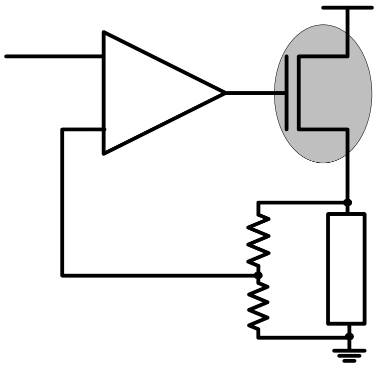
Technical Approach

Embedded Passives in-package and on-die

High density inductors and capacitors







LC-VR

- High Frequency operation
- Pulse-Frequency Modulation Schemes
- Single Inductor Multiple Output Designs

SC-VR

- Multiple conversion ratios
- Die integration
- Finer domains
- Ripple mitigation

Linear Regulator

- Low efficiency
- Die integration
- Narrow Vout range
- Finest domains
- Fastest response

Application of IVRs in micro-architectural power management

- Enable fine-grained spatio-temporal power management
- Interaction of IVRs with system states, DVFS states

Thrust II: Power Distribution

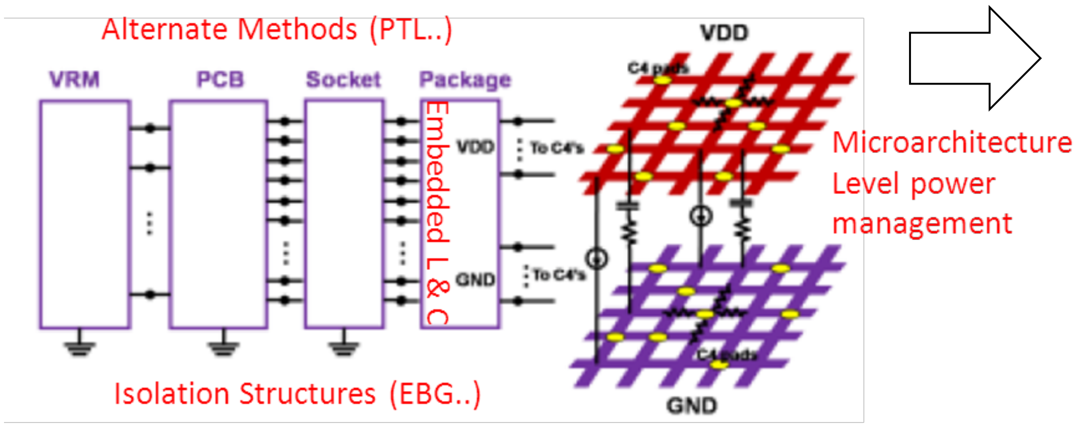
Thrust Leader: Prof. Madhavan Swaminathan

❑ Objective

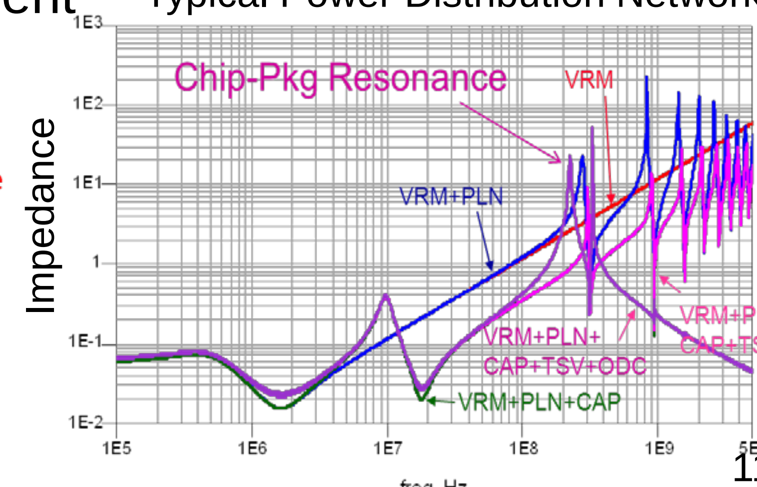
Develop new techniques and technologies in conjunction with microarchitecture level power management methods that provide best a) power integrity; b) signal integrity and c) isolation using minimum components, real estate and power consumption

❑ Tasks

1. Embedded Inductors
2. Embedded Capacitors
3. Alternate Methods
4. Isolation Techniques
5. Microarchitecture level Power Management



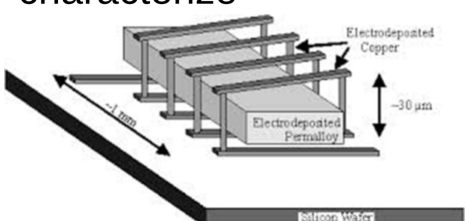
Typical Power Distribution Network

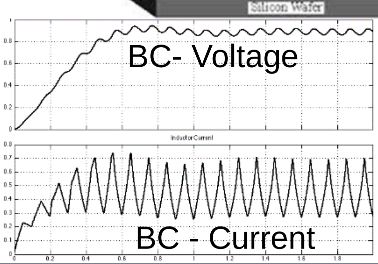


Technical Approach

Task 1
Embedded Inductors

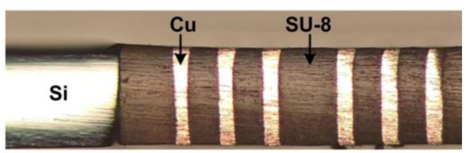
- Materials: Ultra low loss Insulation High Perm. Cores
- Optimum permeability for core based on application
- Determine effect of B-H Hysterisis on Buck Converter and optimize μ_r
- Fabricate embedded coiled inductors with min. size using simplified processes
- Integrate with Buck Converter (BC) & characterize



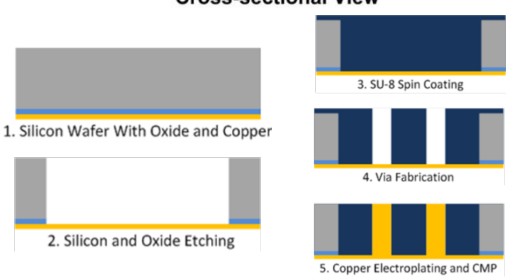


Task 2
Embedded Capacitors

- Develop innovative low cost interposer with low loss polymer embedded via fabrication in photo-defined polymer wells
- Develop innovative concepts for dense Capacitors for Mid-High frequency decoupling using established platform



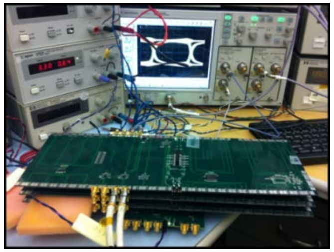
Cross-sectional View



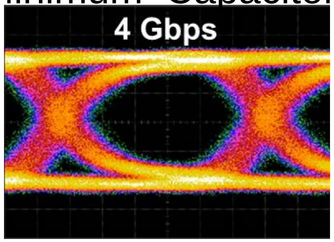
Task 3
Alternate Methods

- Minimize resonances in PDN
- Minimize capacitors
- Embedded capacitors
- Compensation techniques to minimize Power (Integrated LDO..)
- Maximize Signal & Power Integrity through PDN Design by construction

New PDN -Stacked Board

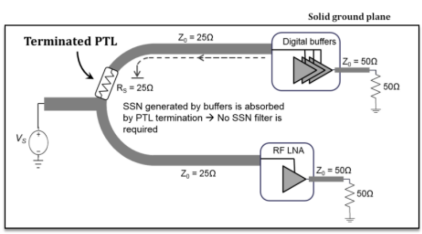


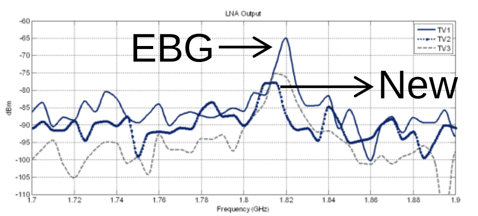
Minimum Capacitors



Task 4
Isolation Structures

- Focus on Mixed Signal (Digital/Analog/RF)
- Eliminate extra components (Ferrite Beads, caps…)
- Use appropriate Referencing
- Achieve >70dB isolation over wide band w/ minimum EMI - EBG, PTL ….





Thrust III: Wireless Power Transfer

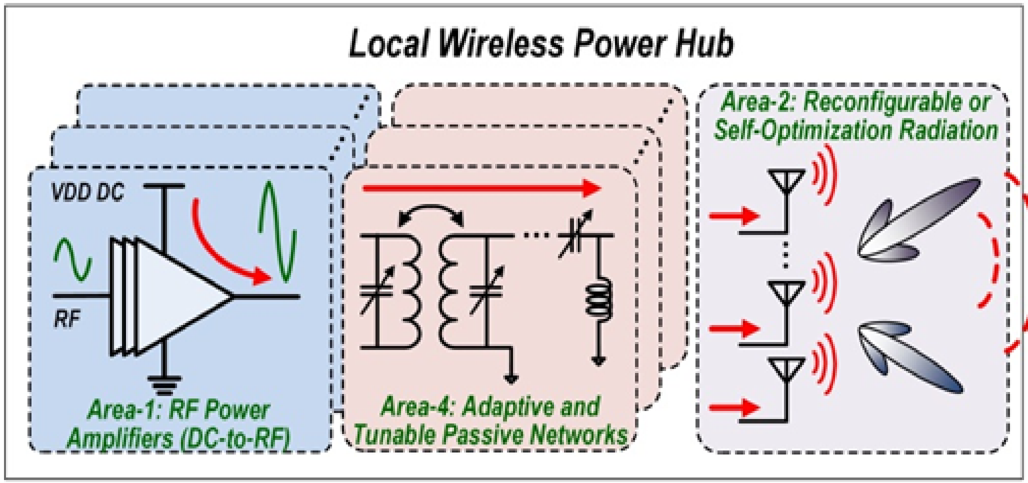
Thrust Leader: Prof. Hua Wang

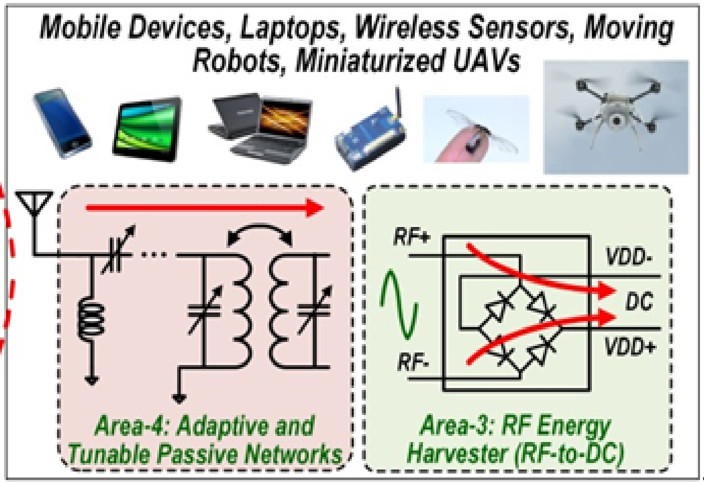
❑ Objective

Develop new technologies to achieve high-efficiency far-field radiation based power transfer (10× to 100× efficiency improvement). Applications include mobile devices/local “wireless power hub”, moving robots or UAVs, wireless sensor networks, IoT devices.

❑ Tasks

1. High-Efficiency, Power-Scalable, and Freq.-Agile RF Power Amplifier for DC-to-RF Conversion
2. Reconfigurable/Self-Optimized Radiation
3. RF Energy Harvester for RF-to-DC Conversion
4. Adaptive and Tunable Passive Networks





Technical Approach

Task 1 DC-to-RF

•High-Efficiency PA Architectures at Peak/Back-Off P_{out}

•Multi-Band or Broadband PA Operation

•PA/VR Co-Designs

•PA/Novel-Passive Devices Co-Designs

Task 2 Radiation

•Phased-Array for Reconfigurable Beam-Forming, EIRP Enhancement, and Mobile Device Tracking

•Ultra-Low-Power Array

•Co-Design with Novel Passives

Task 3 RF-to-DC

•High Efficiency Harvester (especially at Low Received RF Power Level)

•Co-Designs with VR/Integrated Battery

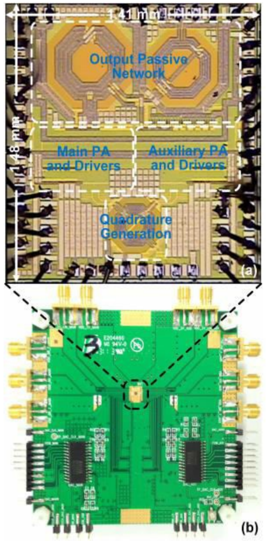
•Architecture-Level Optimization

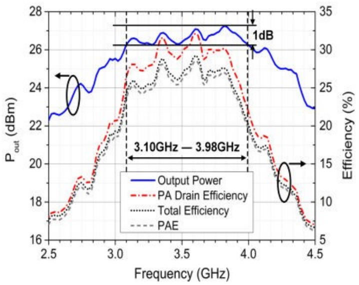
Task 4 Passive Networks

•Antenna Load Tuning

•P. V. T. Variations

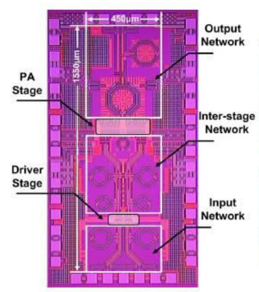
•Co-Designs with Novel Passives

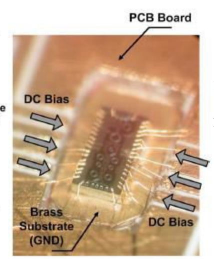




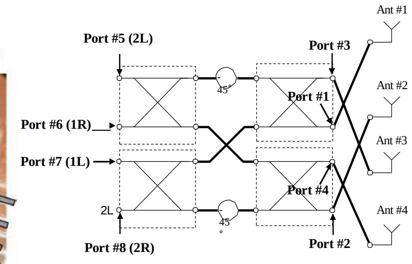
Digital Doherty Polar PA in

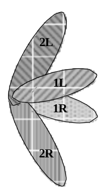
2014 IEEE RFIC Best Student Paper Award 1st Place

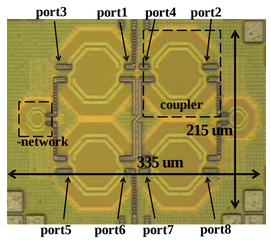


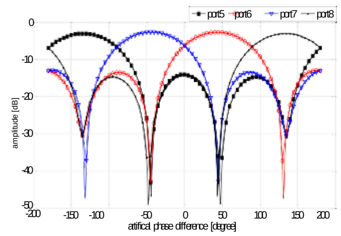


IEEE ISSCC 2010 & JSSC 2010









A 60 GHz 4 × 4 Butler Matrix in 65nm CMOS

2013 IEEE CICC

Thrust IV: Power Delivery Solutions for Self-Powered Internet-of-Thing Devices

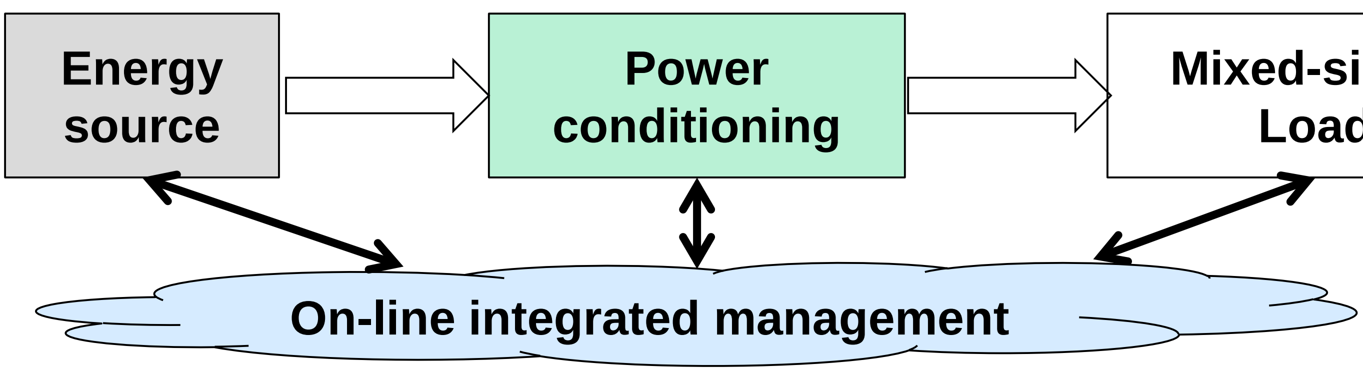
Thrust Leader: Prof. Saibal Mukhopadhyay

❑ Objective

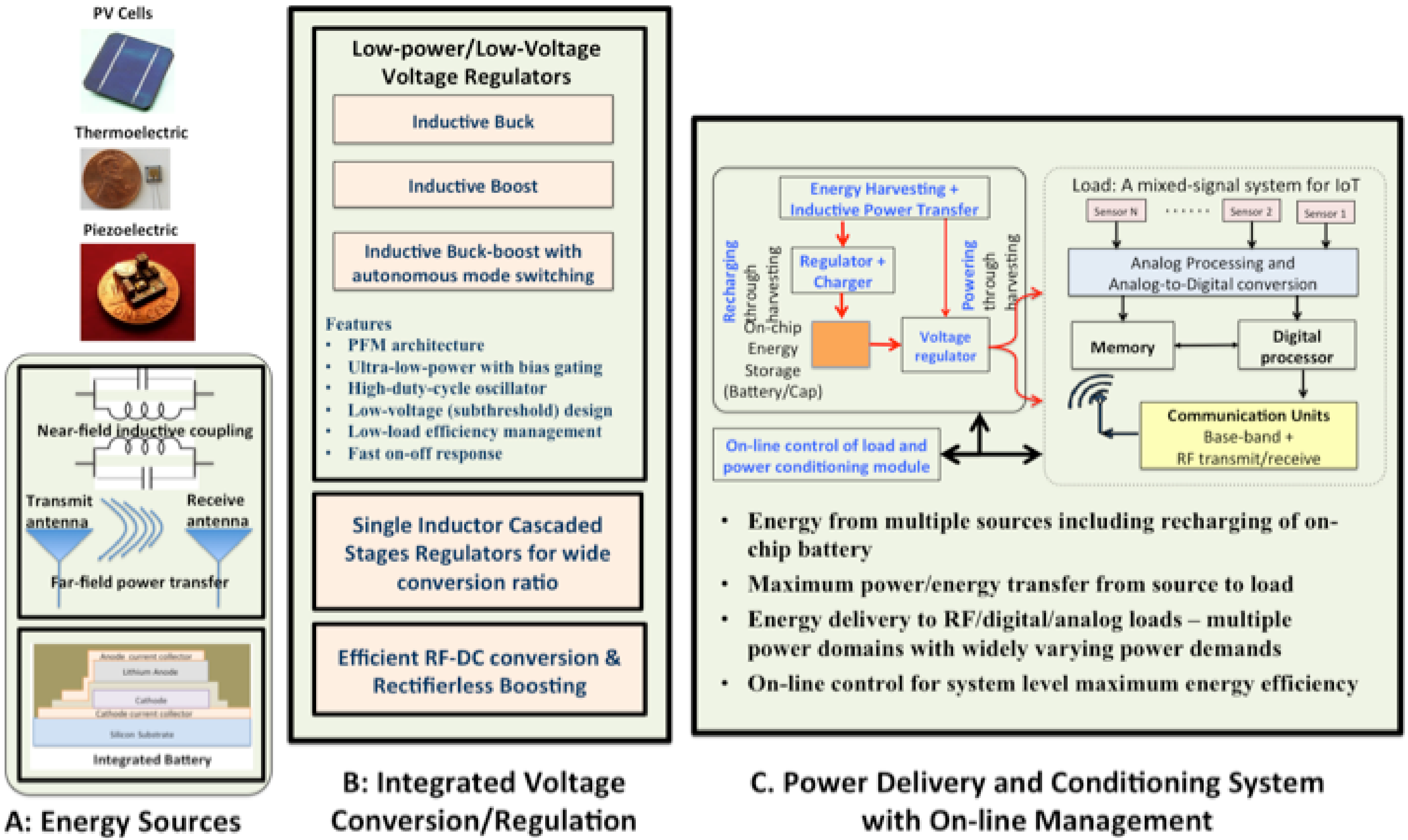
Design of power management solutions for ultra-low-power devices. The thrust will develop technologies in three major areas: (a) integrated energy sources; (b) integrated voltage conversion/regulation; and (c) power delivery and conditioning system with on-line management.

❑ Tasks

1. Integrated energy storage – battery and high-density capacitor
2. Energy transfer through near-field coupling
3. Low-power/Low-voltage inductive converters with wide conversion ratio
4. Power Delivery and Conditioning System with On-line Management



Technical Approach



Example Projects

- Important that projects cut across thrusts

Project	Thrust I					Thrust II					Thrust III				Thrust IV			
	Task 1	Task 2	Task 3	Task 4	Task 5	Task 1	Task 2	Task 3	Task 4	Task 5	Task 1	Task 2	Task 3	Task 4	Task 1	Task 2	Task 3	Task 4
1	x				x	x		x										
2			x					x	x				x	x				
3						x		x					x		x	x	x	x

- Project 1

  - Application: High Perf/FPGA
  - Integrated inductive buck VR
  - Power Management
  - Embedded inductors
  - Embedded capacitors
  - Power distribution methods

- Project 2

  - Application: RF Energy harvesting (far field)
  - Passives Tuning
  - Linear regulation
  - Power Distribution
  - RF passives
  - Isolation

- Project 3

  - Application: IoT
  - Near/far field coupling
  - Embedded inductors
  - Rectifier less DC conversion
  - Integrated battery
  - Power Management

Facilities

- ❑ Experience in electronics design & micro/nano fabrication
- ❑ Recent formation of the Institute of Electronics and Nanotechnology (IEN)
  - 9 Centers
  - Interconnect & Packaging Center (IPC)
  - Power Delivery Consortium
- ❑ Marcus & Pettit Laboratories
  - 30,000 square feet of clean room
- ❑ State of the art measurement facility
  - High Speed Equipment
  - 325GHz RF labs;40Gbps Digital labs
  - Digital w/ PC & FPGA interfaces for automatic & scan based testing
  - Direct probing
  - Low current, low power with sub nA and sub nW precision
- ❑ State of the art Design Facility
  - Large Computer Clusters with Design & Analysis Software

What can a Company Expect by joining the Consortium?

- ❑ Access to leading edge <u>precompetitive</u> research on Power Delivery that combines IC, Package, their interactions and their integration for a suite of applications
- ❑ <u>Definition and mentoring</u> of a project aligned with other company needs that maximizes ROI
- ❑ Access to <u>all projects</u> in the consortium
- ❑ IC design, package/module design, fabricated IC/package/module, models and measurements (details provided in the thrust presentations)
- ❑ Access to students, research trained in power delivery, for internship or full time positions
- ❑ Access to world class faculty focusing on power delivery
- ❑ Inclusion of <u>specific technologies</u> from company members through supplemental projects (protected by NDA, Additional $$):
  - Example 1: Module designed using substrate technology supplied by Company A using the same chip sets. Substrate fabrication and assembly done by Company A. Modeling and measurements by Georgia Tech
  - Example 2: Power Inductors and/or capacitors supplied by Company B assembled on module. Modeling and measurements by Georgia Tech.

Schedule

- Webinar – Nov. 19, 2014 (Attendance: 120+)
  - Slides and White Paper available

- Jan. 2015 – May 22, 2015
  - Several individual meetings with companies
  - Used to shape the specifics of thrust areas
  - This will be seen in the thrust presentations
  - Several companies interested in joining

- Today's workshop
  - Collect additional input and feedback from industry
  - Use to finalize consortium scope

- Condensed workshop in San Diego
  - May 25, 2015
  - Additional input and feedback from industry

- May 25, 2015 – Sep 1, 2015
  - Individual conf. calls or F2F meetings with companies (as required)

- Launch consortium – Sep 15, 2015

Summary

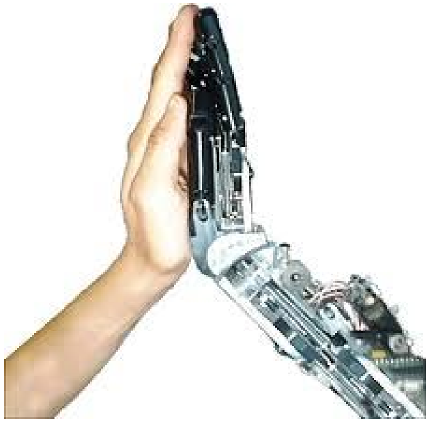
- Georgia Tech just launched an Industry/University Consortium titled "Integrated Approach to Power Delivery for Electronic Systems"
  - Launch Date: Sep 15, 2015
  - $60K/year membership for 2 years (min)

- Member company can define a project
  - Cuts across atleast two thrusts
  - Aligned with other companies to maximize ROI
  - SIP Solution for Power Delivery
  - Focus is on Design, Modeling and Measurements

- Details on Consortium Membership & Execution (Contact: Dean Sutter)

- We look forward to welcoming you to join the consortium on Power Delivery for Electronic Systems (PDES)

Thank You



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